Unconventional Phase-Locked Loops Simplify Difficult Designs

By James A. Crawford

One of the most important building blocks in modern day communication and signal processing systems is the phase-locked loop. This topic has been written about extensively over the years, but the four techniques described in this article will likely be unfamiliar to most readers. These methods should prove helpful across a wide range of applications, including both analog / RF and digital signal processing domains.

Technique #1: Addition of a Passive Lag-Lead Network

Readers familiar with PLL design will recognize the classic type-2 fourth-order loop filter shown in Figure 1. This PLL is fourth-order because the single-ended loop filter has three capacitors (C_1, C_3, and C_5) and the voltage-controlled oscillator (VCO) contributes one additional pole.

Focusing first on Figure 1, the phase detector in this case has two outputs that are often labeled as the *pulse-up* (PU) and *pulse-down* (PD) outputs. Denoting the phase detector gain by K_d (V / rad.), the VCO tuning sensitivity by K_v (rad. / sec. / V), and assuming that the loop filter component values are perfectly symmetric, the open-loop gain transfer function can be written as

$$G_{OL}(s) = \left(\frac{\omega_n}{s}\right)^2 \frac{(1+s\tau_2)}{(1+s\tau_3)(1+s\tau_5)} \tag{1}$$

where

$$\tau_1 = (R_1 + R_2)C_3 \tag{2}$$

$$\tau_2 = R_5(C_3 + C_5) = \tau_4 + \tau_5 \tag{3}$$

$$\tau_3 = \frac{R_1 R_2}{R_1 + R_2} C_1 \tag{4}$$

$$\tau_4 = R_5 C_3 \tag{5}$$

$$\tau_5 = R_5 C_5 \tag{6}$$

$$\omega_n = \sqrt{\frac{K_d K_v}{N\tau_1}} \tag{7}$$

With reasonable choices for the additional pole locations compared to a classical type-2 second-order PLL, it is convenient to adopt the classical definition for damping factor and write

$$\varsigma = \frac{1}{2}\omega_n \tau_2 \tag{8}$$

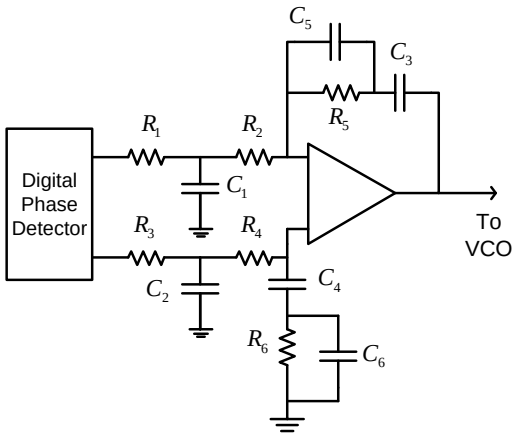

Figure 1 Classic loop filter configuration for a type-2 4th-order PLL

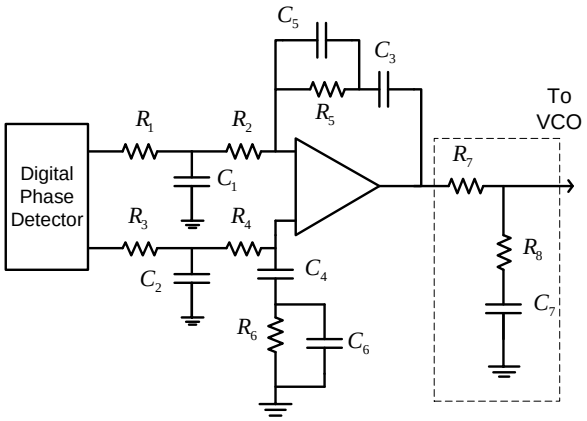

Figure 2 Classic loop filter configuration appended with additional lag-lead type RC network

These results are fairly standard and Bode methods can be used to explore the open-loop gain and phase of (1) quickly.

For a numerical example, assume that the PLL has the following parameters:

ω_n	Natural frequency, rad / s	2π 20 kHz
ζ	Damping factor	0.80
N	Feedback divider ratio	100
K_d	Phase detector gain, V / rad	0.525
K_v	VCO tuning sensitivity, rad / s / V	2π 100 MHz

In order to keep the phase detector referred noise floor low while not excessively loading the phase detector outputs, resistors R_1 and R_2 are chosen to be 510Ω. From this point on, the remaining component values can be derived using a simple spreadsheet like that shown in Table 1. The only other design parameters that are needed are the ratios τ_2 / τ_5 and τ_3 / τ_5. The ratios need to be made as large as possible in order to preserve PLL gain and phase margin, and are consequently both chosen equal to 10 in this example.

A casual inspection of the computed results shows an immediate issue with the design value for R5 because it is only 56Ω. Many op-amps could exhibit their own stability issues if configured for such low high-frequency gain. A second concern is that the VCO's K_v value is fairly high and this will make circuit layout issues between the op-amp output and the VCO critical. Never the less, calculation of the closed-loop gain functions [2]

$$H_1(f) = \frac{G_{OL}(f)}{1+G_{OL}(f)}$$
$$H_2(f) = \frac{1}{1+G_{OL}(f)} \quad (9)$$

using (1) can be done as shown in Figure 3. With the circuit configuration in Figure 1 left unchanged, there is little recourse available to address these two very real design issues just mentioned. Another degree of design freedom is needed in order to improve the design.

Table 1 Spreadsheet Calculation for PLL Component Values[1]

	Inputs	Calculated
Loop Natural Frequency, Hz	**20000**	
in rad/s		1.2566E+05
Loop Damping Factor	**0.8**	
Feedback Divider Ratio	**100**	
VCO Tuning Sensitivity, MHz/V	**100**	
VCO Kv, rad/sec/V		6.2832E+08
Phase Detector Kd, V/rad	**0.525**	
Resistors R1 and R2	**510**	
Time Constant tau_1		2.0889E-04
Capacitor C3		2.0480E-07
Time Constant tau_2		1.2732E-05
Ratio of tau_2 to tau_5 (>>1)	**10**	
Time Constant tau_5		1.2732E-06
Time Constant tau_4		1.1459E-05
Resistor R5		5.5954E+01
Capacitor C5		2.2755E-08
Ratio of tau_2 to tau_3	**10**	
Time Constant tau_3		1.2732E-06
Capacitor C1		4.9931E-09

[1] Calculated using U17365 Technique 1 Loop Filter Values.xlsx, available at www.am1.us .

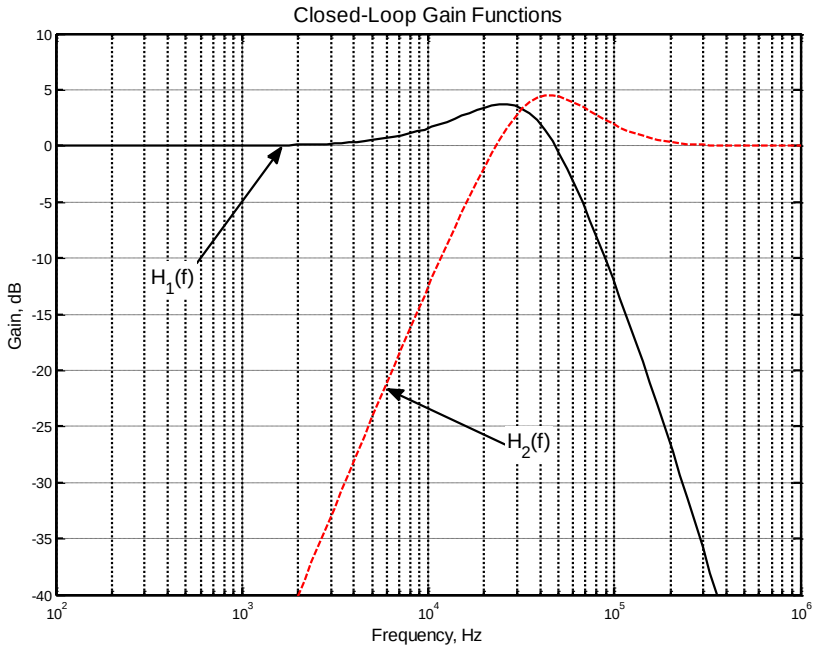

Figure 3 Closed-loop gain functions[2] for Figure 1 when configured with the component values given in Table 1

Improving the Design

The previous design example can be markedly improved by appending what appears to be a passive lag-lead network following the op-amp circuit as shown in Figure 2. Although it has the appearance of a passive lag-lead network, it is used to perform an entirely different function.

The best way to understand the role of this additional RC section is to mentally replace capacitor C_7 with an ideal battery. When the battery voltage is set to precisely the value needed by the VCO to be on frequency, the output voltage from the op-amp will be equal to this same value in steady-state operation and there will be no dc current flow through R_7 and R_8. In this context, it is as if the battery is acting like an ideal coarse tuning voltage for the VCO. Since there is no current flow through R_7 and R_8, the resistive divide ratio R_8 / (R_7 + R_8) can be made as small as desired thereby reducing the effective VCO tuning sensitivity seen at the op-amp output by the same ratio. This ratio provides the extra degree of design freedom needed as mentioned in the previous section.

The voltage transfer function of this passive network between the op-amp output and the VCO's tuning port input is given by

$$G_{post}(s) = \frac{1 + sR_8C_7}{1 + s(R_7 + R_8)C_7} \Rightarrow \frac{\tau_6}{\tau_7}\frac{s + \tau_6^{-1}}{s + \tau_7^{-1}} \tag{10}$$

where $\tau_6 = R_8 C_7$ and $\tau_7 = R_7 C_7 + \tau_6$. In order to properly use this network, the pole- and zero-frequencies in (10) must be placed well inside the closed-loop bandwidth where they will not affect the stability margins of the PLL. Assuming that these frequencies are much less than the

[2] Computed using u17333_technique1.m, available at www.am1.us .

natural frequency of the PLL, $G_{post} \rightarrow \tau_6 / \tau_7$ for all frequencies of interest. An example will make the details more clear.

Assume that the 100 MHz / V tuning sensitivity is to be dropped down to an effective VCO tuning sensitivity of 5 MHz / V. This will require the resistor ratio $R_8 / (R_7 + R_8) = 1 / 20$. Choosing resistor R_8 to be set to 200Ω as discussed later, R_7 = 3.8 kΩ. In order to have the pole and zero well within the PLL's closed-loop bandwidth, C_7 = 1 μF is chosen corresponding to a zero-frequency of 796 Hz and a pole-frequency of 39.8 Hz. The gain and phase of this network versus frequency are shown in Figure 4.

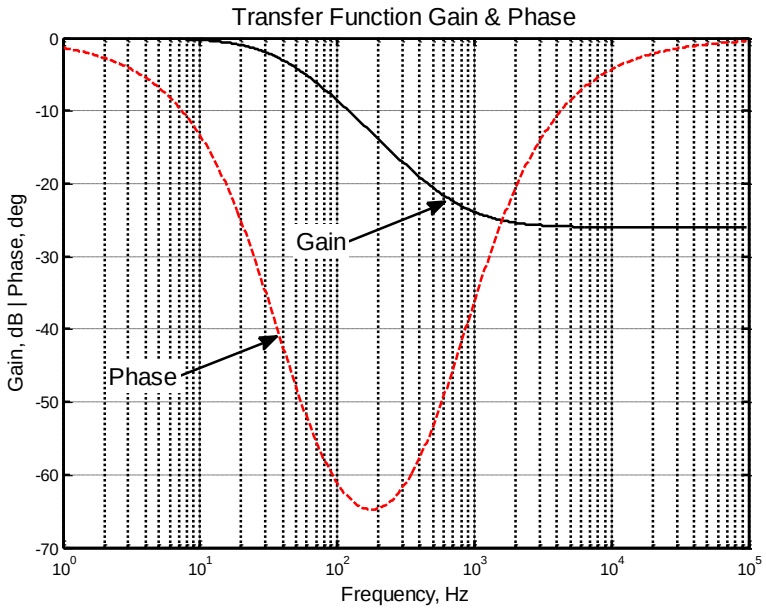

Figure 4 Gain and phase for the passive RC-network[3] with R_7 = 3.80 kΩ , R_8 = 200Ω , and C_7 = 1 μF

Although the additional RC network increases the gain at low frequencies substantially, the gain margin and phase margin remain nearly the same provided that the PLL natural frequency and damping factor are kept the same. Letting K_{veff} represent the effective VCO tuning sensitivity, the design equations for Figure 2 that must be modified are

$$K_{veff} = \frac{R_8}{R_7 + R_8} K_v = \frac{\tau_6}{\tau_7} K_v \tag{11}$$

$$\omega_n = \sqrt{\frac{K_d K_{veff}}{N \tau_1}} \tag{12}$$

Appending (10) to (1) produces the open-loop gain function

$$G_{OL}(s) = \left(\frac{\omega_n}{s} \right)^2 \frac{(1 + s\tau_2)}{(1 + s\tau_3)(1 + s\tau_5)} \frac{\left(s + \tau_6^{-1}\right)}{\left(s + \tau_7^{-1}\right)} \tag{13}$$

[3] Calculated using u17335_technique1.m, available from www.am1.us .

The other circuit values can be found by using the spreadsheet shown in Table 1 while changing the K_V value from 100 MHz/V to 5 MHz/V. The resulting closed-loop gain functions are almost identical to the original case whereas the additional open-loop gain at low frequencies is apparent as shown in Figure 5.

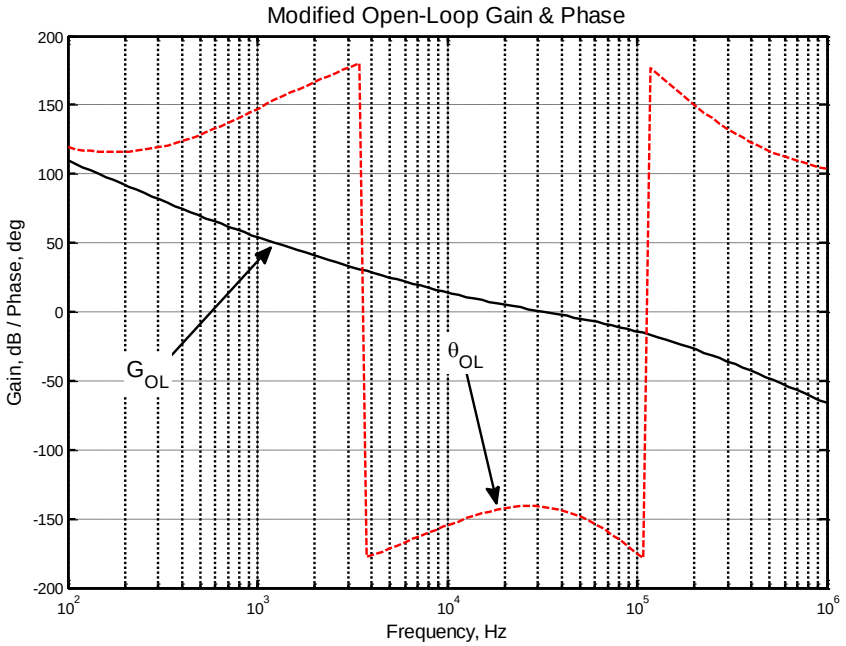

Figure 5 Open-loop gain and phase for the modified loop filter case[4] shown in Figure 2. For frequencies less than about 10 Hz, the open-loop gain is 20 Log_{10}(20) = 26 dB higher than for the original loop filter.

Performance Characteristics

The discussion that follows is better facilitated using the annotated schematic shown in Figure 6. Compared to the original design given in Table 1, resistors R_5 and R_6 now have a much more practical value of 1120Ω and the main feedback capacitors C_3 and C_4 have been reduced to 10 nF from 0.2 μF.

At first glance, it may appear that the large value for R_7 and its related Johnson noise could hamper noise performance due to the VCO's tuning sensitivity of 100 MHz / V. Looking back from the VCO's tuning port to the left, however, the tuning port sees the parallel combination of R_7 and R_8 which is only 190 Ω. This modified loop filter configuration frequently makes it easier to handle noise problems rather than making them more difficult.

Referring to Figure 4, the additional RC network increases the open-loop gain for frequencies less than about 1 kHz up to as much as 26 dB. This can be helpful in thwarting low-frequency power supply noise or excessive close-in 1/*f* noise in the VCO.

The primary disadvantage of the modified loop filter arrangement is that the transient response for any large frequency step is slowed substantially. If the new PLL output frequency requires a large change in the VCO tuning voltage, the active portion of the loop filter must charge or discharge capacitor C_7 through the large resistance R_7 + R_8. In some situations, particularly tracking-loop situations, this characteristic can actually be used to advantage.

[4] Computed using u17333_technique1.m, available at www.am1.us .

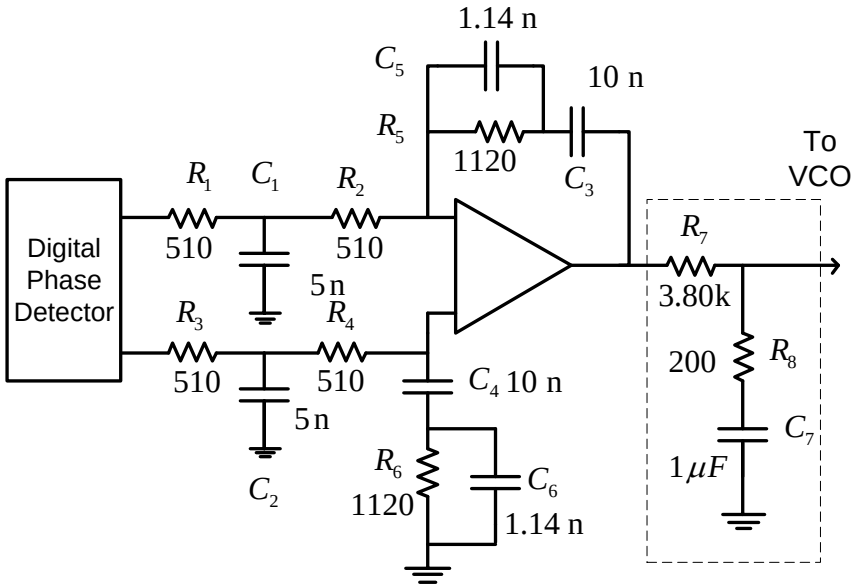

Figure 6 Modified loop filter with component values shown

Technique #2: Long-PLLs

The terminology *long-PLL* [1] normally appears in the context of phase-locked receivers like those used for deep-space communications. A representative example is shown in Figure 7. The IF bandpass filter and baseband lowpass filter normally have reasonably small bandwidths and together result in appreciable group delay that complicates loop stability. Space receivers must usually accommodate appreciable Doppler rates thereby leading to an even more difficult compromise between closed-loop bandwidth, acquisition capability, and stability. A simple modification of the classic type-2 lag-lead loop filter equations can be used to solve this otherwise difficult design problem.

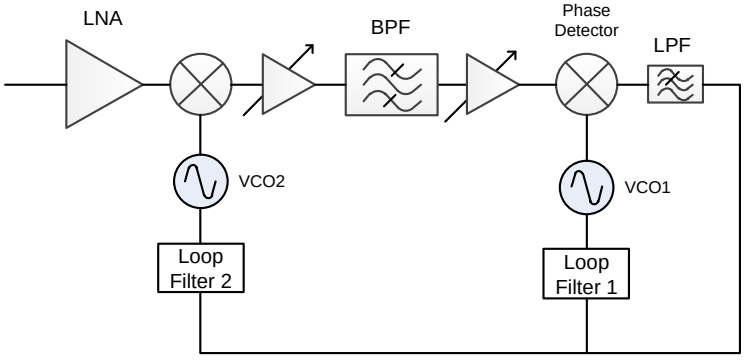

Figure 7 A representative *long-PLL* within a double-conversion receiver architecture

The open-loop gain function for a classic type-2 PLL is given by

$$G_{OL}(s) = \frac{K_d}{N}\frac{1+s\tau_2}{s\tau_1}\frac{K_v}{s} \tag{14}$$

It is a simple matter to re-write (14) as

$$G_{OL}(s) = \frac{K_d}{N}\left(\frac{1}{s\tau_1} + \frac{\tau_2}{\tau_1}\right)\left(\frac{K_v}{s}\right) \tag{15}$$

where the proportional and integral terms in the active lag-lead network have been separated. Frequency domain analysis can be used to show that most of the stability issues come from appreciable delay applied to the proportional gain term whereas the integral term is far more tolerant to delay. The design improvement in the context of Figure 7 then comes by putting most if not all of the proportional gain in Loop Filter 1 where no group delay contribution from the narrow bandpass filter comes into play. The remainder of the open-loop gain function (15) is situated into Loop Filter 2.

In order to quantitatively look at this design modification further, assume that the group delay through the bandpass filter is represented by τ_{BPF}, and the group delay through the lowpass filter is represented by τ_{LPF}. Only one of the several possible gain distribution variations will be considered here where the loop filter transfer functions are given by

$$\begin{aligned} G_1(s) &= \alpha\frac{\tau_2}{\tau_1} \\ G_2(s) &= (1-\alpha)\frac{\tau_2}{\tau_1} + \frac{1}{s\tau_1} \end{aligned} \tag{16}$$

where α is an arbitrary gain-term ($0 \le \alpha \le 1$) that distributes the proportional gain between the two loop filters. Assuming that both VCOs have the same tuning sensitivity and that N = 1, the Laplace transfer function between the phase at the receiver's input θ_{in} and the phase error seen by the phase detector θ_e is given by

$$\frac{\theta_e}{\theta_{in}} = \frac{s^2\exp(-s\tau_{BPF})}{s^2 + \omega_n^2\exp(-s\tau_{LPF})\left\{\alpha\tau_2 s + \left[1+(1-\alpha)\tau_2 s\right]\exp(-s\tau_{BPF})\right\}} \tag{17}$$

In this form, it is easy to recognize that the effective open-loop gain function is given by

$$G_{OL}(s) = \left(\frac{\omega_n}{s}\right)^2\exp(-s\tau_{LPF})\left\{\alpha\tau_2 s + \left[1+(1-\alpha)\tau_2 s\right]\exp(-s\tau_{BPF})\right\} \tag{18}$$

The closed-loop gain function H_1 using (9) and (18) is shown for a variety of α values in Figure 8 illustrating how effective this technique can be for constraining what would otherwise be unacceptable gain-peaking. Without this technique, nearly 15 dB of gain-peaking would occur as shown, but with it, the peaking is reduced to a very acceptable 4 dB. The phase margin versus parameter α for this example is shown in Figure 9. Evidence of poor long-loop stability in the time domain is manifested as increasingly under-damped phase error transient responses as shown in Figure 10 for several values of α.

As simple as splitting the lag-lead transfer function apart in (15) is, this is a very effective way to counter filter-related group delay in a long PLL.

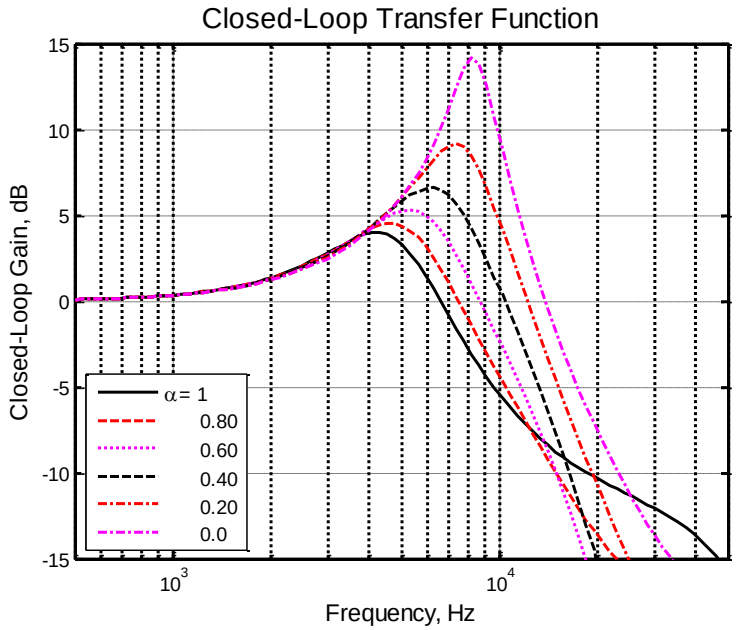

Figure 8 Variation of the long-loop closed-loop gain characteristic[5] with parameter α. In this example, the loop natural frequency is ω_n = 2 π 5 kHz, the damping factor is ζ = 0.707, with τ_{LPF} = 2.12 μs and τ_{BPF} = 17 μs.

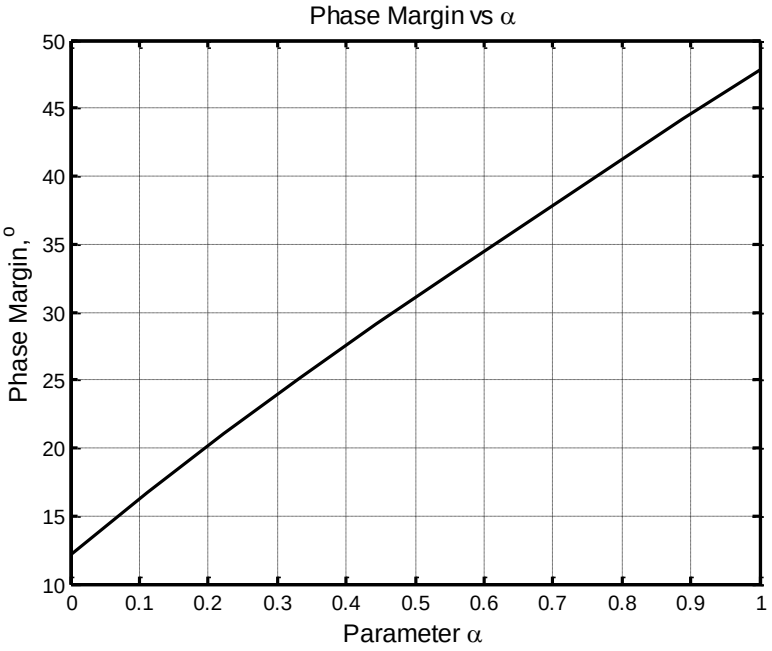

Figure 9 Phase margin[6] versus parameter α corresponding to Figure 8

[5] Calculated using u17346_technique2.m, available at www.am1.us .
[6] Ibid.

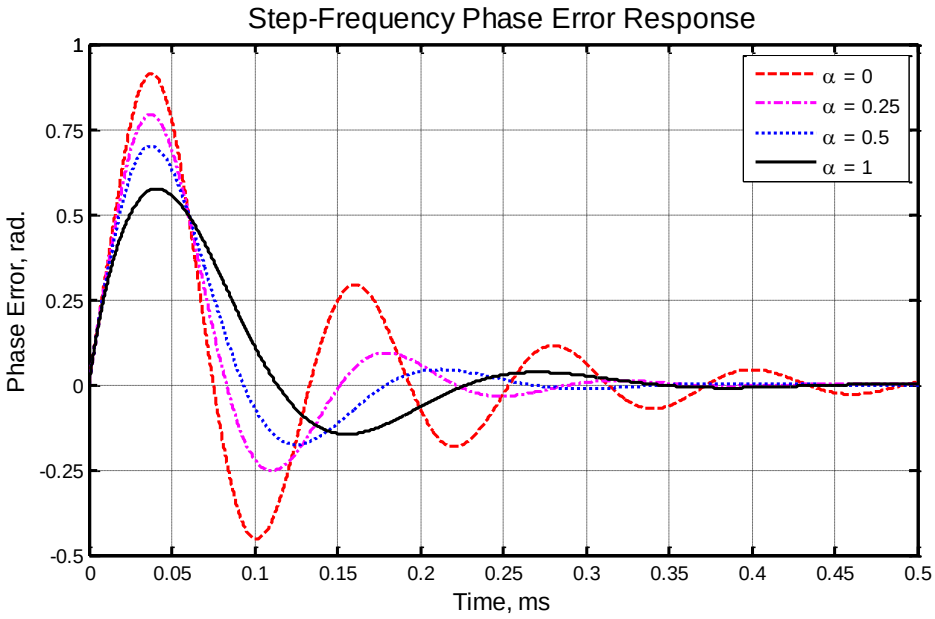

Figure 10 Transient phase error response[7] to a 5 kHz input frequency step as a function of parameter α corresponding to Figure 8

Technique #3: Haggai Constant Phase Margin Loop

The Haggai PLL is named in honor of Ted Haggai who was a senior scientist at Hughes Aircraft Company many years ago. This technique was mentioned in my 1994 textbook on frequency synthesizers and expanded further in my 2008 textbook on advanced phase-lock techniques. The method has its roots in the constant phase network methods of Bode nearly 100 years ago.

The Haggai PLL uses a modified lag-lead network like that shown in Figure 11. The beauty of this method is that the closed-loop bandwidth can be varied by a factor of even 100:1 while the phase margin remains nearly unchanged.

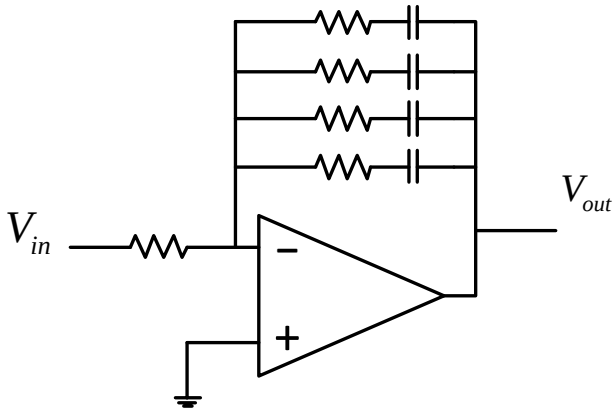

Figure 11 Single-ended active loop filter architecture for the Haggai PLL

[7] Calculated using u17363_transient_method2.m, available at www.am1.us .

In a phase-locked receiver, the phase detector gain is always a function of the input signal to noise ratio (SNR) due to small-signal suppression effects imposed by the noise. Since the PLL's natural frequency is a function of the phase detector gain as shown by (7), and the PLL's damping factor is a function of natural frequency ω_n based upon (8), the PLL's phase margin normally deteriorates as the input SNR decreases. The PLL's ability to track Doppler frequency error is also degraded under these conditions. Haggai was granted a patent[8] on his constant phase margin technique in 1970 because his method ingeniously solved these problems.

The Haggai method is also very useful when the closed-loop bandwidth is to be purposely adjustable over a wide frequency range in a synthesis application, for example. Even though the bandwidth can be changed significantly, the phase margin remains almost constant.

There is no closed-form solution for the lag-lead zeros used in the Figure 11 schematic. These parameters must be found using numerical methods as discussed in Chapter 6 of [2].

In the Haggai loop filter case utilizing two sections as shown in Figure 12, its open-loop gain function is given by

$$G_{OL}(s) = \left(\frac{\omega_n}{s}\right)^2 \frac{(1+s\tau_1)(1+s\tau_2)}{1+s\tau_p}\left(\frac{1}{1+s\tau_x}\right) \tag{19}$$

where $(1 + s\tau_x)^{-1}$ represents the additional lowpass filter section following the Haggai lag-lead network and

$$\omega_n = \sqrt{\frac{K_d K_v}{N(C_1 + C_2)}} \tag{20}$$

$$\tau_p = \frac{C_1 C_2}{C_1 + C_2}(R_1 + R_2) \tag{21}$$

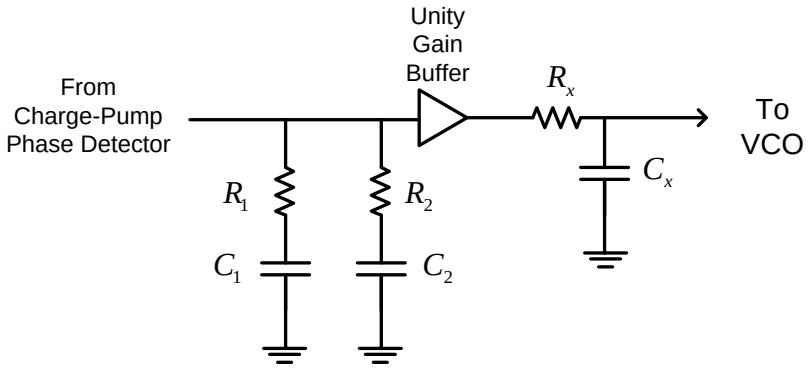

Figure 12 Two-section Haggai loop filter

In the case of a step-frequency change applied to the PLL (represented by a step-change in the VCO tuning voltage of δV), the Laplace transform of the PLL's output phase error is given by

[8] U.S. Patent 3,551,829 granted 29 Dec 1970, titled "Phase Lock Receiver with a Constant Slope Network."

$$\theta_o(s) = \delta V\ K_v \frac{(1+s\tau_p)(1+s\tau_x)}{s^2(1+s\tau_p)(1+s\tau_x)+\omega_n^2(1+s\tau_1)(1+s\tau_2)} \tag{22}$$

A simple design example helps to illustrate how this PLL configuration performs. Based upon design information provided in [2], consider the case where R_1 = 1k, R_2 = 692.928, R_x = 1k, C_1 = 46.78 nF, C_2 = 3.436 nF, Cx= 265 pF, K_d = 0.001 / π (A/rad), K_v = 2π 25 MHz/V, and N = 1000. The natural frequency given by (20) is 5.022 kHz. The open-loop gain and phase for this example are shown in Figure 13. Since the open-loop phase remains almost constant over the frequency range of about 8 kHz to over 200 kHz, the closed-loop bandwidth can be varied over this same span with almost no affect on the PLL stability margins. The closed-loop gain functions are very well behaved as shown in Figure 14.

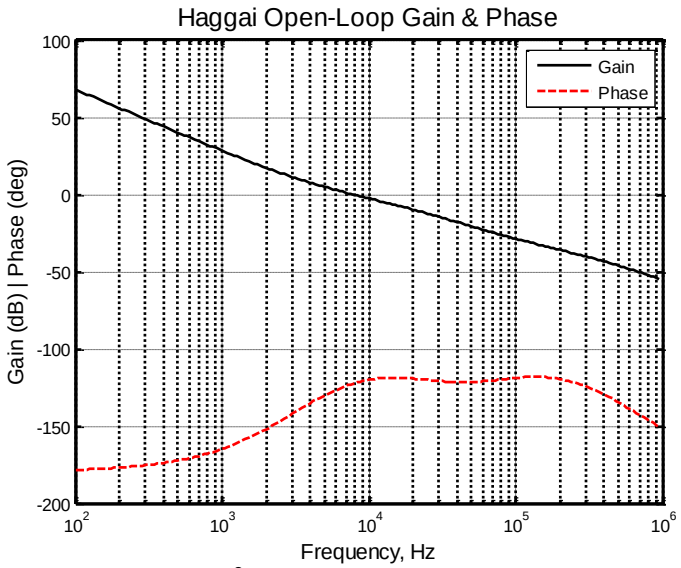

Figure 13 Open-loop gain and phase[9] for the two-section Haggai PLL example. Note that the open-loop phase is equal-ripple about –120° from about 8 kHz to slightly over 200 kHz representing a bandwidth range of 25 : 1.

[9] Calculated using u17364_technique3.m, available at www.am1.us .

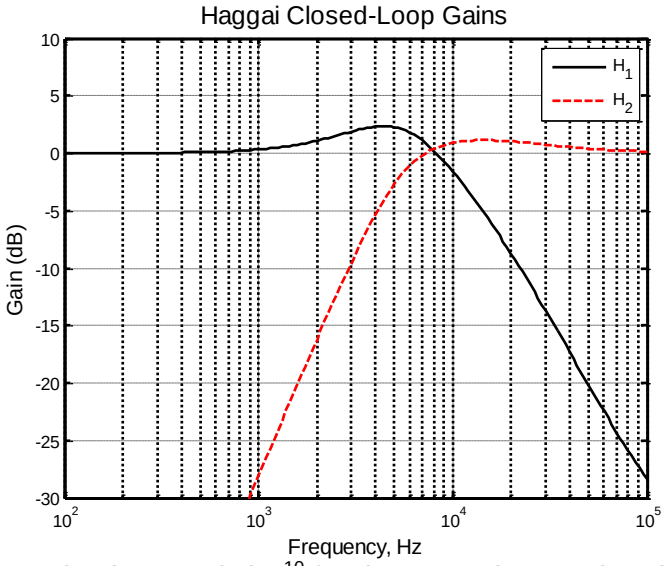

Figure 14 Closed-loop gain characteristics[10] for the Haggai example. The gain-peaking is very low because the phase margin is 60°.

There is only one characteristic of the Haggai method that may present an issue and that is its time domain transient response behavior. The penalty for bandwidth flexibility with constant phase margin is an extended time domain response tail as shown in Figure 15 as compared to an optimized traditional type-2 PLL having the same bandwidth. The PLL bandwidth (ω_n) is changed over a 10:1 range in this figure and no hint of loop instability emerges due to the constant phase margin delivered by this method.

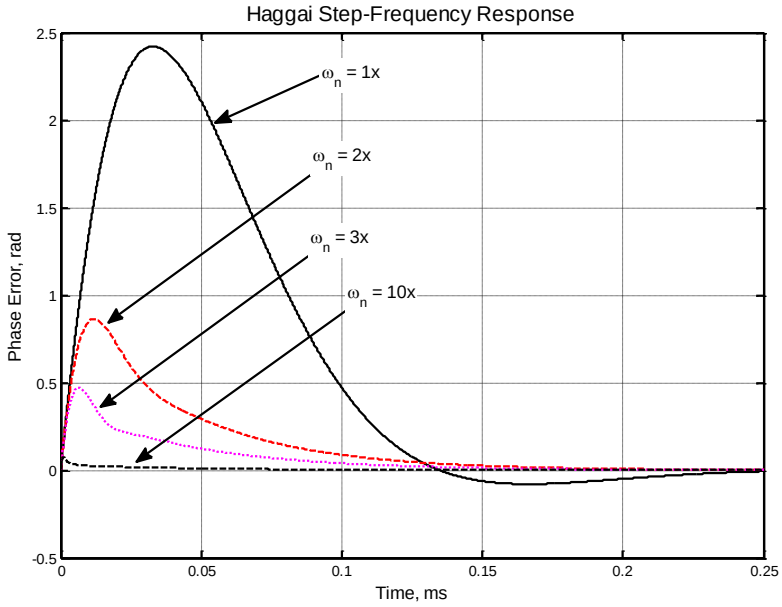

Figure 15 Transient phase error response of the Haggai PLL[11] to a 1 mV step-change in the VCO tuning voltage. Natural frequency cases shown correspond to 5.02 kHz for the 1x case up to 50.2 kHz for the 10x case.

[10] Ibid.

Technique #4: Quadri-Correlator

The rapid evolution of wireless systems over the past twenty years has led to truly exceptional integrated PLL devices, notably the *Platinum* family from National Semiconductor and more recently the Hittite HMC700. Even so, if the ultimate in phase noise performance is needed, a mixer-based phase detector of some kind must normally be used. Harmonic-sampling phase detectors are also a member of this category. One major disadvantage that must be addressed with mixer-based PLL approaches, however, is the dramatically reduced capture range that normally results. PLLs that implement the phase detector function digitally usually include a frequency discrimination capability that allows them to achieve phase-lock even if very large initial frequency errors are present whereas this feature is absent in mixer-based PLLs.

The quadri-correlator method has been known for a long time, having appeared in Gardner's classic book on PLLs [3]. This method as well as several other related frequency discriminator methods can be derived from the classic paper by Natali [4]. A variant of this method was used in [5] for differentiating between upper and lower sideband mixing products in an offset-PLL. Whereas many methods have been proposed and used to address this frequency pull-in limitation, the quadri-correlator method is particularly advantageous.

The quadri-correlator method gets its name from the fact that it requires in-phase (I) and quadrature-phase (Q) components of the RF signal to be resolved. Since the associated phase of the signal is given by

$$\theta = \tan^{-1}\left(\frac{Q}{I}\right) \tag{23}$$

implicit differentiation of this equation combined with recognizing $d\theta/dt$ as radian frequency ω results in the instantaneous frequency error being expressible as

$$\omega = \frac{I\dot{Q} - Q\dot{I}}{I^2 + Q^2} \tag{24}$$

where the overhead dots denote differentiation with respect to time. This result can be closely approximated with several remarkably simple analog circuits to produce a very effective frequency-discrimination capability.

A convenient approximation for the time derivatives in (24) is

$$\begin{aligned} \frac{dI}{dt} &\approx \frac{I\left(t+\tau/2\right) - I\left(t-\tau/2\right)}{\tau} \\ \frac{dQ}{dt} &\approx \frac{Q\left(t+\tau/2\right) - Q\left(t-\tau/2\right)}{\tau} \end{aligned} \tag{25}$$

where τ is a small time delay compared to the possible frequency errors involved, and substitution into (24) thereby produces

$$\omega \cong \frac{1}{\tau}\frac{I\left(t\right)\left[Q\left(t+\tau/2\right) - Q\left(t-\tau/2\right)\right] - Q\left(t\right)\left[I\left(t+\tau/2\right) - I\left(t-\tau/2\right)\right]}{I^2\left(t\right) + Q^2\left(t\right)} \tag{26}$$

[11] Ibid.

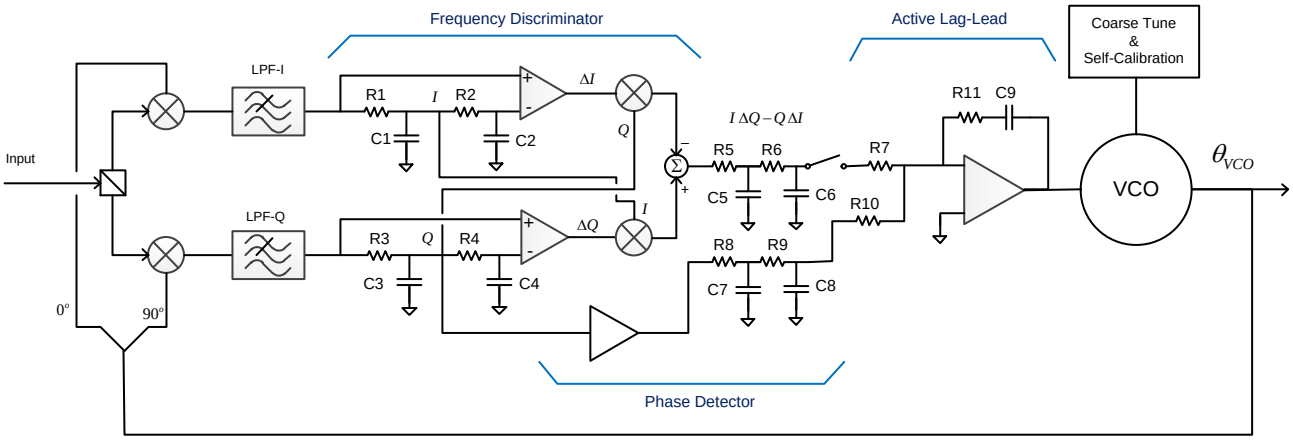

Figure 16 Mixer-based PLL configured with a quadri-correlator based frequency discriminator. Once the VCO has been frequency-locked, the frequency discriminator path is switched out leaving a conventional PLL.

Normally the 1 / τ is simply lumped in with other gain factors as a single proportionality constant, and the time delays in (26) can usually be approximately by using simple RC-sections as shown in Figure 16.

The frequency discriminator portion of Figure 16 can be analyzed using Laplace transforms based upon the simplified model shown in Figure 17. The key parameters are

τ_{FD}	Time delay associated with frequency discriminator
K_{FM}	Gain of frequency discriminator, V / Hz
H_{LPF}	Second-order passive lowpass filter that follows the discriminator
K_v	VCO tuning sensitivity in rad/s/V

The voltage transfer function of the lowpass filter immediately following the frequency discriminator is simplified if the $R_5 = R_6 = R_7 = R$ and $C_5 = C_6 = C$ to

$$H_{LPF}(s) = \frac{\omega_{LPF}^2}{s^2 + 4\omega_{LPF}s + 3\omega_{LPF}^2} \tag{27}$$

where ω_{LPF} = (RC)$^{-1}$. The bandwidth of the LPF-I and LPF-Q lowpass filters is usually very large compared to closed-loop bandwidth, so these filters are ignored in Figure 17 except for the delay that they present τ_{FD}.

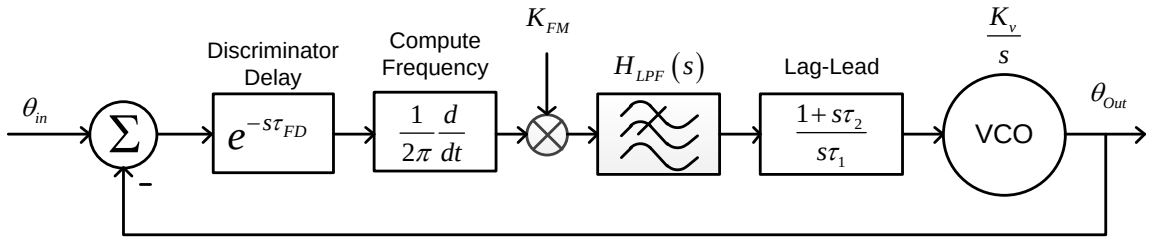

Figure 17 Linearized model for the frequency-locked loop

From Figure 17, the open-loop gain can then be written as

$$G_{OL}(s) = e^{-s\tau_{FD}} \left(\frac{s}{2\pi} \right) K_{FM} H_{LPF}(s) \left(\frac{1+s\tau_2}{s\tau_1} \right) \frac{K_v}{s} \tag{28}$$

A first-order design equation can be obtained by approximating exp($-s\tau_{FD}$) as $1 - s\tau_{FD}$ in (27) as

$$H_{LPF}(s) \approx \frac{1}{3} \frac{1}{1+s\gamma} \tag{29}$$

where $\gamma = 4 / (3\ \omega_{LPF})$. The characteristic equation for the system follows as

$$s^2 + s \frac{1+K'(\tau_2 - \tau_{FD})}{\gamma - K'\tau_2\tau_{FD}} + \frac{K'}{\gamma - K'\tau_2\tau_{FD}} = 0 \tag{30}$$

with $K' = K_{FM}\ K_v / (6\ \pi\ \tau_1)$. Based upon this result, the natural frequency and damping factor for the frequency-locked loop are approximately given by

$$\omega_n = \sqrt{\frac{K'}{\gamma - K'\tau_2\tau_{FD}}} \tag{31}$$

$$\varsigma = \frac{1+K'(\tau_2 - \tau_{FD})}{2} \sqrt{\frac{1}{K'(\gamma - K'\tau_2\tau_{FD})}} \tag{32}$$

It is immediately clear from these results that $\gamma > K'\ \tau_2\ \tau_{FD}$ is required in order to have any measure of loop stability. It can also be shown that the transient response of the FLL is optimized by choosing $\tau_2 = \tau_{FD}$.

It is convenient to use (9) in the context of (28) for computing the transient response of the FLL to a step-change in input frequency. Owing to the time-delay term present in (28), the inverse Laplace calculation must be done numerically. The example that follows illustrates how effective the quadri-correlator can be for reducing the initial frequency error in a FLL / PLL system like that shown in Figure 16. The parameter details are provided in Table 2. The closed-loop gain functions for this example are shown in Figure 18 and the well-behaved transient response to a step-change in frequency is shown in Figure 19.

A number of design parameters need to be considered when designing a frequency-locked loop including the magnitude of the initial frequency error possible, the switching-time required, and the manner in which the FLL is to be transitioned into a phase-locked loop configuration once the frequency error has been adequately reduced. Digital variants of the quadri-correlated based upon (26) can also be implemented for digital signal processing applications as well. Equations (31) and (32) are convenient approximations that can be used to begin the design process while more exact calculations using (28) or Spice-based simulations can be used to complete the detailed design.

Table 2 Frequency-Locked Loop Analysis Example

FLL Parameter	Value	Comments
τ_{FD}	125 ns	Delay through discriminator
K_{FM}	10^{-7} V / Hz	0.1V per MHz
K_v	2π 20 MHz/V	VCO tuning sensitivity
τ_1	1 µs	
τ_2	125 ns	Equal to τ_{FD}
ω_{LPF}	2π 250 kHz	
ΔF	10 MHz	Applied step-frequency for transient response

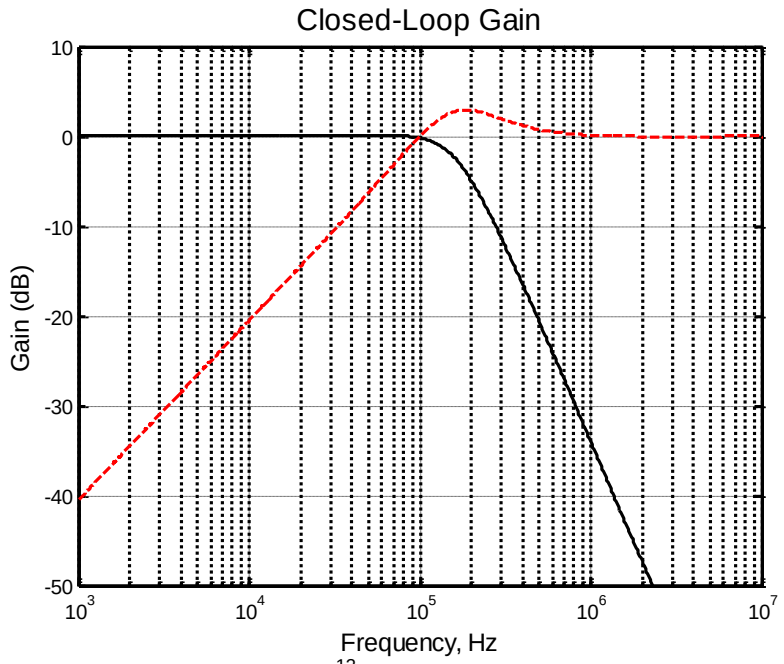

Figure 18 Closed-loop gain characteristics[12] for the frequency-locked loop detailed in Table 2

[12] Computed using u17368_technique4.m.

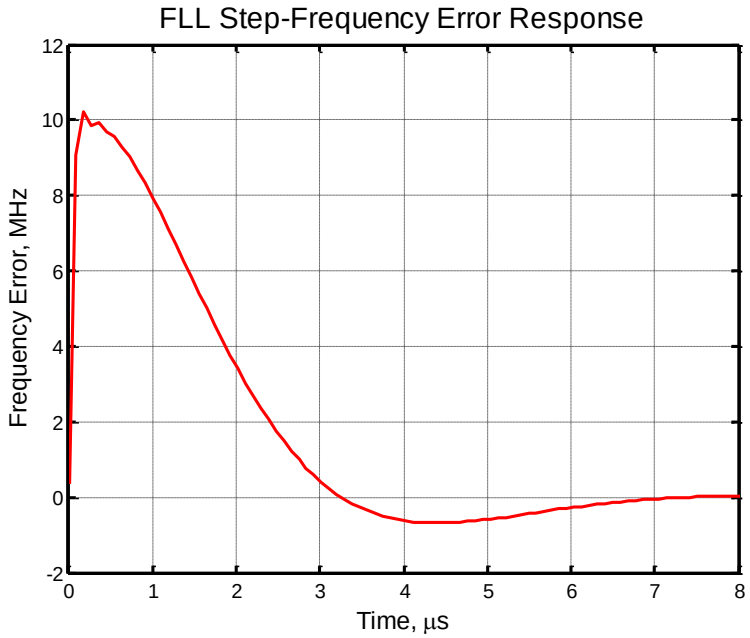

Figure 19 Frequency-locked loop step-frequency transient response[13] corresponding to Table 2 and Figure 18. Input step-frequency change applied was 10 MHz.

Summary

Four unconventional phase-locked loop methods have been presented that should strengthen and widen the tools available for all sorts of PLL designs. Additional information, including the MATLAB scripts used to create this article can be found at http://www.am1.us by following the hyperlink found on the home page.

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Number of Words = 3826

[13] Ibid.