A Multiple Antenna 5 GHz OFDM Single-Chip SiGe BiCMOS Transceiver for Wireless HDTV and Data Distribution

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Multiple antenna approaches for wireless systems have been used for many years. By utilizing the complex diversity properties of the channel, they can mitigate the effects of fading and dramatically improve receiver performance in the presence of multipath [1]. Unfortunately, these techniques can also dramatically raise the cost and DC power consumption of the system, since multiple receive antennas could require *multiple* complete downconversion stages. This cost and power dissipation penalty has limited most multiple antenna approaches in cellular and WLAN applications to simple selection diversity between two or three antennas [2]. We have developed a single-chip 5 GHz SiGe BiCMOS transceiver designed to accept inputs from up to *five* separate antennas, and downconvert the resulting signal to *two* low-frequency outputs for processing by the Magis CMOS digital baseband IC, for an overall maximum data rate of 54 Mbps. The complete system is designed to operate in dense closed spaces over distances greater than 250ft.,

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while maintaining Quality of Service (QOS) for the reliable transport of HDTV and other streams of multimedia content.

The key features of our single-chip RF solution are: “five-to-two” antenna selection at RF, an offset PLL for low phase noise, a low phase noise BiCMOS VCO, multiple transmitter gains for power level control, and automatic frequency calibration at power-up. These features, combined with the high level of integration, provide the numerous benefits of multiple antenna technology in consumer product applications.

Figure 1 shows the block diagram of the transceiver. Each of the five antennas is connected to a switched-gain LNA, which can be programmed by the baseband chip to work with either of the two subsequent receive chains. The choice of which two of the five antennas to select for downconversion is made at the baseband level, and the two outputs provide nearly identical performance to that of a full five-branch Maximum Ratio Combining approach, but at substantially lower DC power and die area. A heterodyne architecture, with a first IF at approximately 1GHz and a bandpass-sampled 60 MHz output, was chosen to achieve the highest possible sensitivity, selectivity and interference suppression consistent with minimum DC power consumption.

The front end SiGe LNAs provide gain switching, with a maximum gain of 19dB, NF of 3.9dB, IIP3 of -12dBm and a gain range of 18dB. The LNA's are followed by an RF 5-to-2 switch, which routes the two "best" antenna outputs to the downconverters. The switch is followed by a doubly balanced mixer/downconverter. The LNA and mixer provide a combined receiver image rejection of 25dB. The IF is routed through off-chip SAW filters into an IF LNA, followed by an IF image-reject downconverter and a 60MHz VGA. The VGA gain can be varied from -20dB to +50dB in steps of 1dB for a total receiver gain range of 105dB. The downconverted 60MHz signal is sampled by a 10-bit ADC in the baseband IC. The measured performance of the receiver is summarized in Figure 2, with a total noise figure of less than 4.5dB, and an IIP3 of -12dBm.

The first component in the transmit chain is a 60MHz programmable attenuator, used to calibrate gain variations. This is followed by a single side-band IF upconverter. The IF VGA consists of cascaded common-emitter stages, each with switchable degeneration. The gain can be varied from -30dB to +25dB in steps of 1dB. The IF output of the VGA is routed through the SAW filter (which is shared with RX2) into a single-sideband upconverter at 5.2GHz. The upconverter uses polyphase filters to generate in-phase and quadrature components of the LO and IF. The final block in the

transmitter is a two-stage power amplifier and an associated power detector for power control. Strict OFDM linearity requirements of dictate that the amplifier to be a Class A amplifier. The amplifier has switchable gain states of 26dB, 18dB, -4dB and -18dB in order to accommodate a variety of deployment scenarios. This switching is achieved by four parallel driver stages and two parallel output stages. Figure 3 shows the high gain output stage and the highest gain driver. On-chip inductors are used to create an inter-stage match and the output match is completely off-chip. The drivers use high f_T, low-breakdown devices to provide high gain whereas the output stage uses high breakdown devices to achieve maximum output power. The saturated output power of the transmitter is 18dBm and the output 1dB compression point is 15dBm. The performance of the transmitter is summarized in Figure 2, and it achieves better than 4.5% EVM at maximum power output. The peak power added efficiency of the output stage is 20% at lower data rates, dropping to roughly 5% at 54 Mbps.

The PLL synthesizer in Figure 4, generates a ~2GHz signal for the IF chains, and a ~4GHz signal for the RF chains. An offset loop approach is employed to minimize the overall phase noise. A Colpitts differential crystal oscillator (XO) operates at 40MHz. The 160MHz required by the offset mixer in the

IF PLL and the BBIC clock is generated by series multiply-by-2 circuits. Each multiplier consists of a rectifier followed by amplifier stages that also provide a filtering function, and the measured multiplier noise floor is -135dBc/Hz.

The VCO is a differential, cross-coupled design. The tank circuit consists of varactors in parallel with an on-chip differential inductor. There are two sets of varactors that support a coarse/fine tuning scheme in the PLL, with the coarse-tuning varactor bias set during a frequency calibration at power-up. The IF VCO frequency is divided down from ~2GHz for offset mixing with a signal from the XO chain to produce a 40 MHz output. This is compared to the 40MHz reference frequency with a phase-frequency detector. The RF VCO frequency is divided down from ~4GHz to ~2GHz for offset mixing with ~2GHz from the IF PLL, which is then divided to a reference frequency of 2.5MHz, 5MHz, or 10MHz by a CMOS integer-N divider. The 40MHz XO signal is divided down by a /4 /8 /16 selectable CMOS divider to the above frequencies for the compare. The synthesizer performance is summarized in Figure 2, and the measured phase noise is shown in Figure 5. The total integrated phase noise at the synthesizer output from 1kHz to 10MHz is

1.0 degree rms, which is sufficient for 64QAM operation. A transmit constellation is shown in Figure 6.

The chip was fabricated in the Jazz Semiconductor 0.18 um SiGe BiCMOS process, and a die photograph appears in Figure 7. The circuit occupies 25 mm^2.

References:

[1] M. Okada, et. al, "Pre-DFT Combining Space Diversity Assisted COFDM," IEEE Transactions on Vehicular Technology, vol. 50, no. 2, March 2001, pp. 487-496.

[2] D. Su, et. al., "A 5 GHz CMOS Transceiver for 802.11a Wireless LAN," ISSCC Digest of Technical Papers, Paper 5.4, Feb. 2002.