AM1-S100 Frequency Synthesizer

Part II

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Synopsis

The S100 frequency synthesizer is the first frequency synthesizer in a planned progression of synthesis projects on the drawing board. Although this synthesizer only provides core frequency coverage from 10 MHz through 1344 MHz, it also provides a wide compliment of precision reference outputs at 10 MHz and 100 MHz which can be used across my entire electronics laboratory as a master coherent source as needed.

The embedded 10 MHz precision frequency reference is based upon a 10 MHz OCXO which is frequency-locked to the 1 PPS output of a GPS receiver. The 100 MHz precision reference is created using a separate high quality 100 MHz VCXO which is phase-locked to the 10 MHz OCXO.

The tunable frequency source output is further conditioned using a bank of harmonic rejection filters and digital ALC for precise output level control.

One of the more significant aspects of this installment is the new methodology presented in §3.1.1 for varactor-tuned filter designs. Without this new design approach, the diode capacitance ratios would have needed to be greater than 8:1 to achieve octave-band tuning. Such diodes are generally difficult to obtain while also leading to higher intermodulation distortion terms than desired. The new design approach only requires tuning capacitance ratios on the order of 4.5:1.

This project installment is Part II of the series[1].

[1] Part I, released 29 Oct. 2017 as U24872_AM1_S100_Synthesizer.pdf.

1 Introduction

A revised high-level block diagram of the S100's frequency synthesis portion is shown in Figure 3. There are multiple implementation differences between the project plan now and the original diagram shown in [1]. The most significant change is the decision to augment the Arduino Mega2560 with a flat-panel Vaio computer.

The decision to include the Vaio computer was motivated by:

- Better visibility/readability than using the 4-D Systems LCD originally planned for
- Itemization of the many I/O and control of functional areas made easier
- The desire to use the GPS receiver in an expanded role to assess OCXO frequency accuracy over time with the ability to display statistics of interest
- Realization that incorporation of the Vaio computer would greatly ease control software development along with hardware integration

Perhaps somewhat premature, a prototype graphical user interface (GUI) for the Vaio is already underway as shown in Figure 1. The GUI is being developed using C# and builds upon a number of other projects I have done in the past using this software. A second graphic of the GUI being hosted on the Vaio computer is shown in Figure 2. The RF board (which is the subject of this development effort) has not been built and assembled yet. Each of the functional buttons have separate windows which pop-up with the associated information and additional control features.

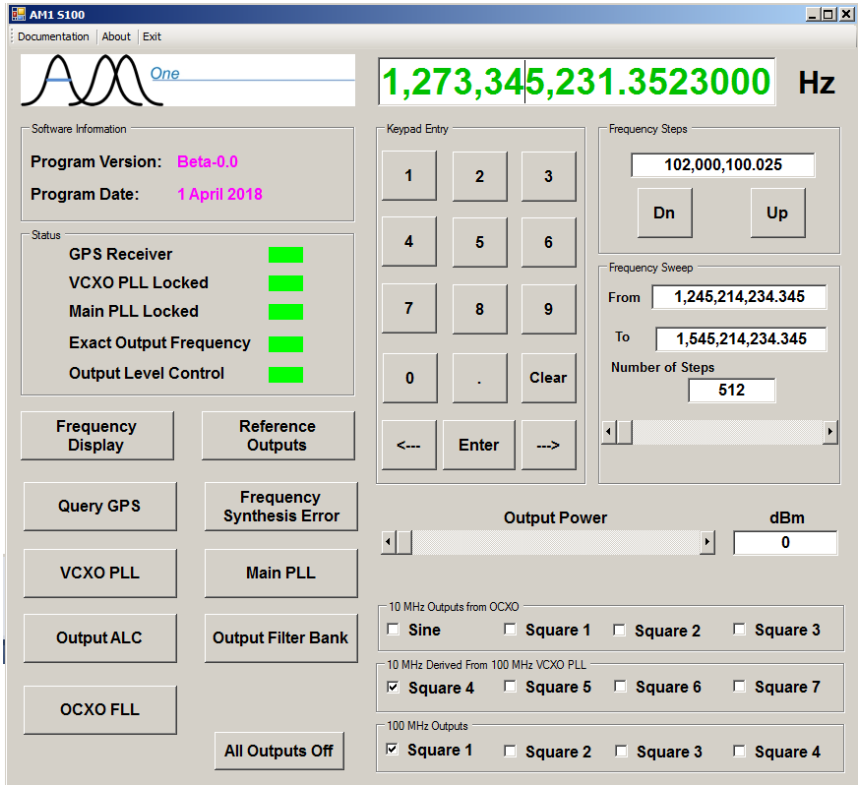


Figure 1 Development of the Vaio-based graphical user interface is underway

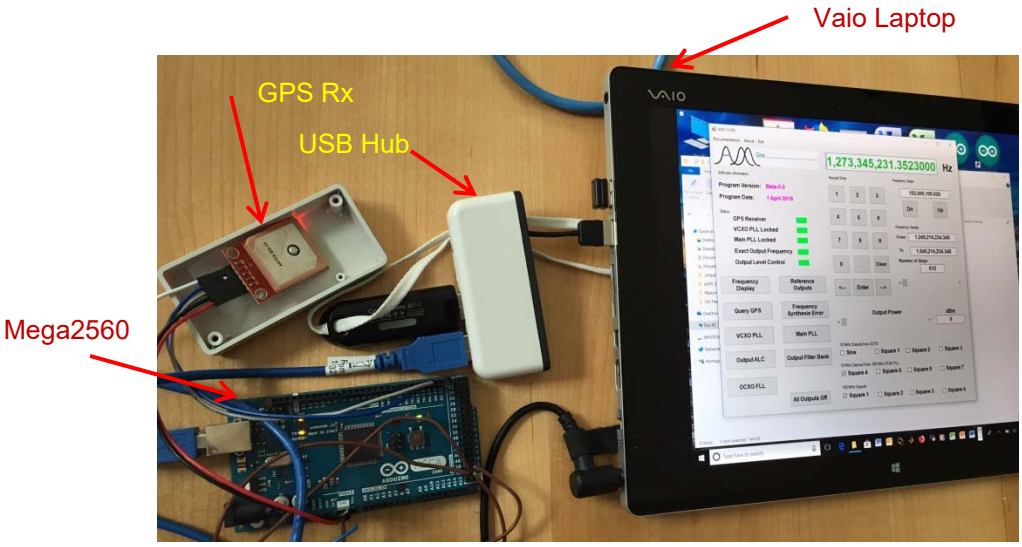


Figure 2 Vaio laptop computer along with USB expansion port, Arduino Mega2560, and Antek GPS receiver. In the final form-factor, the GPS receiver will be buttoned up as an external module and the Mega2560 board will be integrated within a separate housing along with the RF circuit board which has not been built yet.

Figure 3 is followed by Figure 4 which is devoted to the output signal conditioning portion of the circuitry and has been similarly revised.

The design discussion that follows is broken up into two major sections: (i) Frequency Synthesis (development of the digital hardware needed to support the *frequency-locked loop* operation of the 10 MHz OCXO and GPS receiver) and (ii) RF filtering. The RF filtering topic again took center-stage in this installment in that the original design work on tunable RF filters [2 – 5] still presented tuning-range issues with off-the-shelf low-cost varactors as mentioned in the Synopsis. In most cases, octave tuning range of the original filter designs would have required capacitance-change ratios[2] on the order of 8 to 10; ratios that are not generally available without incurring substantial intermodulation degradation at the high capacitance end of the tuning curves. This problem was circumvented using the new design approach described in §3.1 which achieves octave filter tuning range while typically requiring capacitance ratios less than 4.5:1.

2 Frequency Synthesis

The frequency synthesis portion of the S100 is shown in Figure 3 as already mentioned. Most of the circuitry is devoted to the creation of pristine 10 MHz and 100 MHz reference signals whereas the tunable synthesis portion is performed by the LMX2571 device.

[2] Since only capacitance changes are used, octave tuning range requires a minimum of 4:1 capacitance change. In order to keep the filter-Q constant across the full tuning range, an additional 2:1 capacitance change is needed thereby combining to a minimum capacitance change ratio of 8:1.

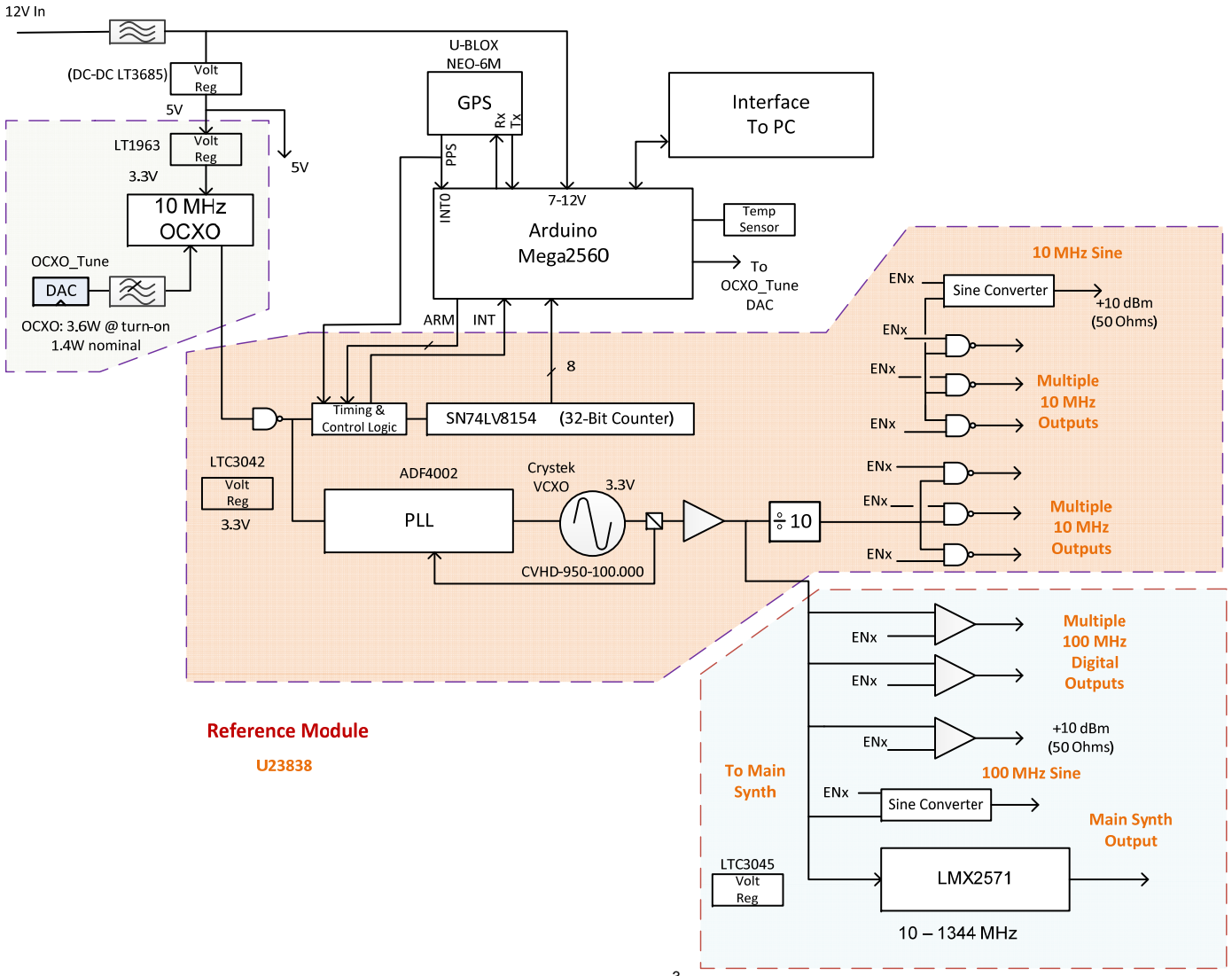


Figure 3 Revised top-level block diagram of the frequency synthesis portion[3] of the S100

[3] From U23838 AM1-S100 Synthesizer.vsd.

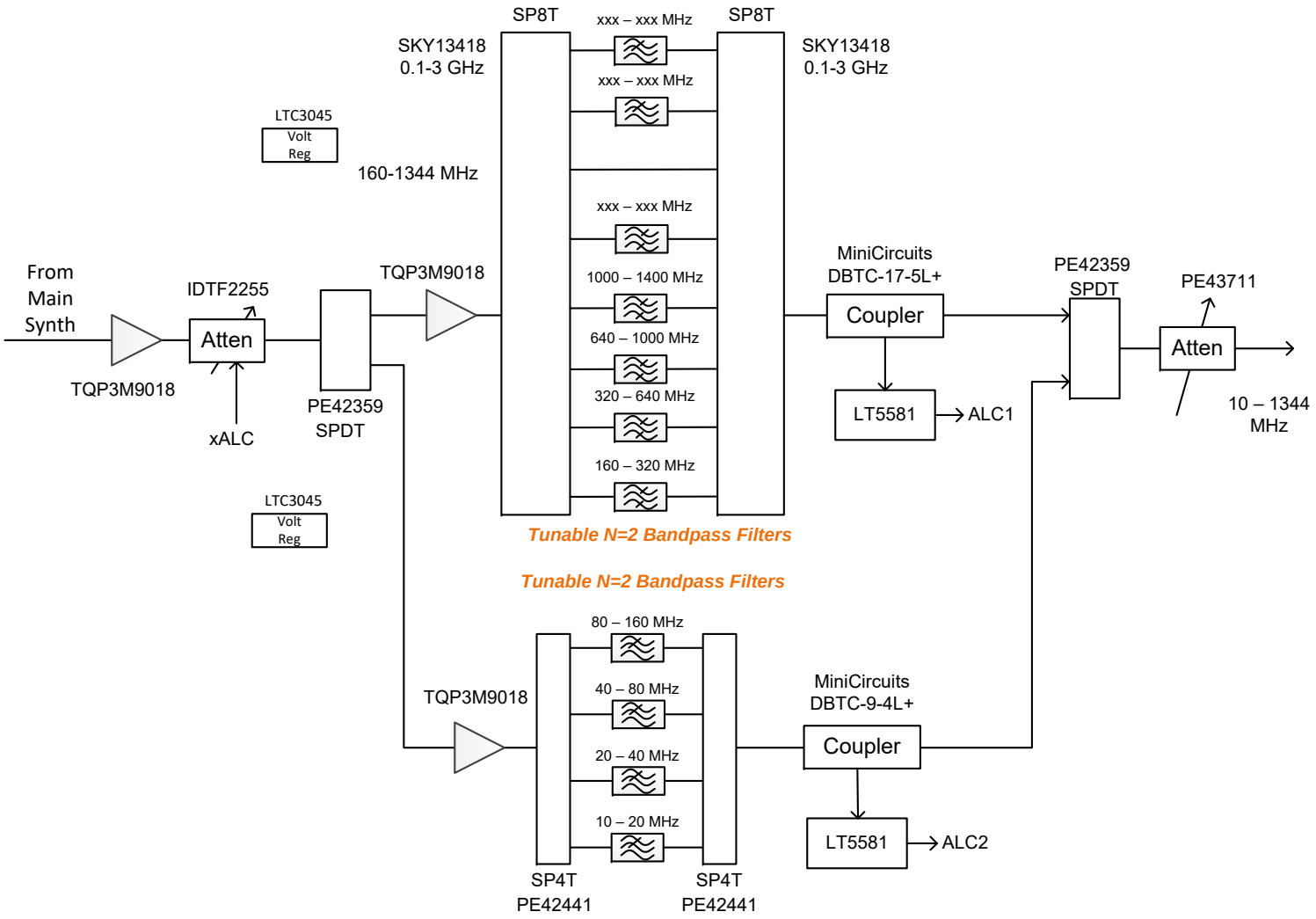


Figure 4 Revised top-level block diagram of the signal conditioning portion[4] of the S100

[4] From U23838 AM1-S100 Synthesizer.vsd.

2.1 10 MHz Reference Creation

Creation of the 10 MHz reference signal is done using a precision 10 MHz OCXO which is frequency-locked to a precision GPS-derived one pulse per second (1 PPS) output whenever the GPS signal is available. Each portion of this circuitry is discussed separately.

2.1.1 10 MHz OCXO

The adopted oven-controlled crystal oscillator (OCXO) is the AOCJY-10.000MHz device from Abracon Corporation. The device delivers ±5 ppb frequency stability over the temperature range of 0° to 50° Centigrade. Over ten years, the device long-term aging is guaranteed to be better than ±500 ppb. The frequency pulling range is a minimum of ±700 ppb.

Phase noise performance of the AOCJY-10.000MHz device is quite good as evidenced by Table 1. However, frequency accuracy/drift for frequency offsets less than roughly 0.1 Hz will be maintained via GPS discipline as discussed in §2.1.2. For frequency offsets greater than about 100 Hz, the phase noise performance of the 100 MHz VCXO[5] shown in Figure 5 will be better than that achievable using the 10 MHz OCXO thereby advocating a VCXO PLL closed-loop bandwidth on the order of 100 Hz.

Table 1 10 MHz OCXO Phase Noise Performance

Frequency Offset, Hz	Phase Noise, dBc/Hz	Ideal Extrapolation to 100 MHz Center Frequency, dBc/Hz	CVHD-950 100 MHz VCXO, dBc/Hz
1	–90	–70	
10	–120	–100	–86
100	–135	–115	–119
1,000	–145	–125	–143
10,000	–150	–130	–157
100,000	–150	–130	–165
1,000,000	–150	–130	–169

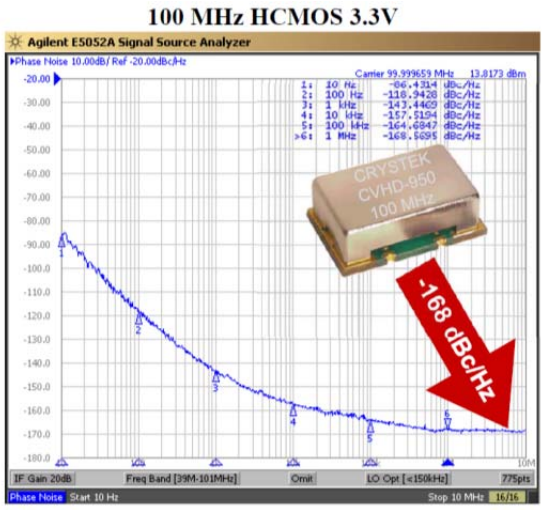


Figure 5 Phase noise performance of the 100 MHz CVHD-950 VCXO from Crystek (open-loop)

[5] See Figure 5.

2.1.2 1 PPS Using U-BLOX GPS Receiver

The U-BLOX NEO-6M GPS receiver conveniently outputs a precision one-pulse-per-second (PPS) signal that can be used to discipline the OCXO's long-term frequency behavior. A frequency-locked control loop implemented through the Mega2560 Arduino microprocessor is used to perform this task. The main elements of this approach are shown in Figure 3 where the imperfect 10 MHz OCXO output zero-crossings are synchronously counted for up to 15 contiguous seconds as governed by the PPS signal and additional control logic. In principle, this permits the frequency error to be tracked to better than $\pm 1/(15 \times 1e7) = \pm 6.7$ ppb if temperature-related frequency variations are adequately slow.

Two SN74HC4040's (12-bit asynchronous counters) operating in cascade would make it possible to count zero-crossings for one second unambiguously since $10^7 < 2^{24}$, but longer counting intervals (e.g., 2 seconds) will cause the cascaded counters to overflow. Since the frequency error cannot be worse than approximately 1 ppm, however, the resulting ambiguity can be easily dealt with. For example, assume that the OCXO's output zero-crossings are counted for 8 seconds. In the case of no frequency error, the count would be mod(8 x 10,000,000, 2^{24}) = 12,891,136. If on the other hand the OCXO's frequency error is +1 ppm, the count would be mod(8 x 10,000,010, 2^{24}) = 12,891,216 and therefore 80 counts too high and this information can be subsequently used to correct the OCXO's frequency slowly over time. The ideal count value versus measurement time interval is summarized in Table 2. Modulo arithmetic can be used with a smaller count- modulus like 2^{16} as also shown in Table 2 or even smaller. The 24-bit and 32-bit counters could be helpful, however, in the prototype verification effort with its unambiguous count for one second.

Since the SN74LV8154 can provide the full 32-bit counter function in a single integrated device, this choice has been adopted for the AM1_S100.

Table 2 Count Values Versus Time Measurement Interval (Ideal)

Measurement Time, sec	32-Bit Counter (Ideal)	Alternative 24-Bit Counter Value (Ideal)	Alternative 16-Bit Counter Value (Ideal)
1	10,000,000	12,891,136	38,528
2	20,000,000	3,222,784	11,520
4	40,000,000	6,445,568	23,040
8	80,000,000	12,891,136	46,080
10	100,000,000	16,113,920	57,600
12	120,000,000	2,559,488	3,584
15	150,000,000	15,782,272	53,632

2.1.3 Frequency Locking OCXO with 1 PPS

The frequency measurement error associated with a single measurement is directly related to the measurement time interval as suggested by Table 3. Additional provisions can be made within the control loop to attain considerably better precision for a given measurement interval, however. In the case of a one-second measurement interval, the observed counts could be $10{,}000{,}000 \pm \varepsilon$ where $\varepsilon \in \{-1, 0, 1\}$ and sufficient loop intelligence subsequently included to *ride* the transition between $\varepsilon = -1$ and $\varepsilon = 0$ where the probability of $\varepsilon = 0$ is maintained in the 90% range and noise-averaging used to track the exact transition point.

More details about the actual frequency-locked loop closed-loop algorithm will be provided in Part III.

Table 3 One-Shot Frequency Error Measurement Error Versus Measurement Time

Measurement Time, sec	Ideal Counts Accumulated	Frequency Estimation Error, ppb
1	1e7	±100
2	2e7	±50
4	4e7	±25
8	8e7	±12.5
15	1.5e8	±0.6.67

In order to obtain a precise frequency measurement, the OCXO's output zero-crossings must be counted between contiguous PPS positive-going edges. The circuitry shown in Figure 6 is used to create the gated 10 MHz clock needed for this purpose. Circuit operation is as follows:

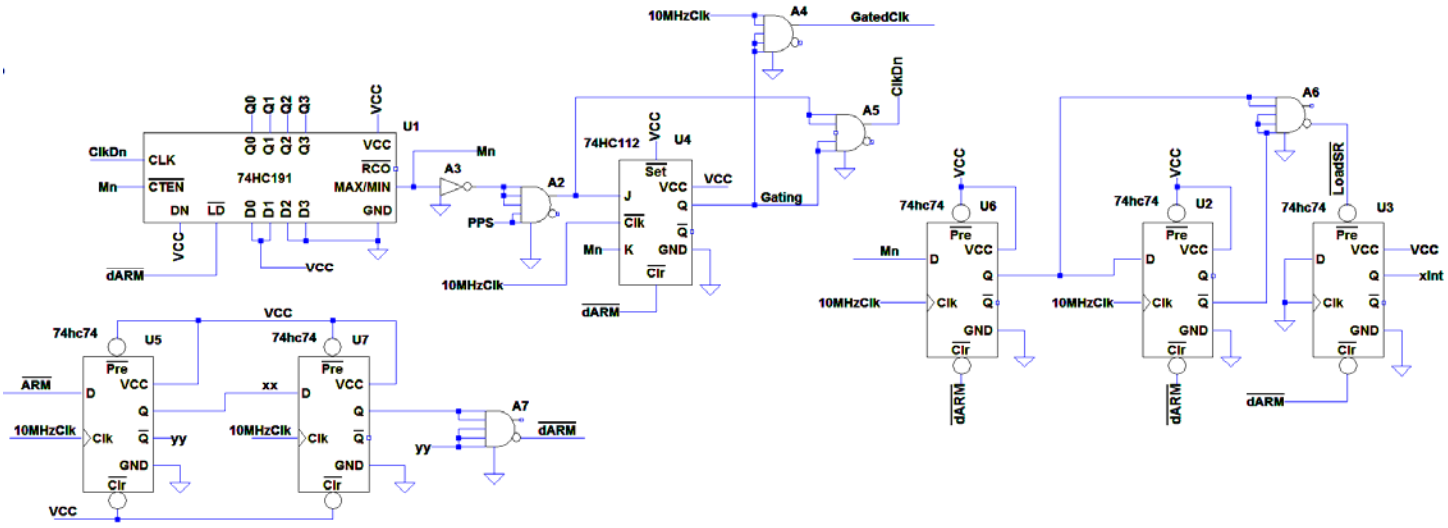


Figure 6 Creation of gated 10 MHz clock for frequency measurement metric[6] in LTSpice

1. A frequency measurement is initiated by issuing a $\overline{ARM}$ (active low) strobe with a binary value *M* (1–15) present on the D3–D0 input lines to the U1 down-counter. The time duration for the measurement is given by $(M-1)$ seconds. The $\overline{ARM}$ loading action is synchronized with the leading-edge of the *10MHzClk* signal to create $\overline{dARM}$ which initializes the HC191 down-counter and resets other flip-flops in the circuit.
2. The PPS signal is asynchronous to the 10 MHz OCXO reference oscillator since it originates from the U-BLOX GPS receiver. In order to avoid meta-stability issues between the 10 MHz clock and the PPS signal, a synchronous version of the PPS signal is created with U4 on the falling edge of the 10 MHz clock. The U4-Q output remains high (thereby allowing 10 MHz clocking to pass through A4 to the accumulation counters) until the HC191 counter reaches a count of zero and issues a true MAX/MIN output signal. This is a direct result of the final PPS signal's leading-edge which creates the ClkDn signal that toggles the HC191's count-value. Although the HC191 count-value is triggered by the unsynchronized PPS signal, the GatedClk signal is not disabled until the HC191 Mn signal synchronously resets the U4 JK-flip-flop.

[6] LTSpice file: AM1_S100_Freq_Meter.asc.

3. Since the GatedClk signal is framed by the U4 JK-flip-flop whose state transitions are tied to the negative-going edges of the $10MHzClk$ signal but subsequent counter action is always based upon positive-going edges of the same signal, counting errors associated meta-stability or race conditions should be absent.
4. The $GatedClk$ signal are accumulated in the 32-bit counter function provided by a SN SN74LV8154.
5. Once the measurement time interval has been completed, signal *Mn* is set true. A synchronized version of *Mn* is used to set flip-flop U3 true which serves as an interrupt signal to the Mega2560.
6. Once the Mega2560 recognizes the interrupt, it issues the needed sequence of shift/read operations to read back the counter value to the processor from the SN74LV8154.

A few graphical results associated with operation of the Figure 6 circuitry follow. In Figure 7, issuance of the possibly long $\overline{ARM}$ signal is synchronized with the $10MHzClk$ signal, and used to create a one-cycle length synchronized load-strobe $\overline{dARM}$ as shown.

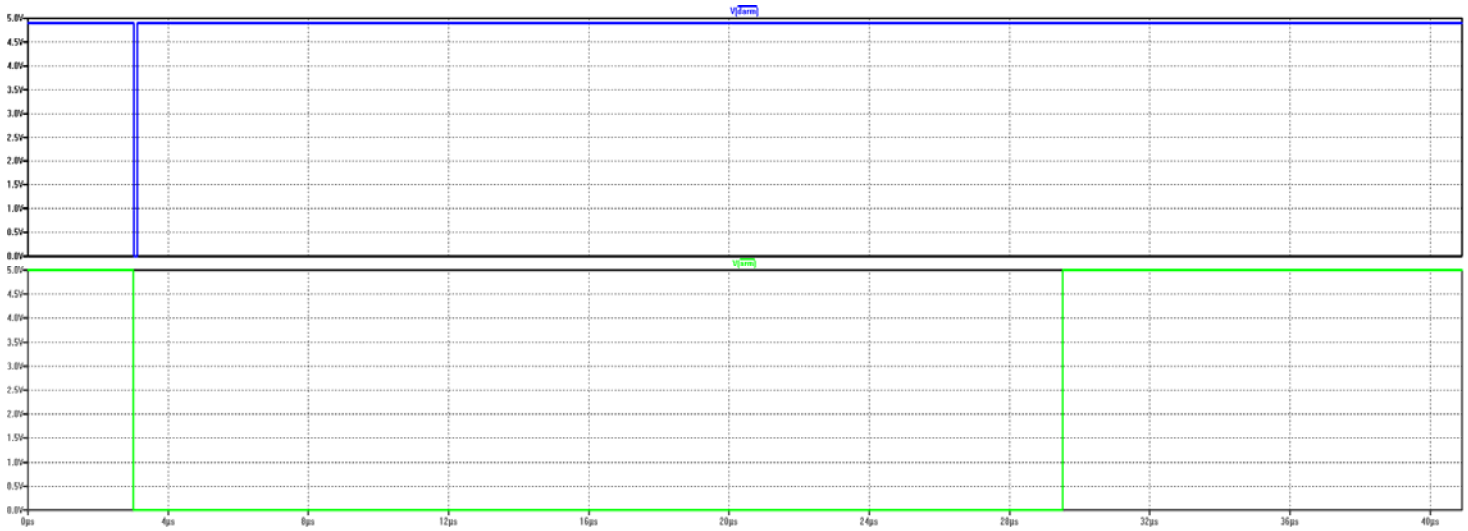


Figure 7 Flip-flops U5 and U7 working with gate A7 initialize the down-counter U1 and the other flip-flops in a synchronous manner. Synchronization is done with the leading edge of the 10 MHz clock and is only one clock-cycle wide regardless of the width of the initiating strobe signal $\overline{ARM}$.

Creation of the pristine *GatedClk* signal (10 MHz) is shown in Figure 8. The *GatedClk* is active for the number of contiguous 1-second intervals initially programmed into the 74HC191 counter. At the end of the measurement sequence, the 74HC191's *Mn* signal becomes High which causes the *Gating* signal to be synchronously removed and the Mega2560 to be interrupted as shown in Figure 9 with additional detail shown in Figure 10.

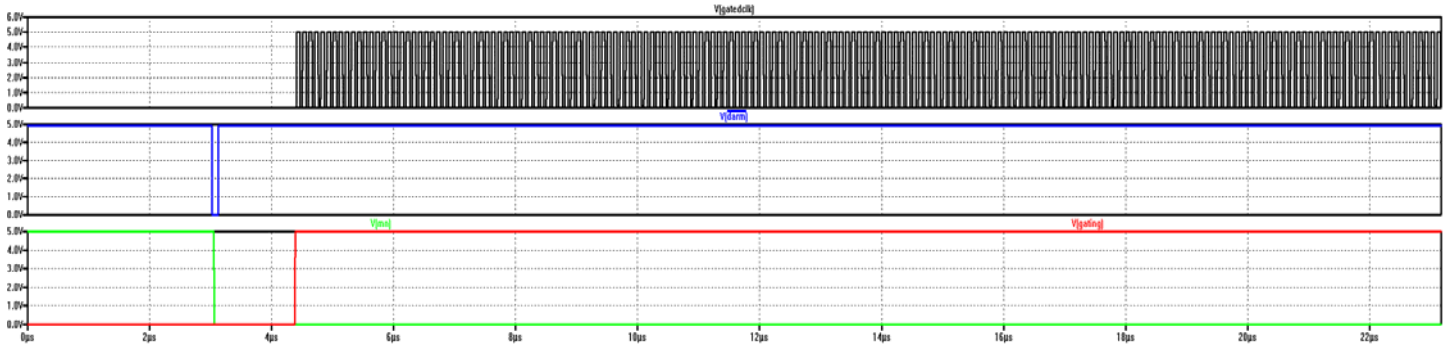


Figure 8 Issuance of the $\overline{ARM}$ strobe sets the measurement sequence into action, beginning with loading of the HC191 down-counter which causes signal *Mn* to go Low and the Gating signal to be synchronously clocked High. The pristine GatedClk signal is counted during the measurement time using the SN74LV8154.

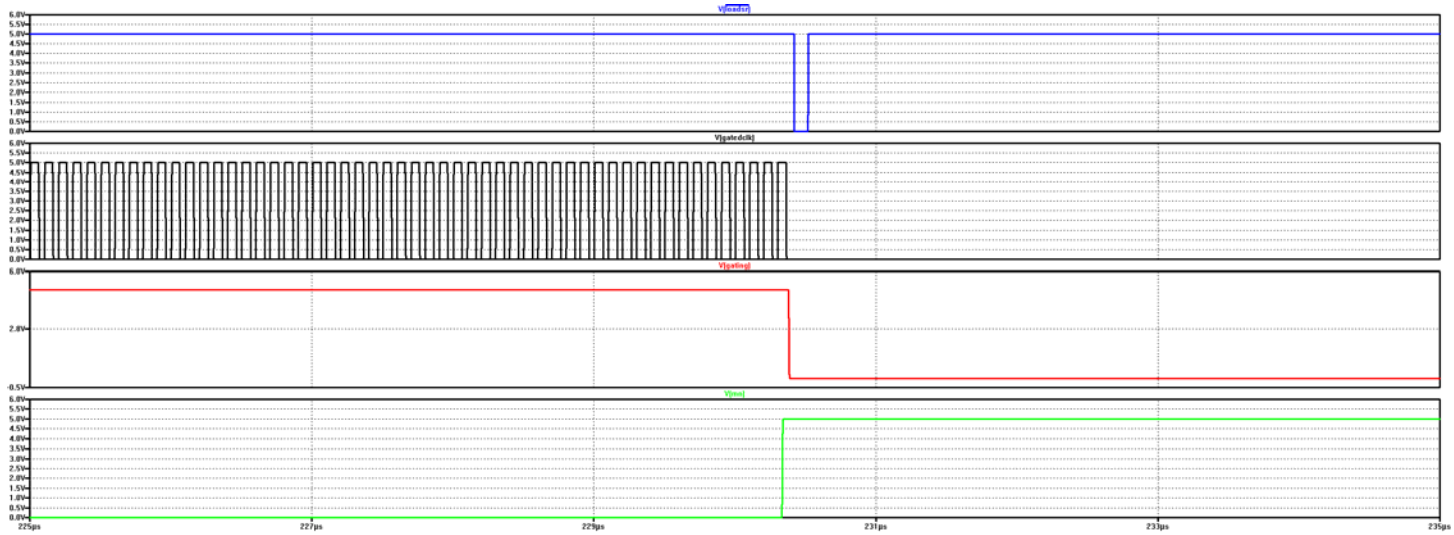


Figure 9 Completion of the measurement sequence where the HC191's *Mn* signal synchronously resets the *Gating* signal which invokes the $\overline{LoadSR}$ signal and interrupts the Mega2560

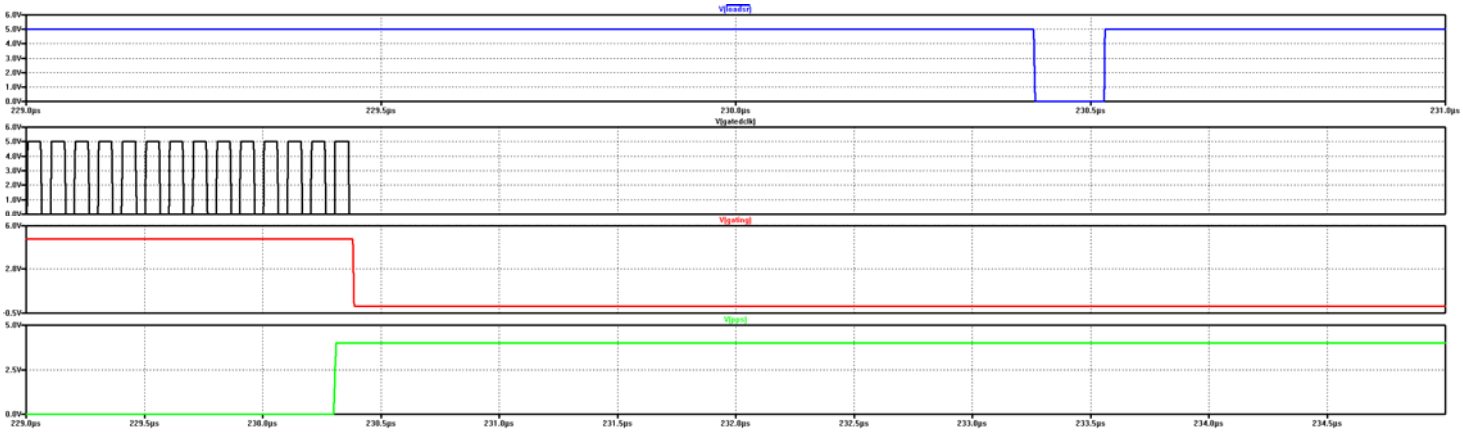


Figure 10 Additional close-up of Figure 9 showing that the *Gating* signal is removed with the first falling edge of *10MHzClk* following the last PPS pulse occurrence, and the absence of any additional *GatedClk* pulses thereafter

2.1.4 10 MHz Reference Sine Wave Output

The 10 MHz output sine wave can be created in a variety of ways. The two methods considered here are to use (i) a heavily filtered 10 MHz square wave or (ii) a heavily filtered 10 MHz triangle wave. The latter approach has some initial appeal because it would inherently lead to lower output harmonics.

The complex Fourier coefficients of a periodic waveform $v(t)$ with period T_o can be computed as

$$c_n = a_n - jb_n = \frac{2}{T_o}\int_0^{T_o} v(t)\exp\left(-j\frac{2\pi n}{T_o}t\right)dt \tag{1}$$

For a mean-zero square-wave signal having amplitude ±*A*, $c_n = -j4A/(n\pi)$ for odd-integer values greater than zero but otherwise zero for all even-integer values. In other words,

$$v_{square}(t) = \frac{4A}{\pi}\sum_{m=0}^{\infty}\frac{1}{2m+1}\sin\left[(2m+1)n\frac{t}{T_o}\right] \tag{2}$$

Similarly, for a mean-zero triangle-wave signal having amplitude ±*A*, $c_n = 8A/(\pi n)^2$ for positive-*n* odd integers but otherwise zero. In other words,

$$v_{triangle}(t) = \frac{8A}{\pi^2}\sum_{m=0}^{\infty}\frac{1}{(2m+1)^2}\cos\left[(2m+1)n\frac{t}{T_o}\right] \tag{3}$$

Comparing (2) and (3) for the same peak-value *A* reveals that the fundamental sine wave component is 1.571 times larger for the square-wave signal than for the triangular-wave signal. Since it is easier to create square-wave signals than triangular-wave signals, it is preferable to create the sine wave output using a heavily filtered square-wave signal. This methodology is easily extended for the 100 MHz case as well which would not be the case for the triangular-wave approach.

A circuit for creation of the 10 MHz sine wave is shown in Figure 11 with the simulated output shown in Figure 12.

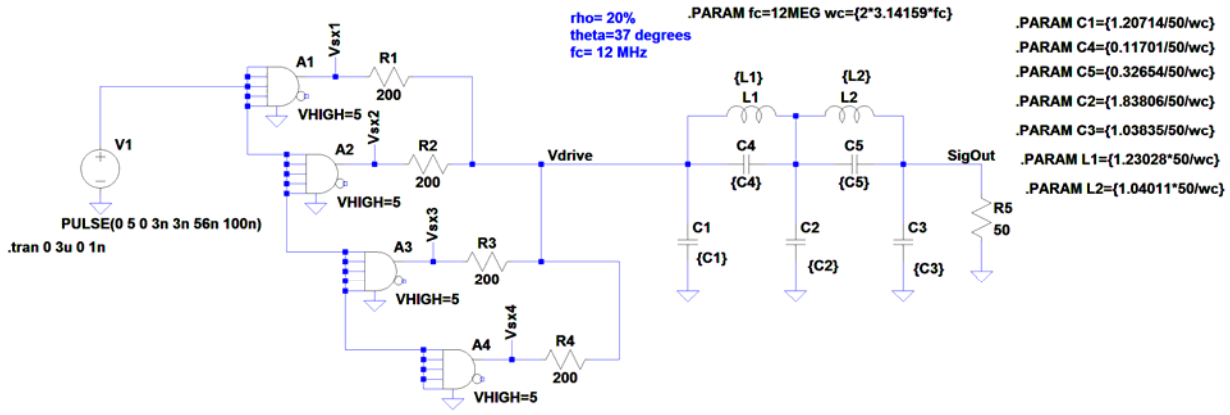


Figure 11 10 MHz sine wave signal creation using heavily filtered HCMOS square-wave output. { C_1, C_2, C_3, C_4, C_5 }= { 320 pF, 488 pF, 275 pF, 31 pF, 87 pF} and {L_1, L_2 }= { 816 nH, 690 nH }

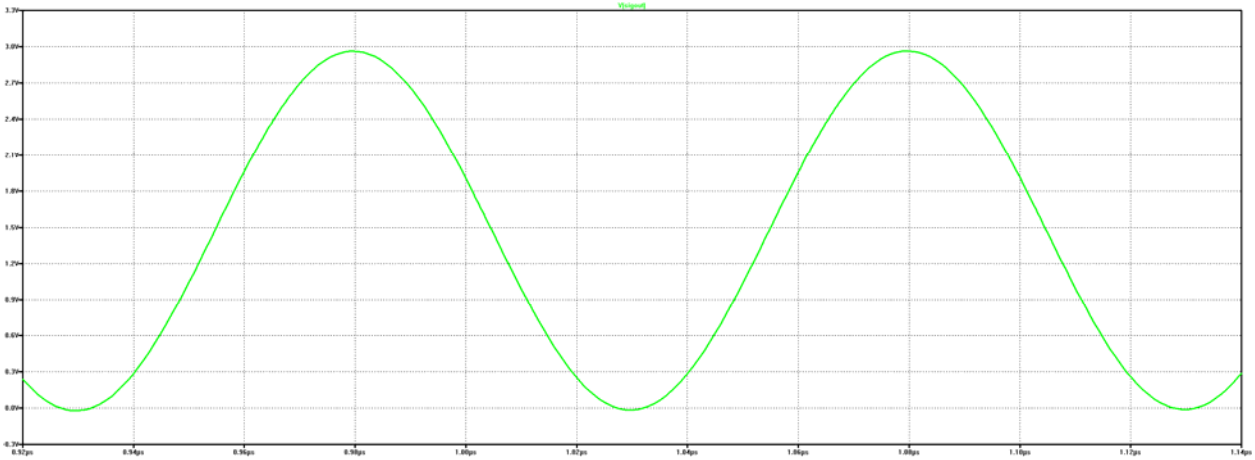


Figure 12 10 MHz sine wave signal created in Figure 11

2.2 100 MHz Reference Creation

The precision 100 MHz output is created by phase-locking a low-noise 100 MHz VCXO to the 10 MHz precision OCXO. The OCXO (which is frequency-locked to the GPS receiver) provides outstanding long-term frequency stability whereas the VCXO provides exceptionally good phase noise performance for frequency offsets greater than about 100 Hz as shown in Figure 13. The phase-locked loop is based upon using the Analog Devices ADF4002 PLL with a 10 MHz phase comparison frequency, natural frequency of 20 Hz, and damping factor of 1.0 with a CVHD-950 VCXO. The loop filter details are provided in Figure 15 in conjunction with Table 4. Phase noise contributors at the PLL's output are detailed in Figure 14.

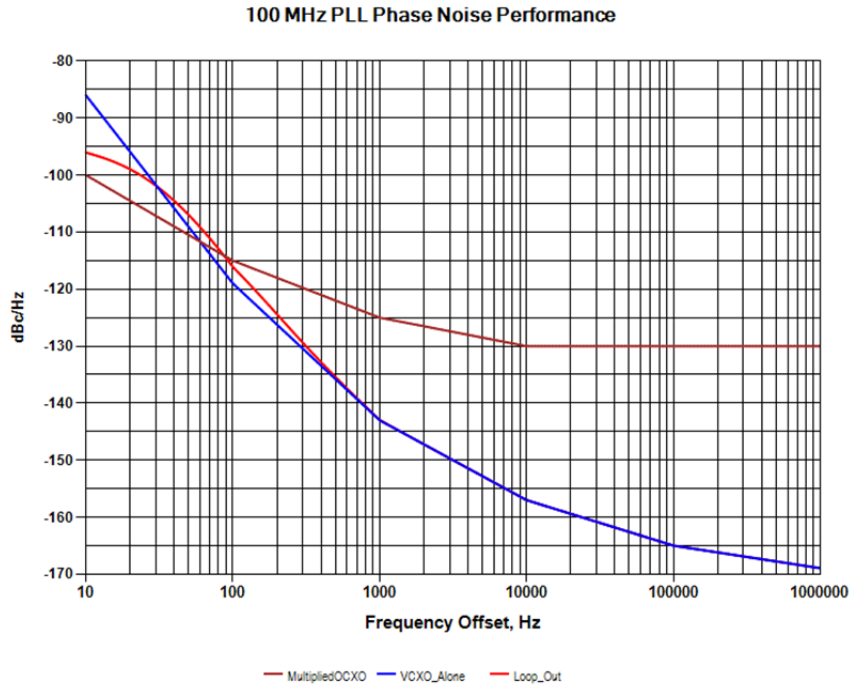


Figure 13 Phase noise performance of 10 MHz OCXO (perfectly multiplied to 100 MHz), 100 MHz VCXO, and 100 MHz PLL compared[7]

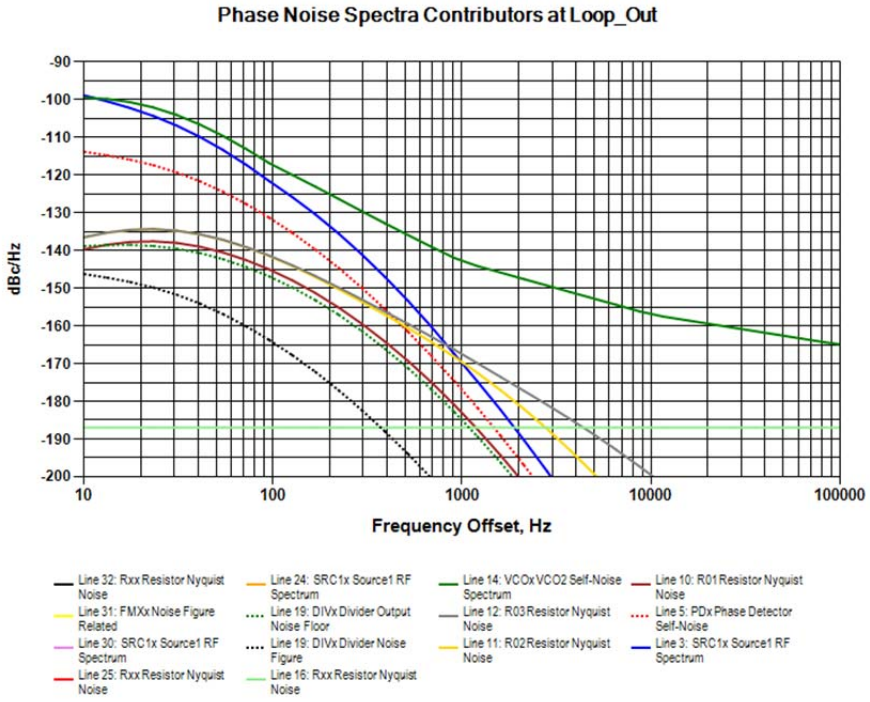


Figure 14 Phase noise contributions at PLL output with reference designators shown in Figure 15

[7] 100MHzPLL_Trial_01.prm.

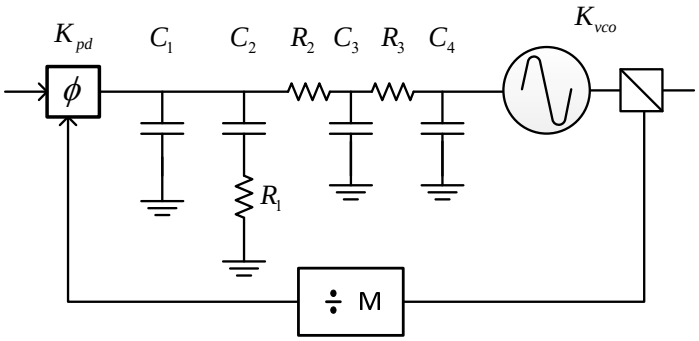


Figure 15 100 MHz PLL loop filter details

Table 4 100 MHz PLL Loop Filter Details Associated With Figure 15

Component	Value	Comments
C_1	1 μF	Ceramic
C_2	33 μF	"
C_3	0.1 μF	"
C_4	0.1 μF	"
R_1	510 Ω	
R_2	1 k Ω	
R_3	1 k Ω	
PLL	ADF4002	I_{cp} = 2 mA, ÷R= 1, ÷M= 10
VCXO	Crystek CVHD-950	K_{vco} = 2500 Hz/V

2.2.1 100 MHz Reference Sine Wave Output

The 100 MHz since wave output is created in the same way as the 10 MHz since wave was created, using a heavily filtered square wave.

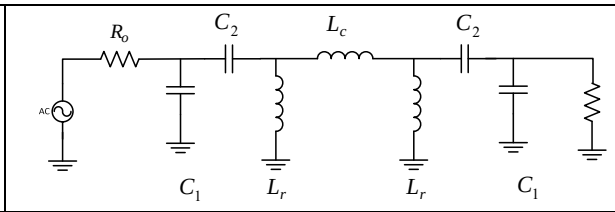
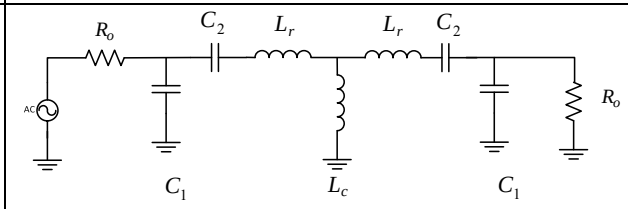
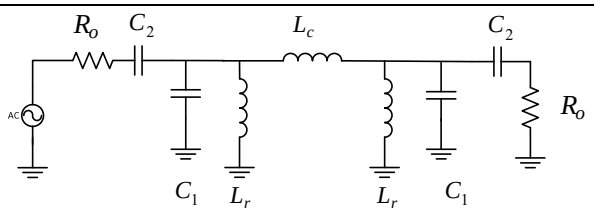
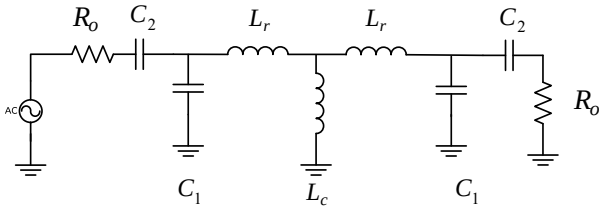
3 Output Signal Conditioning

The output signal conditioning consists of automatic level control combined with tunable bandpass filtering to suppress unwanted harmonics and spurious components.

3.1 Filtering Approach

I have previously written fairly extensively about tunable bandpass filters suitable for this application [2, 3, 4]. A very abbreviated version of the material was also recently published [5]. The ultimate focus of this material was the use of 2nd order inductively-coupled filters using tapped input and output variable capacitances. The primary configurations are repeated here in Table 5 from [3]. A representative design example[8] follows here with some of the results shown in Figure 16 and Figure 17.

Table 5 Primary 2nd Order Bandpass Filter Configurations Employing Tapped Capacitances

A		$R_o < R_{internal}$ Inductor-pi
B		$R_o < R_{internal}$ Inductor-tee
C		$R_o > R_{internal}$ Inductor-pi
D		$R_o > R_{internal}$ Inductor-tee

Although this design approach is optimal in several respects, trial and error with a fairly wide range of different filter parameters always results in a maximum-to-minimum capacitance ratios for C_1 and C_2 which is appreciably larger than 4 in order to achieve octave-band tuning (on the order of 8 to 10 for octave coverage). This becomes problematic because of varactor diode limitations. In the design example

[8] Using u24160_filter_design_aid.m.

that follows, the needed capacitance ratio is almost 8:1 for capacitor C_1 which is challenging to implement in real hardware.

Aside from the final filter design details, the major emphasis of this section is the discovery that the inclusion of two extra inductors denoted by L_m (see Figure 18 or Figure 24 depending upon filter configuration) makes it possible to reduce the tuning capacitance ratio from roughly 8:1 (or worse) down to typically 4:1 for octave coverage. This makes the filter designs implementable using reasonable varactor diodes.

```
---------------------------------
      Design Parameters
---------------------------------
>>> Low frequency tuning limit 10.000000, MHz
>>> High frequency tuning limit 20.000000, MHz
>>> Geometric center frequency 14.142136, MHz
>>> Internal filter impedance at geometric center frequency 15.000000
>>> Bandwidth at geometric center frequency 1.000000, MHz
>>> gamma 1.500000

Inductance Tee:                 Inductance Pi:
        Lr (nH) =    3207.37688        Lr(nH) =     3544.99549
        Lc (nH) =     168.80931        Lc(nH) =    67354.91439

Freq, MHz     C1, pF      C2, pF
-----------------------------------------
10.00          43.39       31.82
14.14          16.98       20.61
20.00           5.44       13.35
```

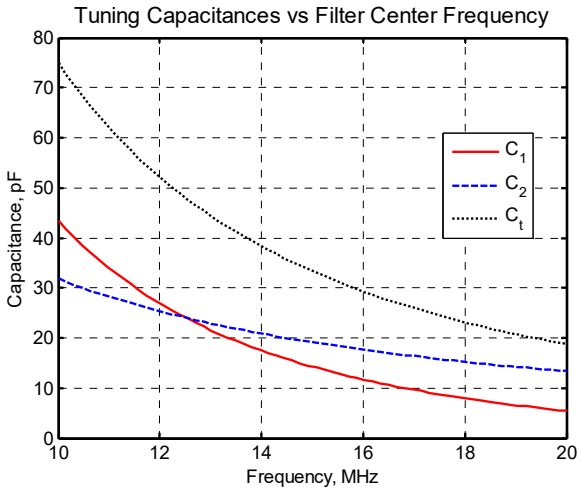


Figure 16 Ideal tuning capacitance values for the filter (Configuration A or B from Table 5)

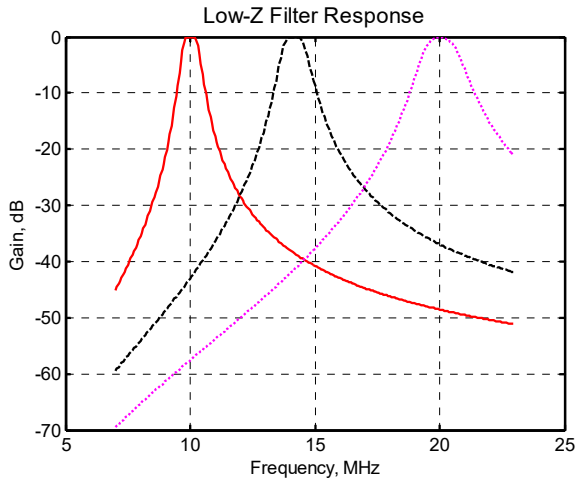


Figure 17 Idealized frequency responses associated with Figure 16

3.1.1 Step-Up Impedance Filter Configuration

An earlier design approach is worthy of design consideration if it can provide a means for reduced capacitance ratios. The technique which will be employed to reduce the maximum-to-minimum capacitance range is to divide and conquer the problem. The core filter will remain almost unchanged compared to the development work just cited, but it turns out that including the correct value of series inductance L_m at the input and output ports can ease the needed tuning capacitance ratio substantially. Ideally, the required capacitance ratio is no worse than $\left(f_{\max} / f_{\min} \right)^2$ since only capacitances are being tuned, and the L_m inductor additions come very close to achieving that limit.

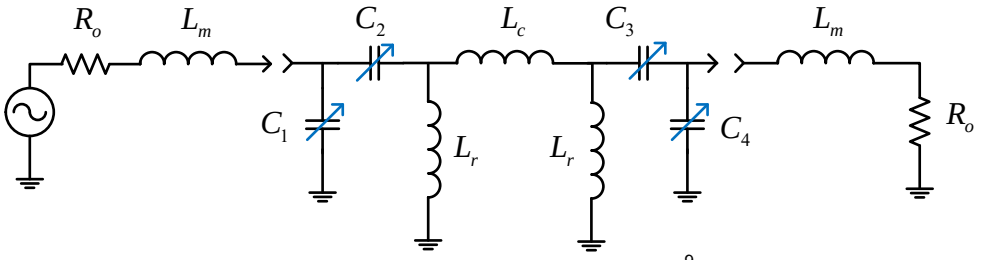


Figure 18 Divide and conquer approach to reduce capacitance ratios[9]

To get started, consider the simple series R-L circuit shown in Figure 19. In order for the filter to be constant-Q in nature, ideally the port impedance values vary as

$$R(f) = R_x \frac{f}{f_1} \tag{4}$$

over the frequency range spanning from f_1 to f_2. In this equation, R_x is an arbitrary scaling impedance value and frequency f_1 is the lowest tuning frequency of interest.

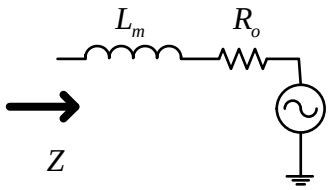


Figure 19 Inserting an inductance L_m in series with the filter terminations increases the apparent (real) part of the termination with frequency

The series circuit in Figure 19 can be transformed to its Norton equivalent as shown in Figure 20 where

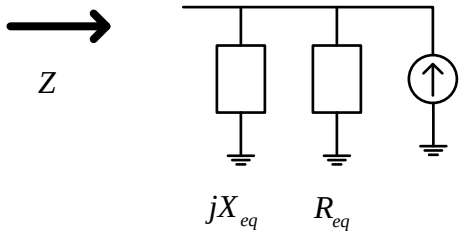


Figure 20 Norton equivalent of Figure 19

[9] From U25111 Tunable LC BPFs.vsd.

$$R_{eq}(\omega) = R_o + \frac{(\omega L_m)^2}{R_o} \tag{5}$$

$$X_{eq}(\omega) = \omega L_m + \frac{R_o^2}{\omega L_m} \tag{6}$$

As evidenced by (5), this technique can be used to increase the equivalent port resistance with frequency rather than solely relying upon the capacitance ratio C_1 / C_2 as done in the configurations shown in Table 5. This approach introduces additional (positive) reactance as given by (6), but it turns out that this can be easily absorbed in Figure 18 with slight modifications to the shunt port capacitances C_1 and C_4.

Given constant impedance values for R_o and resistance level R_x, an optimal choice for R_x can be found by minimizing the mean-square cost function[10]

$$\Lambda = \int_{\omega_1}^{\omega_2} \left[R_x \frac{\omega}{\omega_1} - R_o - \frac{(\omega L_m)^2}{R_o} \right]^2 d\omega \tag{7}$$

This cost function is convex in nature and is therefore very easy to minimize. The solution for inductor L_m is

$$L_m = \sqrt{\frac{R_x R_o \left(\omega_2^4 - \omega_1^4\right) - \frac{4}{3} R_o^2 \left(\omega_2^3 - \omega_1^3\right) \omega_1}{\frac{4}{5}\left(\omega_2^5 - \omega_1^5\right) \omega_1}} \tag{8}$$

As an example, consider the case where the filter tuning range of interest is 200 MHz to 400 MHz. It can be shown that optimal parameter values are given by R_x = 68.041Ω and L_m = 26.59 nH producing the results shown in Figure 21 for the real portion of the port impedance.

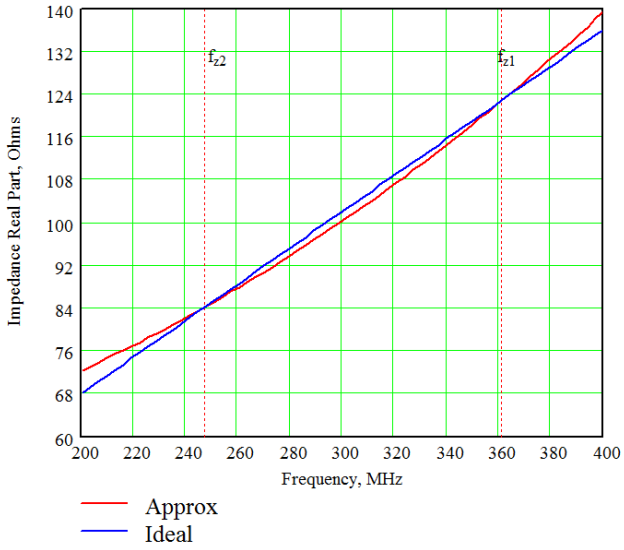


Figure 21 Optimized behavior of the solution versus the ideal characteristic given by (4)

[10] U23020 Tunable Bandpass Filters for Receive.docx, U23028 Capacitively Coupled N=2 BPF.

With R_x and L_m now identified, the filter design proceeds as described in the earlier cited references for the most part. In order to be crystal clear, however, one design example is spelled out here in detail.

The next step in the design process is to pick a filter impedance level R_{geo_core} at the geometric center of the filter's tuning range that results in acceptable filter component values. As such, this is a somewhat iterative process. The tuning capacitors shown in Figure 18 will have to scale the port impedance value (now R_x rather than R_o) up to roughly R_{geo_core} so the associated resistance ratio should not be too large. For this example, $R_{geo\_core} = 300\Omega$ will be chosen.

Next, the coupling inductance value L_c is computed as

$$L_c = \frac{R_{geo\_core}\chi}{\omega_{geo}} \tag{9}$$

where χ is a *fudge-factor* of sorts that is included to easily modify the amount of coupling between the filter's two resonators. It is typically in the range of 0.8 to 1.4. The value adopted here is 1.2.

Next, a filter bandwidth (–3 dB) must be chosen for the filter when it is tuned to its geometric center frequency. In this example, $B_{geo} = 80MHz$ will be chosen. An auxiliary parameter for the tuning capacitance at the geometric center frequency is computed next as

$$C_{tgeo} = \frac{1}{\pi\sqrt{2}R_{geo\_core}B_{geo}} \tag{10}$$

which amounts to 9.378 pF in this example. Several other simple relations follow as[11]

$$\begin{aligned} L_{eff} &= \frac{1}{\omega_{geo}^2 C_{tgeo}} \\ L_r &= \frac{L_{eff}L_c}{L_c - L_{eff}} \\ C_t(\omega) &= \left(\frac{\omega_{geo}}{\omega}\right)^2 C_{tgeo} \\ R_{port}(\omega) &= R_x\left(\frac{\omega}{\omega_1}\right) \end{aligned} \tag{11}$$

All of the inductance values have now been defined and it only remains to compute the tuning capacitance values versus filter center frequency. The calculations involved are given by

$$C_{11}(\omega) = \frac{1}{\omega R_{port}(\omega)}\sqrt{\left(\frac{\omega_{geo}}{\omega}\right)\left(\frac{R_{port}(\omega)}{R_{geo\_core}}\right) + \omega^2 C_t^2(\omega) R_{port}(\omega) R_{geo\_core}\left(\frac{\omega}{\omega_{geo}}\right) - 1} \tag{12}$$

[11] L_r = 40.51 nH, L_c = 202.6 nH.

$$C_2(\omega) = \left[\frac{\omega^2 C_t(\omega)}{\left(\frac{\omega_{geo}}{\omega}\right)^2 \left(\frac{1}{R_{geo\_core}}\right)^2 + \omega^2 C_t^2(\omega)} - \frac{\omega^2 R_{port}^2(\omega) C_{11}(\omega)}{1 + \omega^2 R_{port}^2(\omega) C_{11}^2(\omega)} \right]^{-1} \tag{13}$$

The C_{11} capacitance must be adjusted to remove the additional reactance introduced by (6) finally leading to

$$C_1(\omega) = C_{11}(\omega) + \frac{1}{\omega\left(\omega L_m + \frac{R_o^2}{\omega L_m}\right)} \tag{14}$$

For this example, the resultant tuning capacitance values versus filter center frequency are as shown in Figure 22 corresponding to the filter response characteristics shown in Figure 23. The maximum-to-minimum capacitance ratios for C_1 and C_2 are nicely 3.376:1 and 4:1, respectively, illustrating the huge improvement over the design case without the L_m inductances.

Since one of the main purposes for the filters is the suppression of unwanted output harmonics, it is actually quite advantageous that the filter attenuation characteristics tend to be sharper on the high-side of the passband than on the low-side as shown in Figure 23.

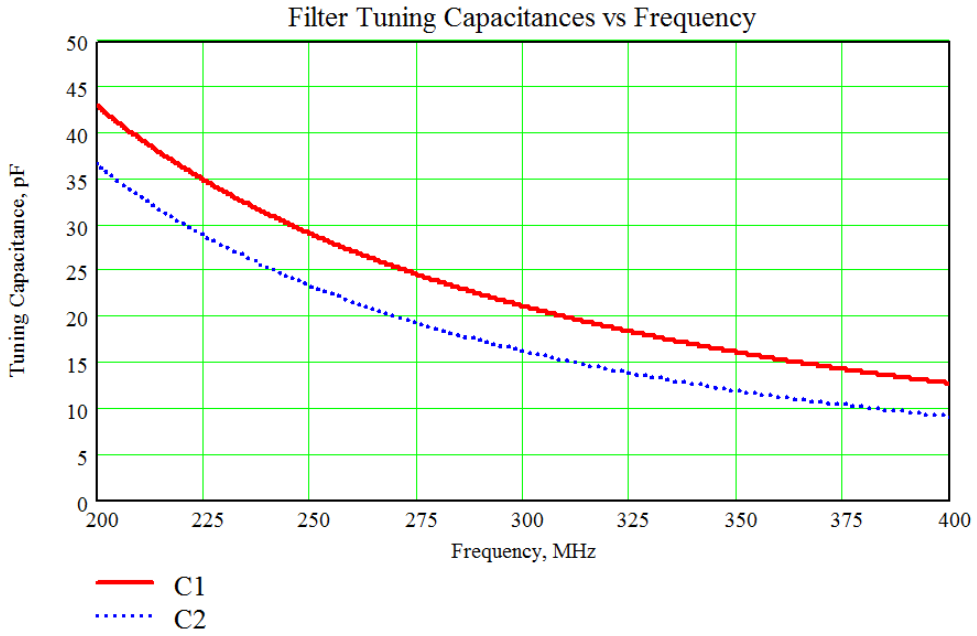


Figure 22 Tuning capacitance values for 200 MHz to 400 MHz filter example[12]

[12] U25110 AM1_S11_BPFs.mcd.

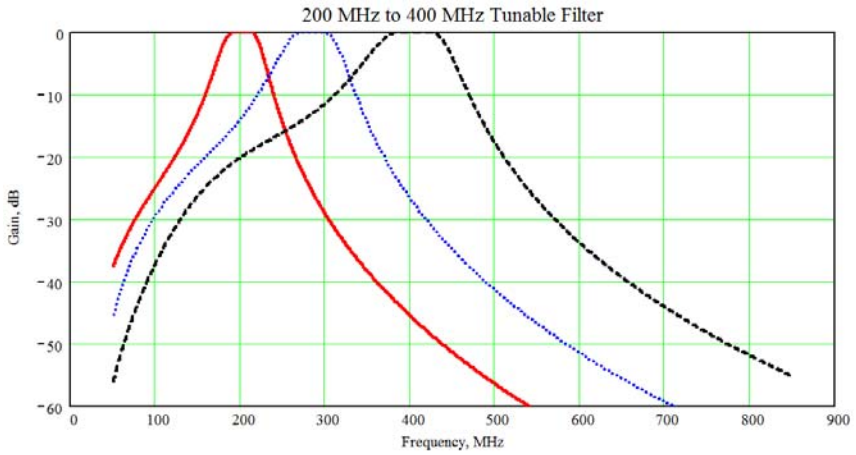


Figure 23 Ideal results for 200 MHz to 400 MHz filter example

3.1.2 Impedance Step-Down Configuration

The step-down impedance version of Figure 18 is also potentially needed in order to help arrive at reasonable component values across the full 10 MHz to 1350 MHz frequency span. This circuit configuration is shown in Figure 24. The combination of inductor L_m working with R_o is used to present port impedance values to the filter core which (approximately) increase linearly with filter center frequency as needed. Referring to Figure 25,

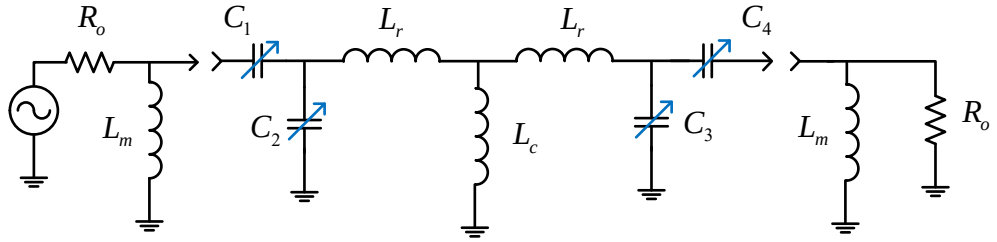


Figure 24 Impedance step-down filter configuration. For the general case, $C_1 = C_4$ and $C_2 = C_3$. Pay special note to the capacitor index-numbering adopted here is different[13] than in [3].

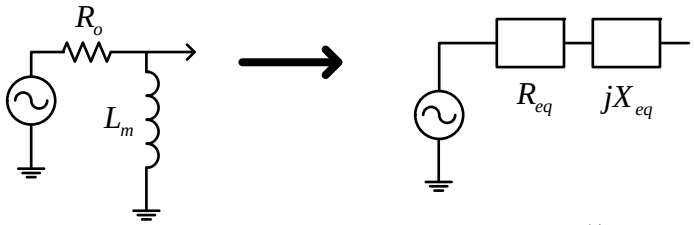


Figure 25 Inductor L_m is used to transform R_o to a lower impedance level[14]

$$R_{eq}(\omega) = R_o \frac{(\omega L_m)^2}{R_o^2 + (\omega L_m)^2} \tag{15}$$

[13] Graphics in U24157 Figures for U24143.vsd.
[14] Graphics in U25111 Tunable LC BPFs.vsd.

$$X_{eq}(\omega) = \omega L_m \frac{R_o^2}{R_o^2 + (\omega L_m)^2} \tag{16}$$

Since slight modifications to C_1 and C_4 can be incorporated to compensate for the additional reactance (16) the first matter for attention needs to be directed to choosing inductor L_m.

Performing the optimization for R_x and L_m in the resistance domain as done in (7) proved to be elusive and apparently ill-conditioned. After several different attempts, it was found that doing the optimization using conductances was a workable solution. The cost function used was

$$\Lambda(R_x, L_m) = \int_{\omega_1}^{\omega_2} \left[\frac{\omega_1}{R_x \omega} - \frac{1}{R_o} - \frac{R_o}{(\omega L_m)^2} \right]^2 d\omega \tag{17}$$

This integral has an easy closed-form solution given by

$$\Lambda = -\frac{\omega_1^2}{R_x^2}\left(\frac{1}{\omega_2} - \frac{1}{\omega_1}\right) + \frac{(\omega_2 - \omega_1)}{R_o^2} - \frac{R_o^2}{3L_m^4}\left(\frac{1}{\omega_2^3} - \frac{1}{\omega_1^3}\right) - \frac{2\omega_1}{R_o R_x}\log_e\left(\frac{\omega_2}{\omega_1}\right) + \frac{\omega_1 R_o}{R_x L_m^2}\left(\frac{1}{\omega_2^2} - \frac{1}{\omega_1^2}\right) - \frac{2}{L_m^2}\left(\frac{1}{\omega_2} - \frac{1}{\omega_1}\right) \tag{18}$$

The cost function can be minimized with respect to L_m by taking the derivative of (18) with respect to L_m which leads to a nice closed-form result as

$$L_m = \sqrt{\frac{\frac{R_o^2}{3}\left(\frac{1}{\omega_2^3} - \frac{1}{\omega_1^3}\right)}{\frac{1}{\omega_1} - \frac{1}{\omega_2} + \frac{\omega_1 R_o}{2R_x}\left(\frac{1}{\omega_2^2} - \frac{1}{\omega_1^2}\right)}} \tag{19}$$

Several example results for optimum R_x and L_m are provided in Table 6. As evidenced in these results, the frequency ratio f_2 / f_1 dictates the optimal value for R_x whereas the inductance L_m is scaled with frequency.

Table 6 Example Results for Optimized R_x and L_m ($R_o \equiv 50\Omega$)

f_1, MHz	f_2, MHz	L_m, nH	R_x, Ω	Λ	Figure
10	20	576.3	17.754	30.869	
10	15	655.1	20.441	1.859	Figure 26 Figure 27
10	25	524.7	15.937	136.957	
10	30	487.7	14.607	365.371	
20	40	288.2	17.754	61.737	Figure 28 Figure 29
40	80	144.1	“	123.474	
640	1280	9.01	“	1976.0	

Figure 26 through Figure 29 illustrate that this approach results in a very good approximation to the ideal resistance behavior for octave-band tuning.

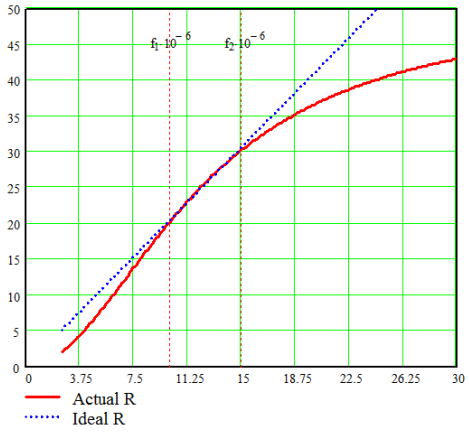


Figure 26 Ideal versus actual for 10 MHz to 15 MHz filter tuning range

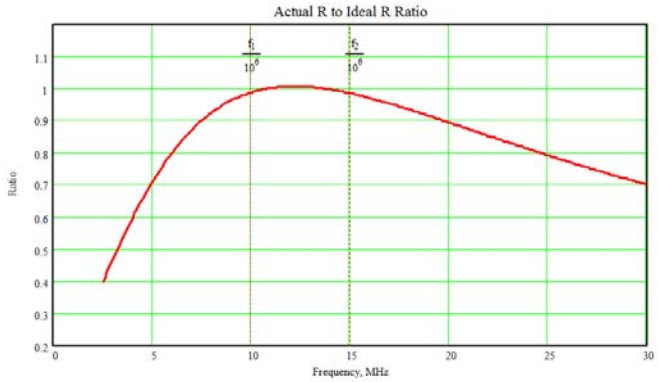


Figure 27 Figure 26 results shown as an impedance ratio

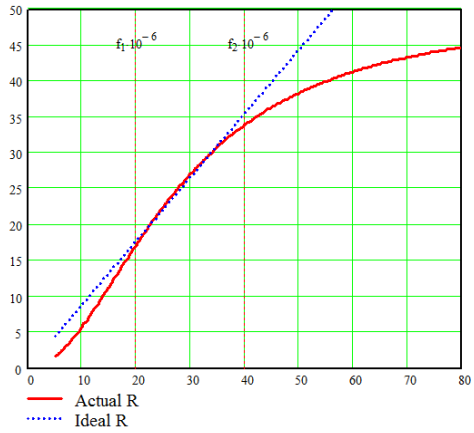


Figure 28 Ideal versus actual for 20 MHz to 40 MHz filter tuning range

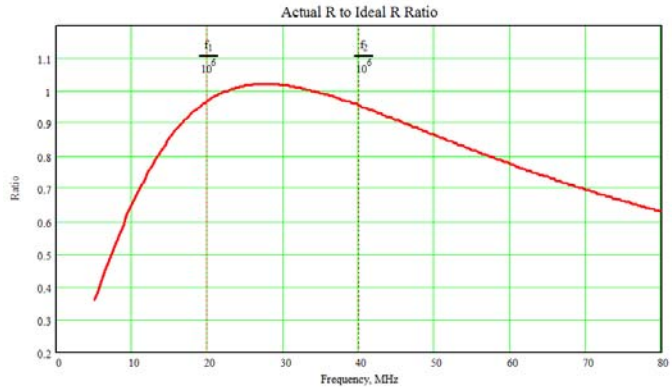


Figure 29 Figure 28 results shown as an impedance ratio

Subsequent filter design details can now follow [3]. The geometric center frequency for the filter is again given by

$$\omega_{geo} = 2\pi\sqrt{f_{low}\, f_{high}} \text{ rad/sec} \tag{20}$$

The coupling inductor L_c is simply

$$L_c = \frac{R_{geo}\gamma}{\omega_{geo}} \tag{21}$$

and

$$L_{eff} = \frac{R_{geo}}{\pi\sqrt{2}B_{geo}} \tag{22}$$

From (21) and (22),

$$L_r = L_{eff} - L_c \tag{23}$$

Continuing,

$$C_{tgeo} = \frac{1}{L_{eff}\,\omega_{geo}^2} \tag{24}$$

and

$$C_t = \left(\frac{\omega_{geo}}{\omega}\right)^2 C_{tgeo} \tag{25}$$

Next, define the real part of the impedance presented to the filter core (same as (15))

$$R_{port}\left(\omega_{tune}\right) = R_o \frac{\left(\omega_{tune} L_m\right)^2}{R_o^2 + \left(\omega_{tune} L_m\right)^2} \tag{26}$$

along with

$$\begin{aligned} R_t &= \left(\frac{\omega}{\omega_{geo}}\right)^{\gamma} R_{geo} \\ a\left(\omega_{tune}\right) &= -\omega_{tune}^2 R_{port}\left(\omega_{tune}\right) R_t\left(\omega_{tune}\right) \\ b\left(\omega_{tune}\right) &= \frac{1}{C_t\left(\omega_{tune}\right)} \\ d\left(\omega_{tune}\right) &= \frac{R_t\left(\omega_{tune}\right)}{R_{port}\left(\omega_{tune}\right)} \end{aligned} \tag{27}$$

and also compute

$$\begin{aligned} \alpha\left(\omega_{tune}\right) &= \frac{d\left(\omega_{tune}\right) - \dfrac{b\left(\omega_{tune}\right)^2}{a\left(\omega_{tune}\right)}}{1 + \dfrac{b\left(\omega_{tune}\right)^2}{a\left(\omega_{tune}\right)} - d\left(\omega_{tune}\right)} \\ \beta\left(\omega_{tune}\right) &= \frac{\dfrac{b\left(\omega_{tune}\right)}{a\left(\omega_{tune}\right)}}{1 + \dfrac{b\left(\omega_{tune}\right)^2}{a\left(\omega_{tune}\right)} - d\left(\omega_{tune}\right)} \end{aligned} \tag{28}$$

The solution for C_2 is found by solving the quadratic equation

$$a\alpha C_2^2 + \left(a\beta + b + b\alpha\right)C_2 + \left(b\beta - 1\right) = 0 \tag{29}$$

where the explicit dependencies on ω_{tune} have not been included. C_1 follows as

$$C_1 = \alpha C_2 + \beta \tag{30}$$

The step-down impedance configuration Figure 24 results in dramatically smaller tuning capacitance values for the lower frequency bands (e.g., 10 MHz to 20 MHz) than using the step-up configuration shown in Figure 18. Reasonable varactor diode arrangements can be found for the step-down configuration (see Figure 31) whereas this cannot be said of the step-up configuration. Unlike the step-up filter configuration, however, the upper stopband attenuation is not nearly as attractive for harmonic suppression as for the other configuration (See Figure 23 for a comparison.). Consequently there is still strong motivation to somehow employ the step-up filter configuration for lower frequency bands even if tunability must be realized using something other than varactors. To this end, a switched-capacitor arrangement will be used for the lower frequency bands as developed next in §3.2.

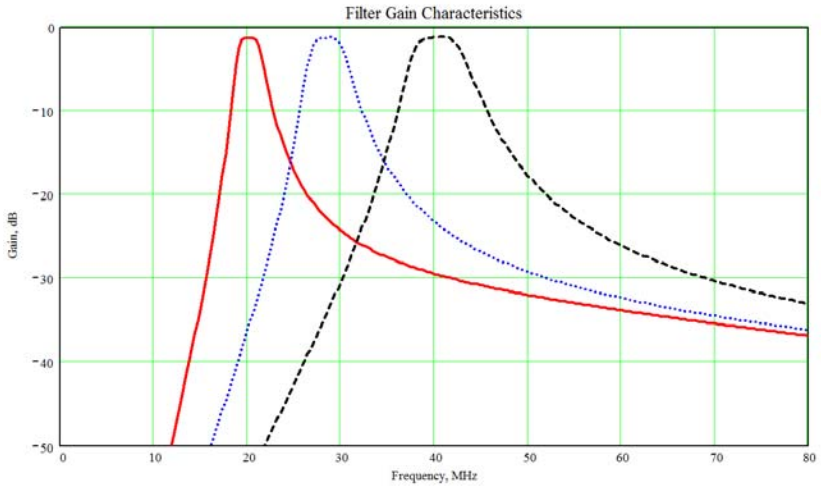


Figure 30 Step-down filter responses for covering 20 MHz through 40 MHz with the tuning capacitance values shown in Figure 31

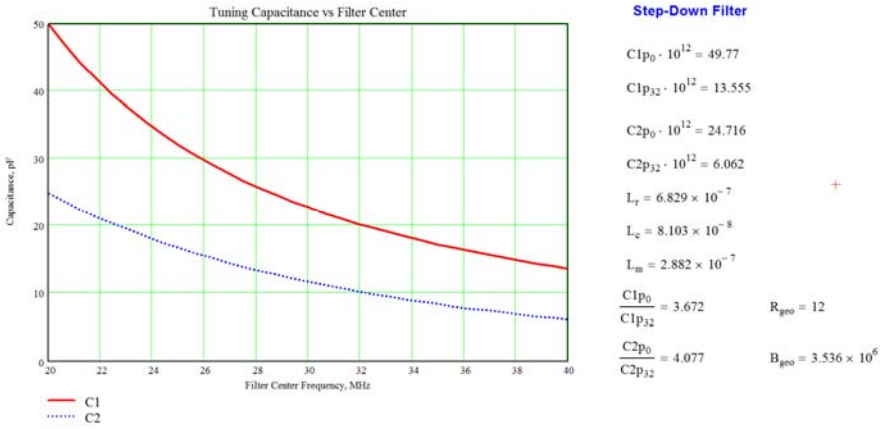


Figure 31 Tuning capacitance values versus filter center frequency associated with Figure 30

3.2 10 MHz to 160 MHz Filter Designs

The filtering operations shown in Figure 4 had to be broken into the two major bands (10 MHz to 160 MHz and 160 MHz to 1350 MHz) in order to accommodate frequency limitations in the RF switches and couplers. Each major band is addressed separately.

As already mentioned, since filter tuning only involves capacitive tuning, the maximum-to-minimum capacitance ratios must generally be a minimum of 4:1 for octave-band tuning. A range of varactor diode characteristics have been collected in Table 7 for easy reference.

Table 7 Varactor Diodes

Part No.	Supplier	Type	Single-Diode Cap(pF) / V	C-Ratio	Q @ 100 MHz, 3V
SMV1253-004LF	Digikey / Skyworks	Common-Cathode SOT-23	37(1) / 4.6(4.7)	12.3	146
SMV1255-004LF	Digikey / Skyworks	“	43.3(1) / 4.26(8)	10.16	160
SMV1234-004LF	Digikey / Skyworks	“	6.5(1) / 2.8(6)	2.8 – 3.4	1800
SMV1470-004LF	Digikey / Skyworks	“	70(1) / 8.5(7)	8.23	106
SMV2022-004LF	Mouser / Skyworks	“	7.5(0) / 0.8(15)	6	
SMV1213-004LF	Digikey / Skyworks	“	22.8(0.5) / 1.9(8.0)	12	
BB201	Mouser / NXP	“	97(1.0) / 15(15)	6.5	106
BB207	Mouser / NXP	“	81(1) / 17(15)	4.76	160
SVC276	Mouser / On	“	76.8(2) / 17(10) 100(1) / 17(10)	4.5 5.9	200
SVC236	Mouser / On	“	97(1) / 13.5(8)	7.2	100
SVC203C	Mouser / On	“	61(1) / 12.1(9)	5	60

3.2.1 10 MHz to 20 MHz Filtering

The design details for a step-up impedance filter solution are provided in Figure 32 and Figure 33. Although the capacitance ratios are attractive, the capacitance values are much larger than what can be reasonably accommodated using regulator varactor diodes, however.

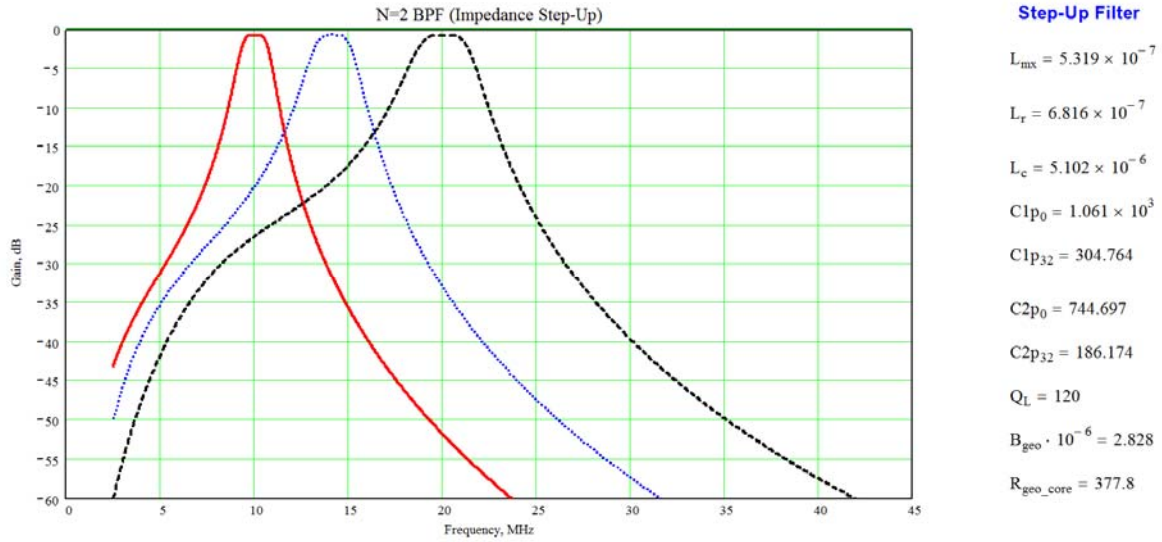


Figure 32 10 MHz to 20 MHz filter characteristics[15] using the impedance step-up configuration. Inductor-Q_L has been taken to be 120.

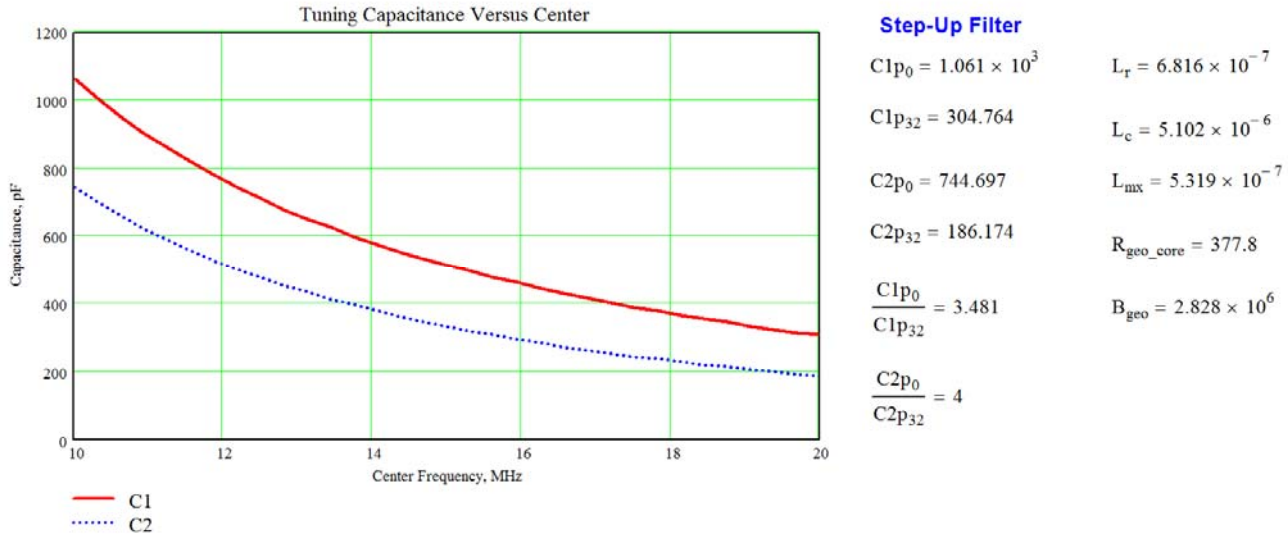


Figure 33 Tuning capacitance values for 10 MHz to 20 MHz coverage

[15] From U25110 AM1_S100_BPFs Up 10_20MHz.mcd.

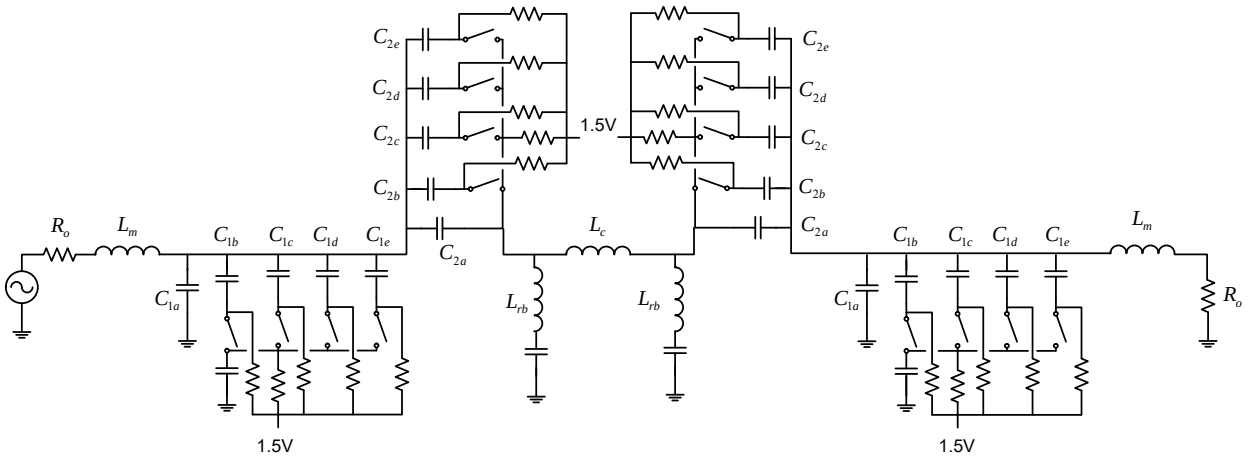


Figure 34 Step-up filter configuration[16] using switched capacitors associated with Figure 32 and Figure 33. All unlabeled resistors are 1MΩ. All switches are TS3A4751 SPST devices with 0.9Ω maximum on-resistance. It may be possible to use fewer resistors around the analog switches, but doing so would leave the normally-open switch terminals more or less open-circuited which could invite ESD problems.

Table 8 Component Values for Figure 34 (10 – 20 MHz BPF)

Component Reference	Value	Component Reference	Value	Component Reference	Value
C_{1a}	270 pF	C_{2a}	150 pF	L_m	540 nH
C_{1b}	56 pF	C_{2b}	43 pF	L_{rb}	680 nH
C_{1c}	110 pF	C_{2c}	82 pF	L_{rc}	5 µH
C_{1d}	220 pF	C_{2d}	180 pF		
C_{1e}	430 pF	C_{2e}	330 pF		

In contrast, the step-down impedance filter design shown in Figure 35 can be realized using only 6 back-to-back varactors from Table 7 as shown. Use of the L_m inductors makes this configuration now feasible. Two different bandwidth cases are presented following.

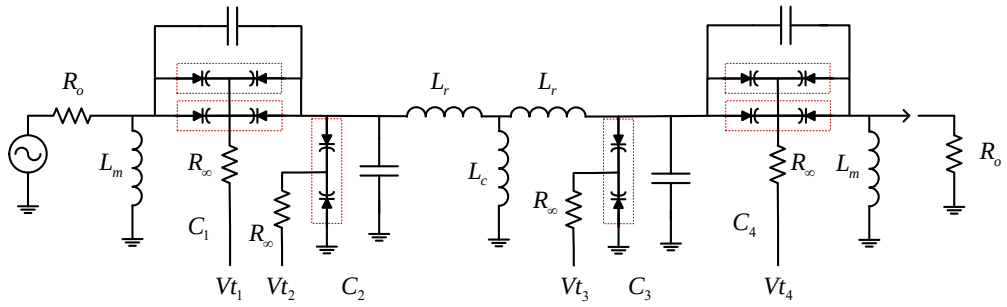


Figure 35 Step-down impedance filter using varactor diodes[17]

The first design utilizes a bandwidth of about 10% and is shown in Figure 36 and Figure 37. Since second-harmonic levels at the LMX2571 will be reasonably low, it is better to focus on filter attenuation at the 3rd harmonic frequency rather than the 2nd harmonic. Assuming an ideal square-wave at the LMX2571 output, the 3rd harmonic should be about –9.54 dBc. With the filter attenuation shown in Figure 36, this would situate the 3rd harmonic level between –45 dBc to –50 dBc for the 10 MHz to 20 MHz frequency

[16] From U25111 Tunable LC BPFs.vsd.
[17] Graphic from U25111.

band. Comparing these results with Figure 32 illustrates the much lower harmonic performance (better than –60 dBc) achievable using the step-up impedance filter configuration.

Increasing the filter bandwidth from 10% to 15% reduces the filter's insertion loss, but the stopband attenuation for 3rd harmonic suppression is also reduced as shown in Figure 38. Overall 3rd harmonic performance would likely be as poor as –40 dBc.

The Figure 34 configuration will therefore be used for the 10 MHz to 20 MHz tunable filter because of its much better stopband performance. Analog switches to be TS3A4751's.

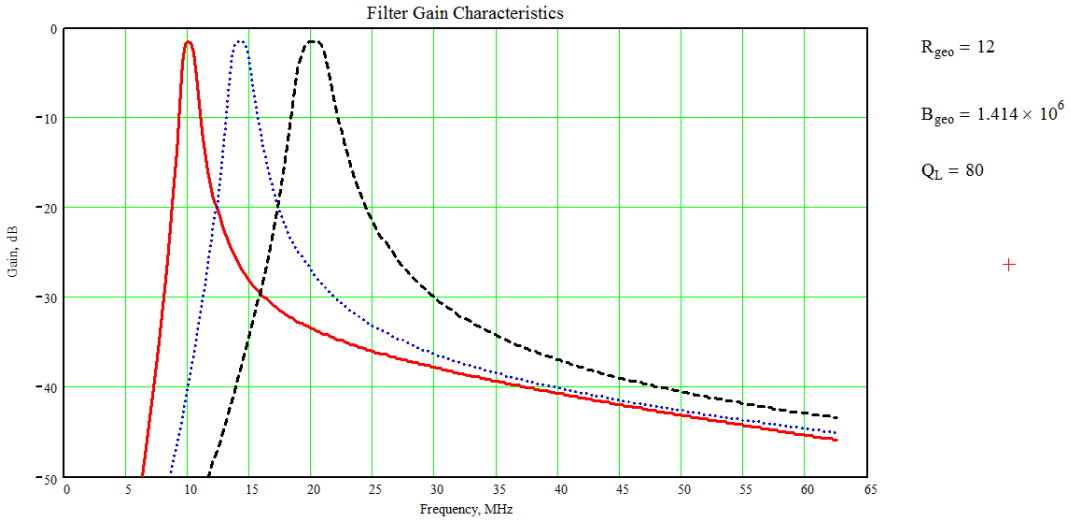


Figure 36 Step-down impedance filter attenuation characteristics[18] with 10% nominal bandwidth. Third-harmonic suppression is on the order of 35 dB to 43 dB as shown. Tuning capacitance values associated with Figure 35 and Figure 36 are shown in Figure 37. Capacitance C_1 generally requires two parallel varactor-pairs whereas capacitance C_2 can be realized using only one varactor-pair.

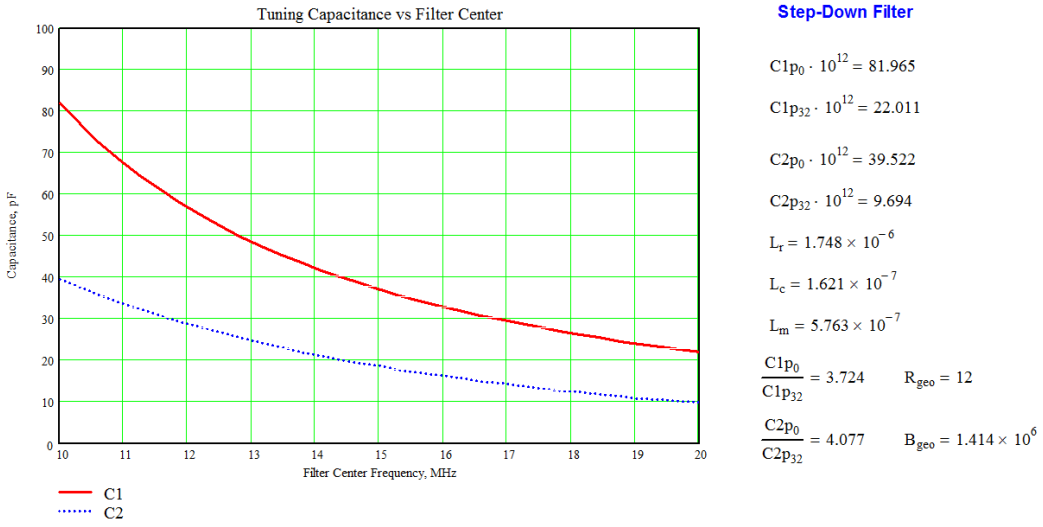


Figure 37 Tuning capacitance values for Figure 36 as a function of filter center frequency. Generally speaking $C_3 = C_2$ and $C_4 = C_1$.

[18] From U25112 AM1_S100_BPFs Down.mcd.

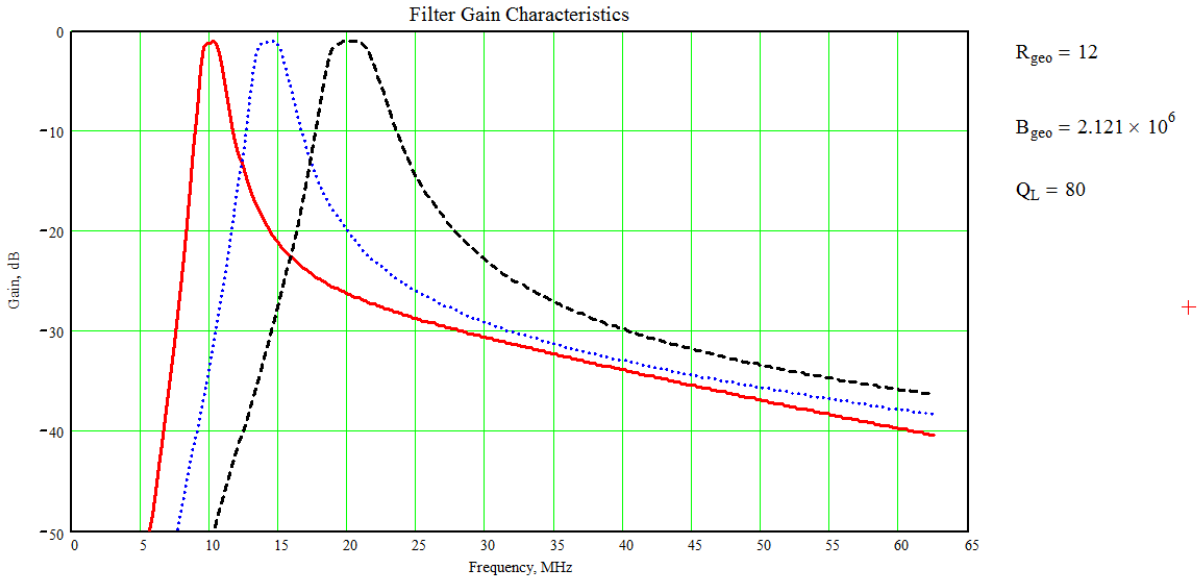


Figure 38 Step-down impedance filter attenuation characteristics[19] with 15% nominal bandwidth.

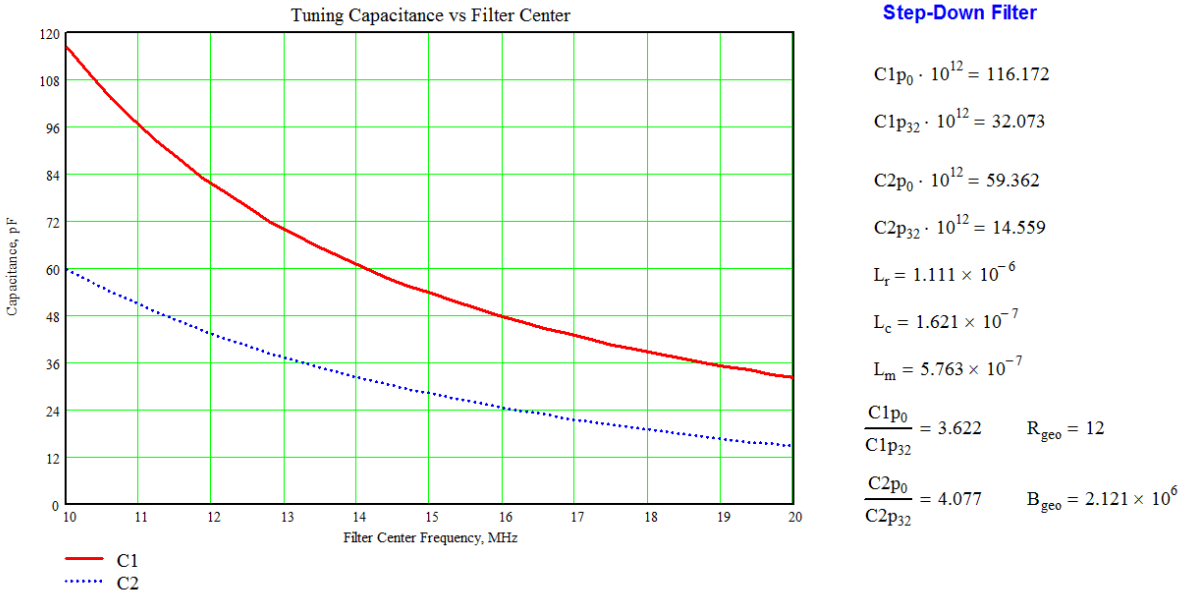
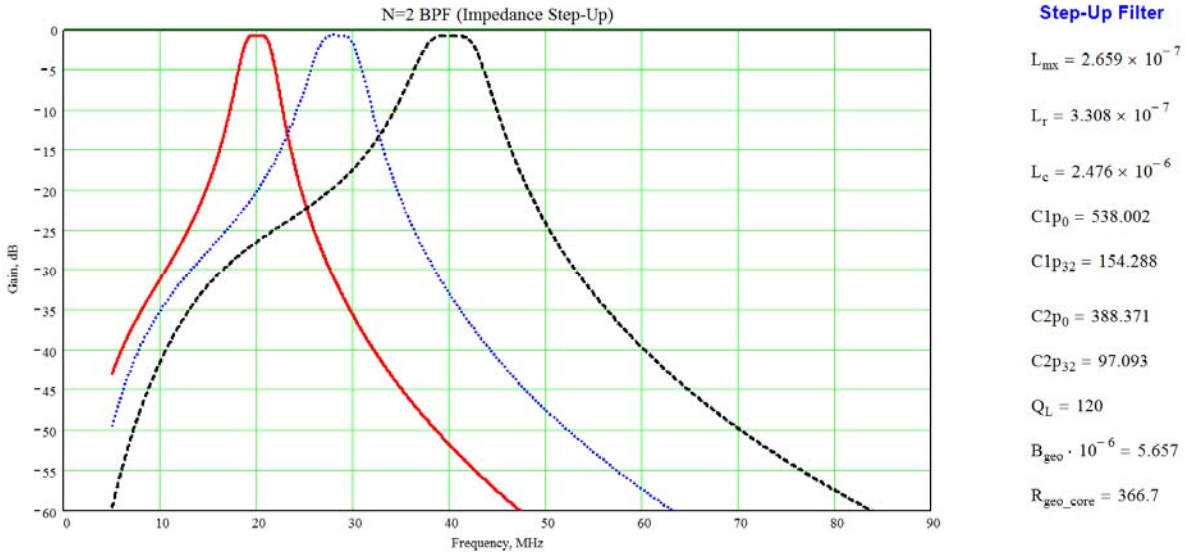


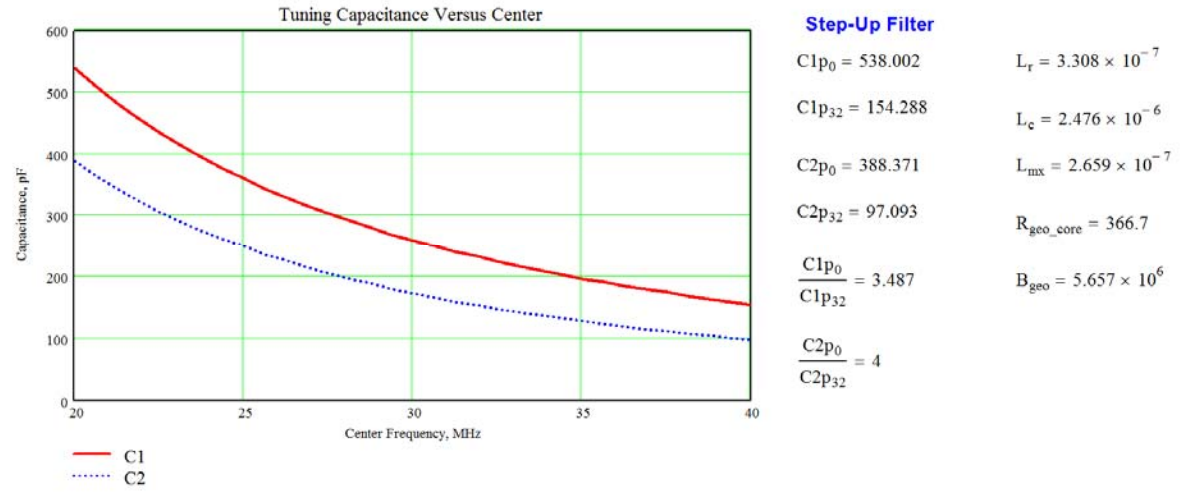
Figure 39 Tuning capacitance values for Figure 38 as a function of filter center frequency.

[19] From U25112 AM1_S100_BPFs Down.mcd.

3.2.2 20 MHz to 40 MHz

Step-up impedance filter configuration shown in Figure 34 will be used again here.





The Figure 34 configuration will be used for the 20 MHz to 40 MHz tunable filter. Analog switches to be TS3A4751's.

Table 9 Component Values for Figure 34 (20 – 40 MHz BPF)

Component Reference	Value	Component Reference	Value	Component Reference	Value
C_{1a}	120 pF	C_{2a}	68 pF	L_m	270 nH
C_{1b}	30 pF	C_{2b}	22 pF	L_{rb}	330 nH
C_{1c}	62 pF	C_{2c}	43 pF	L_{rc}	2.4 µH
C_{1d}	120 pF	C_{2d}	82 pF		
C_{1e}	240 pF	C_{2e}	160 pF		

3.2.3 40 MHz to 80 MHz

This frequency range is high enough that use of the TS3A4751 analog switches could be problematic. Since first-pass success is important in this project, only varactor diode based designs will be considered above 40 MHz. Multiple back-to-back varactors are required as shown in Figure 40.

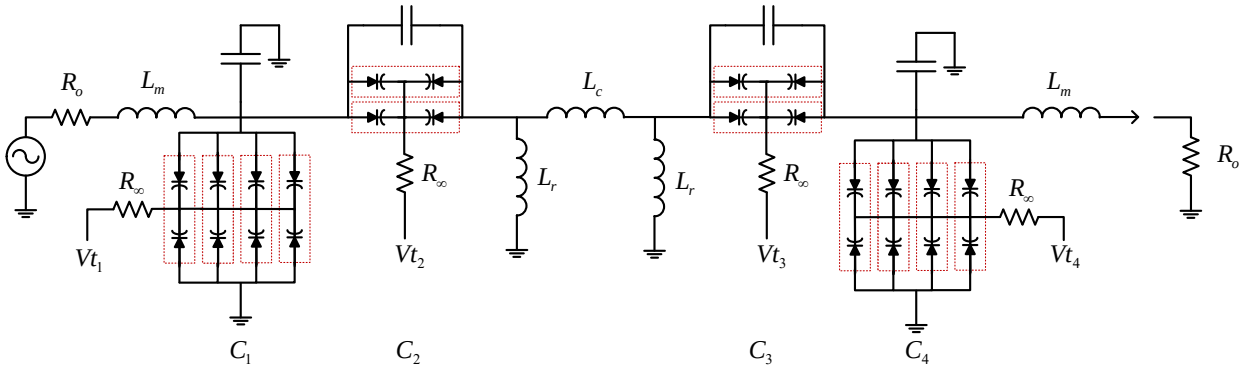


Figure 40 Schematic configuration for step-up impedance filter using multiple back-to-back varactor diodes

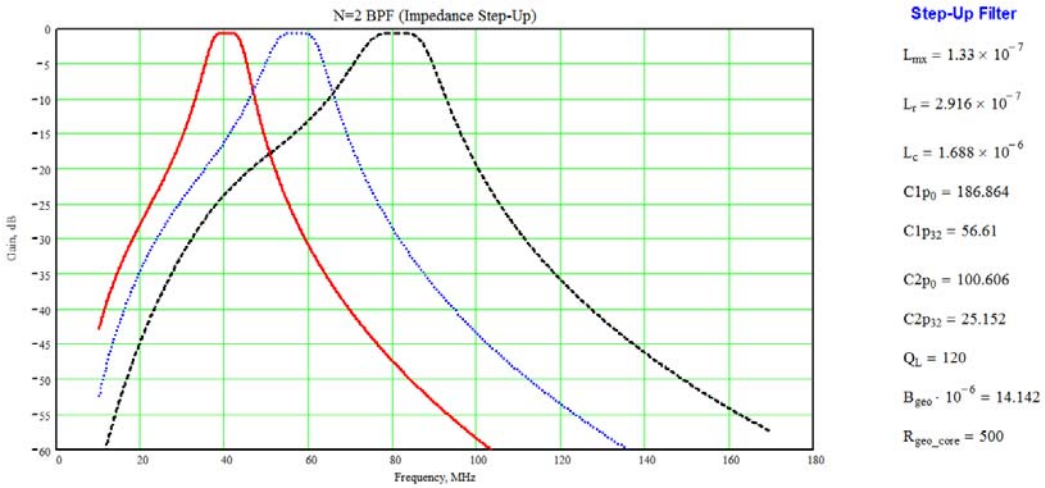


Figure 41 40 MHz to 80 MHz tunable bandpass filter using schematic shown in Figure 40

Table 10 Component Values for Figure 40 for 40 MHz to 80 MHz Tunable Filter in Figure 40

Reference Designator	Components	Comments
L_m	130 nH	
C_1 and C_4	16 pF fixed + 4 x SVC236 or 4 x BB201	
C_2 and C_3	5.6 pF fixed + 2 x SVC236 or 2 x BB201	
L_r	300 nH	
L_c	1.6 μH	

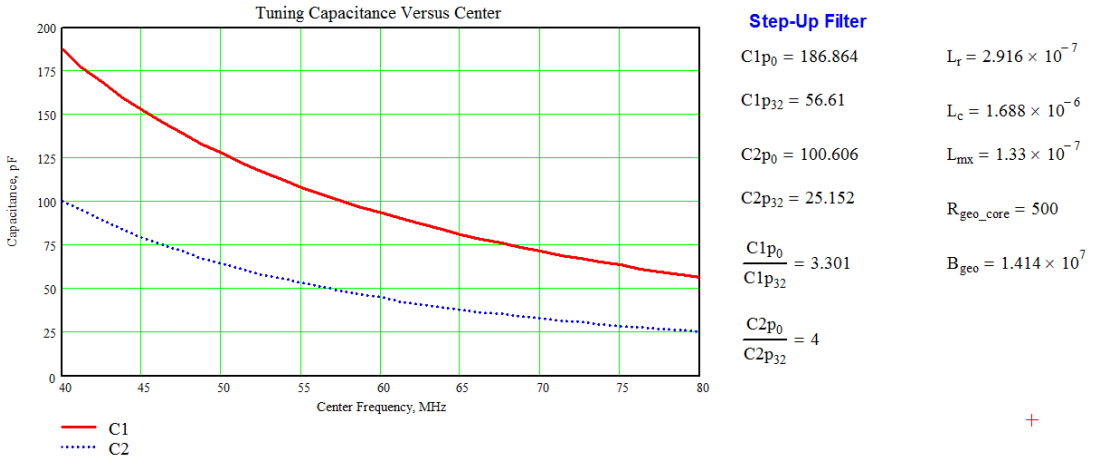


Figure 42 Tuning capacitance values for 40 MHz to 80 MHz filter associated with Figure 41

3.2.4 80 MHz to 160 MHz

The step-up impedance filter topology will be used for this filter as shown in Figure 40.

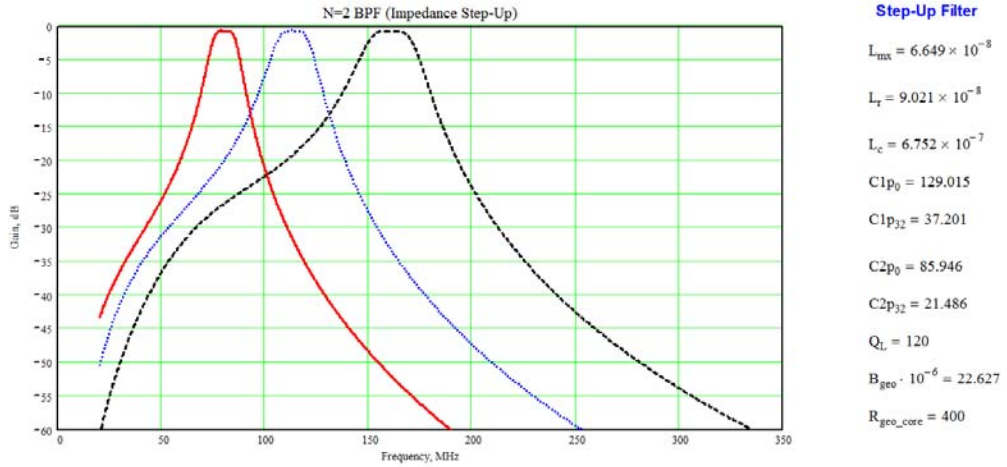


Figure 43 Filter gain characteristics for 80 MHz to 160 MHz case[20]

Table 11 Component Values for Figure 40 for 80 MHz to 160 MHz Tunable Filter in Figure 40

Reference Designator	Components	Comments
L_m	68 nH	
C_1 and C_4	10 pF fixed + 3 x SVC236 or 3 x BB201	
C_2 and C_3	3.3 pF fixed + 2 x SVC236 or 2 x BB201	
L_r	90 nH	
L_c	680 nH	

[20] U25110 AM1_S100_BPFs Up 80_160MHz.mcd.

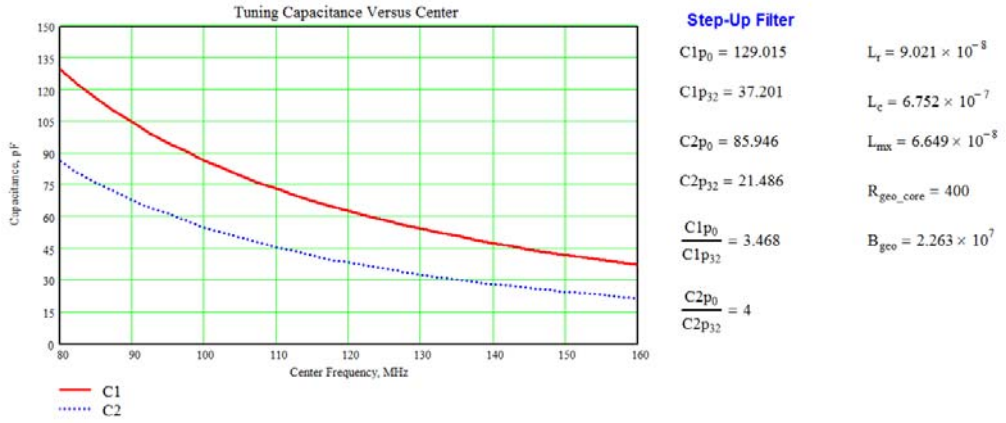


Figure 44 Tuning capacitance values versus frequency associated with Figure 43

3.3 160 MHz to 1400 MHz Filtering

All of the higher frequency filters utilize the step-up impedance filter configuration shown in Figure 40.

3.3.1 160 MHz to 320 MHz Filtering

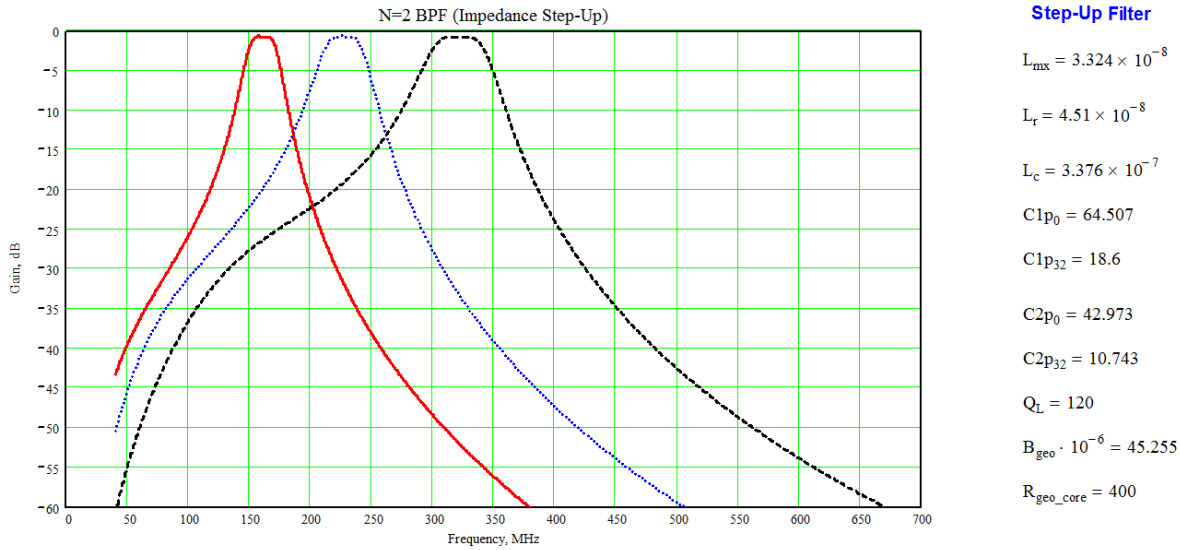


Figure 45 Filter gain characteristics for 160 MHz to 320 MHz case[21]

[21] U25110 AM1_S100_BPFs Up 160_320MHz.mcd.

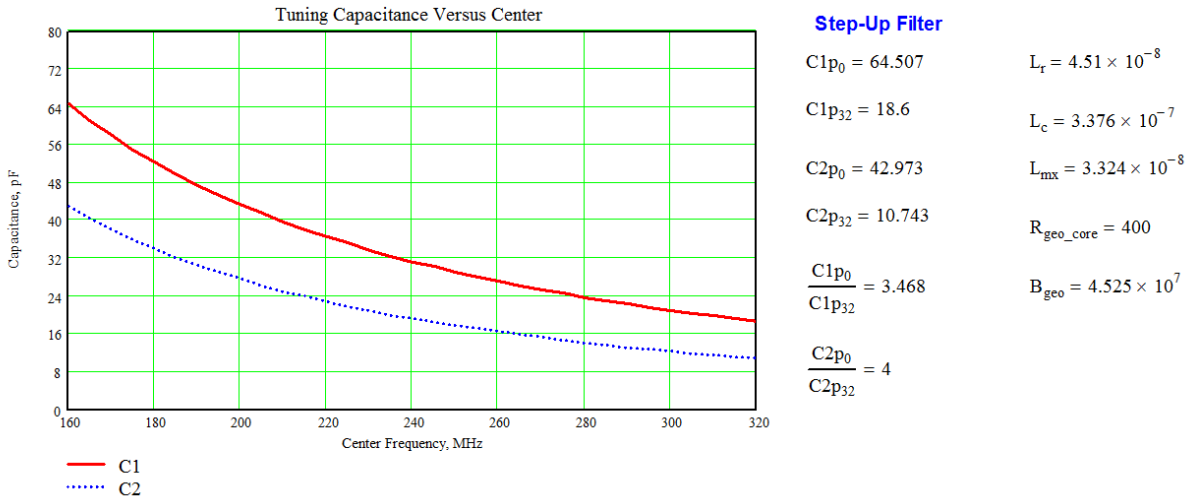


Figure 46 Tuning capacitance values versus frequency associated with Figure 45

Table 12 Component Values for Figure 40 for 160 MHz to 320 MHz Tunable Filter in Figure 40

Reference Designator	Components	Comments
L_m	33 nH	
C_1 and C_4	5.6 pF fixed + 2 x SMV1470	
C_2 and C_3	0 pF fixed + 2 x SMV1470	
L_r	43 nH	
L_c	330 nH	

3.3.2 320 MHz to 640 MHz Filtering

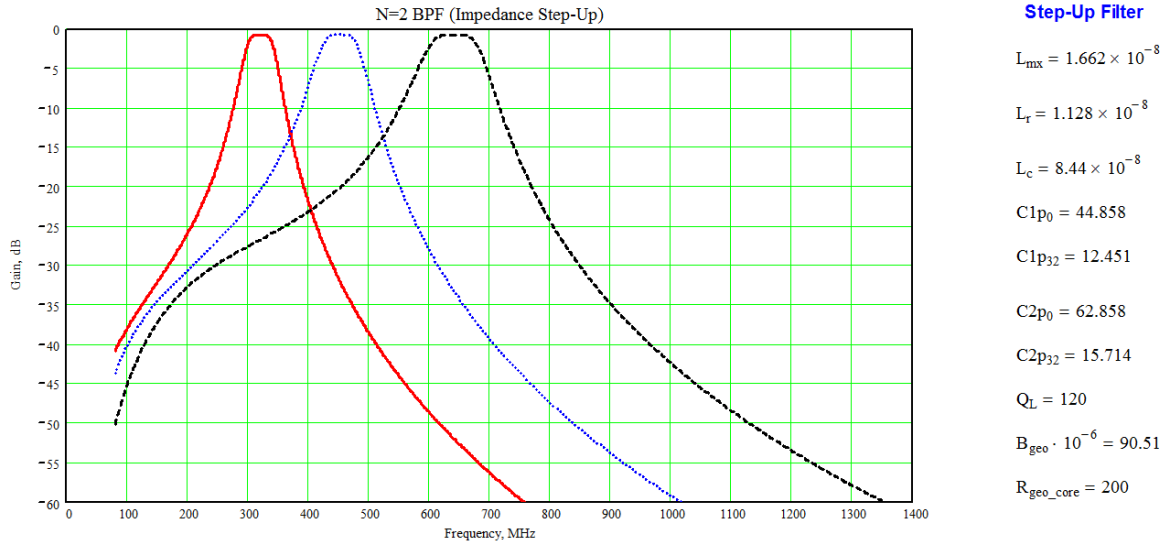


Figure 47 Filter gain characteristics for 320 MHz to 640 MHz case[22]

[22] U25110 AM1_S100_BPFs Up 320_640MHz.mcd.

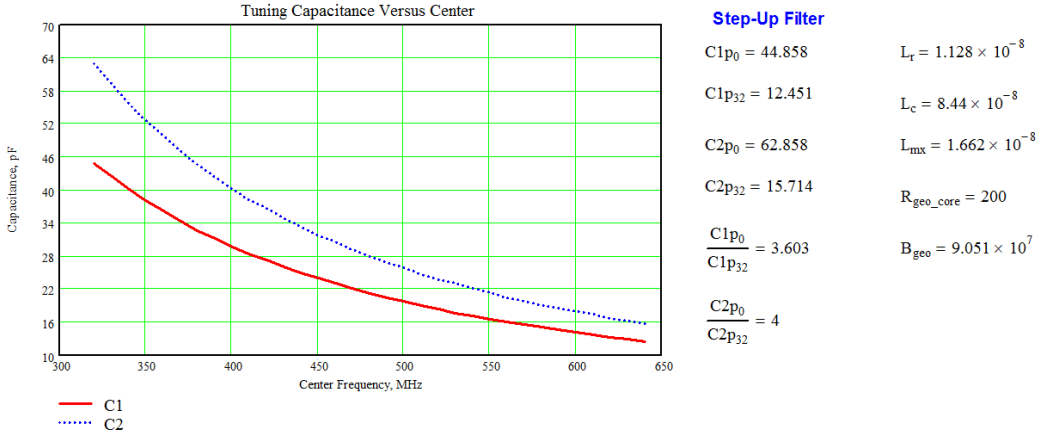


Figure 48 Tuning capacitance values versus frequency associated with Figure 47

Table 13 Component Values for Figure 40 for 320 MHz to 640 MHz Tunable Filter in Figure 40

Reference Designator	Components	Comments
L_m	16 nH	
C_1 and C_4	0 pF fixed + 2 x SMV1470	
C_2 and C_3	0 pF fixed + 2 x SMV1470	
L_r	10 nH	
L_c	82 nH	

3.3.3 640 MHz to 1000 MHz Filtering

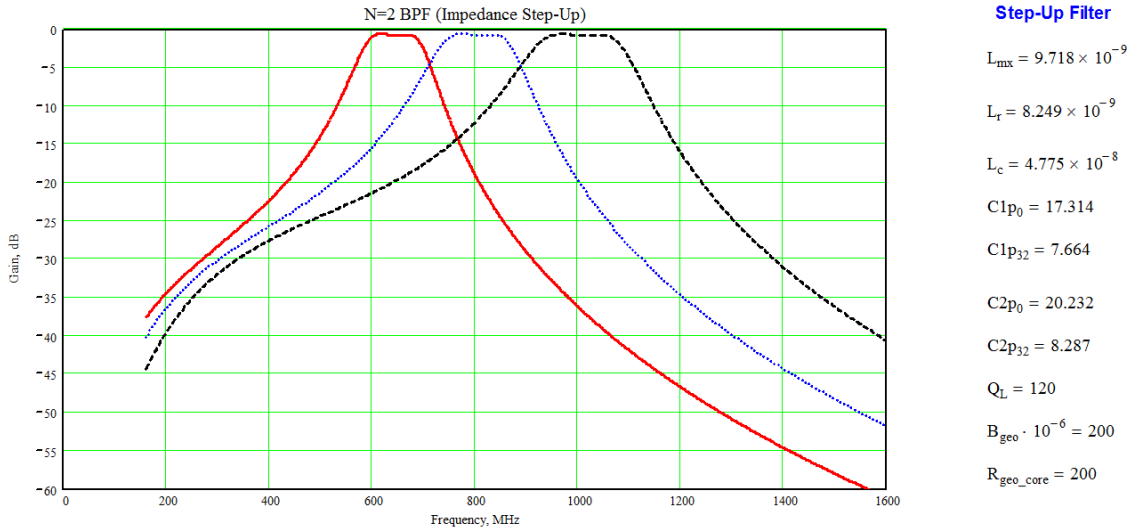


Figure 49 Filter gain characteristics for 640 MHz to 1000 MHz case[23]

[23] U25110 AM1_S100_BPFs Up 640_1000MHz.mcd.

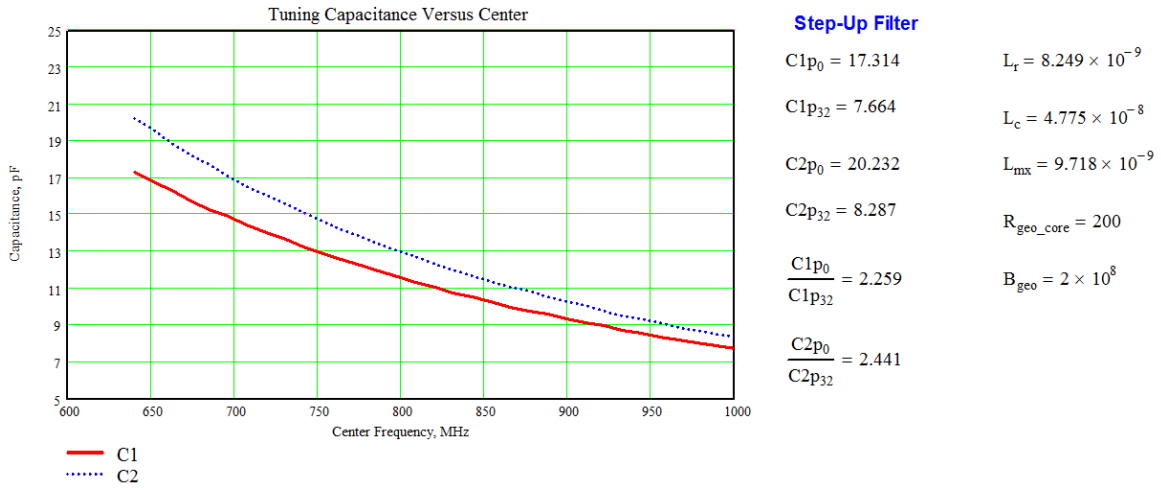


Figure 50 Tuning capacitance values versus frequency associated with Figure 49

Table 14 Component Values for Figure 40 for 640 MHz to 1000 MHz Tunable Filter in Figure 40

Reference Designator	Components	Comments
L_m	10 nH	
C_1 and C_4	0 pF fixed + 1 x SMV1470	
C_2 and C_3	0 pF fixed + 1 x SMV1470	
L_r	8.2 nH	
L_c	47 nH	

3.3.4 1000 MHz to 1400 MHz Filtering

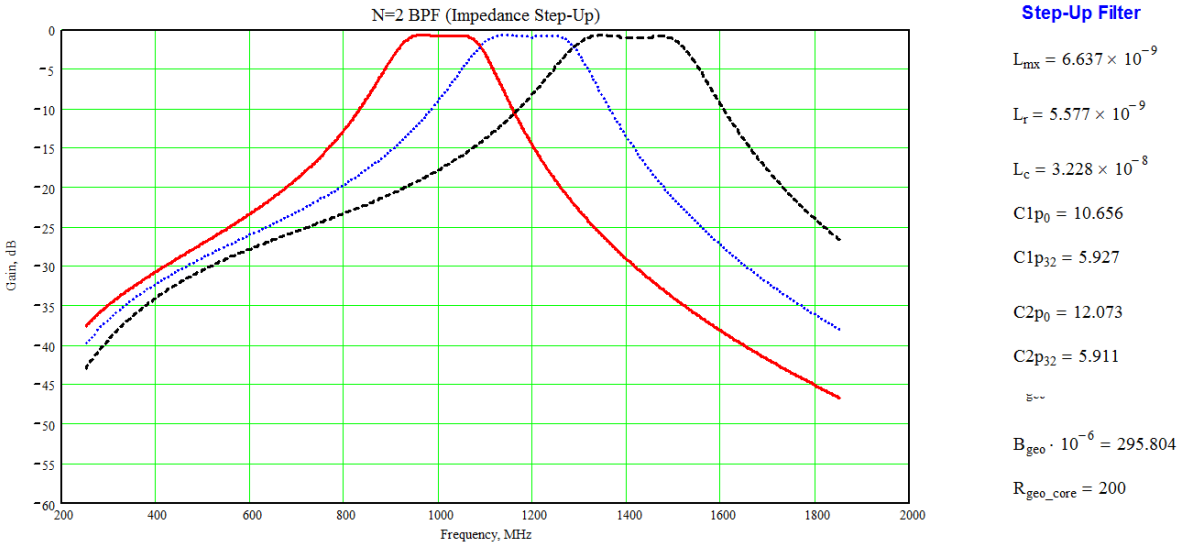


Figure 51 Filter gain characteristics for 100 MHz to 1400 MHz case[24]

[24] U25110 AM1_S100_BPFs Up 1000_1400MHz.mcd.

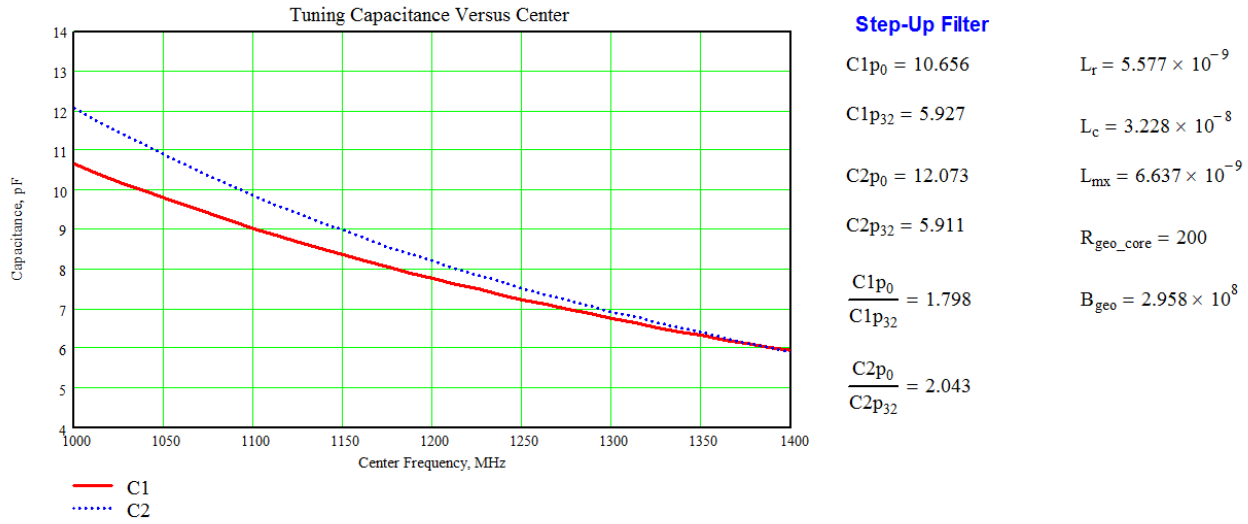


Figure 52 Tuning capacitance values versus frequency associated with Figure 51

Table 15 Component Values for Figure 40 for 1000 MHz to 1400 MHz Tunable Filter in Figure 40

Reference Designator	Components	Comments
L_m	6.8 nH	
C_1 and C_4	0 pF fixed + 1 x SMV1253-004	
C_2 and C_3	0 pF fixed + 1 x SMV1253-004	
L_r	5.6 nH	
L_c	33 nH	

3.3.4.1 Microstrip Versions

Inductance values in Table 15 are becoming rather small. It is consequently worthwhile to consider using a microstrip implementation for the shunt inductors. A parallel coupled-line configuration is shown in Figure 53 whereas the coupling is performed using a lumped inductance in Figure 56.

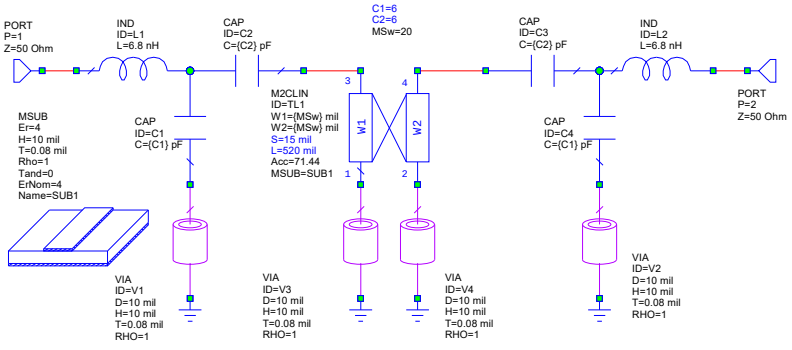


Figure 53 Microstrip implementation of 1000 MHz to 1400 MHz tunable filter using Microwave Office. Relative dielectric constant ε_r = 4.0, dielectric thickness = 10 mils. Microstrip width = 20 mils, microstrip length = 520 mils, and spacing = 15 mils.

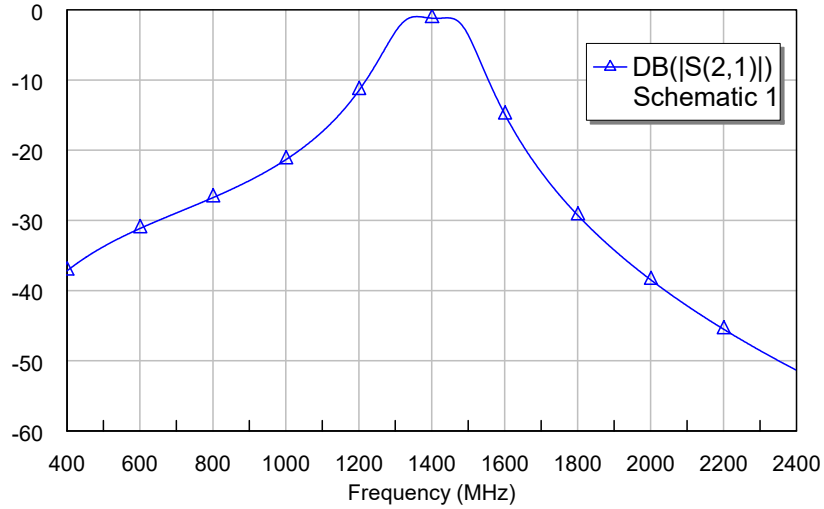


Figure 54 Frequency response of Figure 53 with C_1 = C_2 = 6 pF

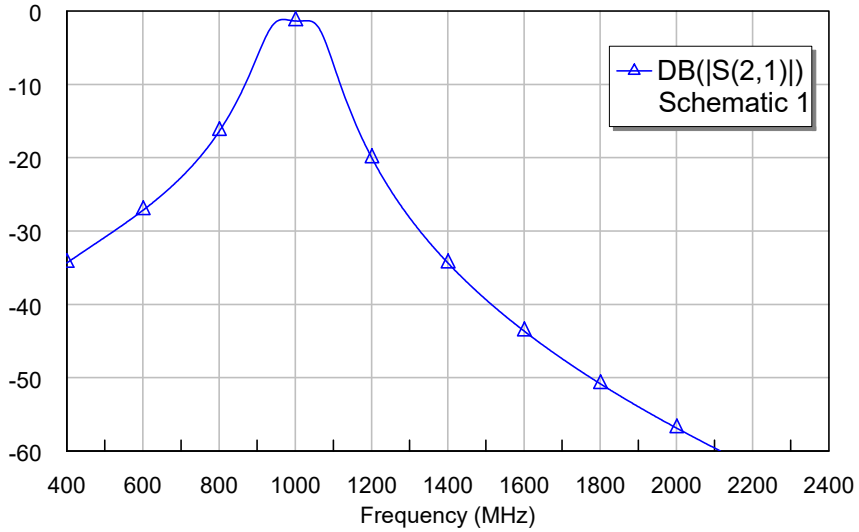


Figure 55 Frequency response of Figure 53 with C_1 = 12 pF and C_2 = 13 pF

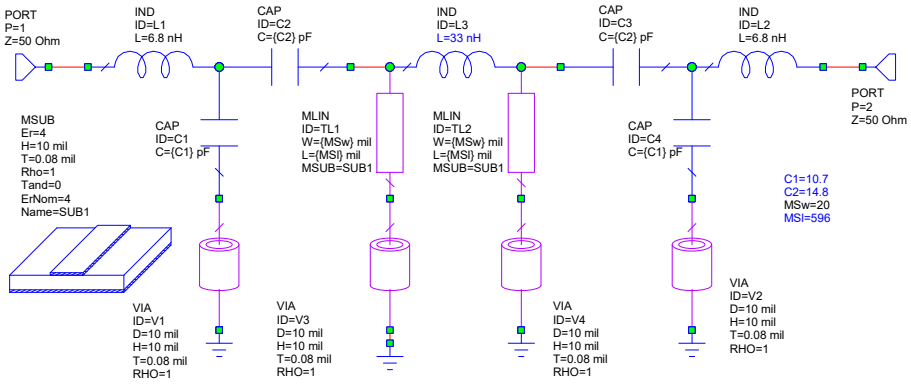


Figure 56 Microstrip implementation using discrete inductor for coupling action

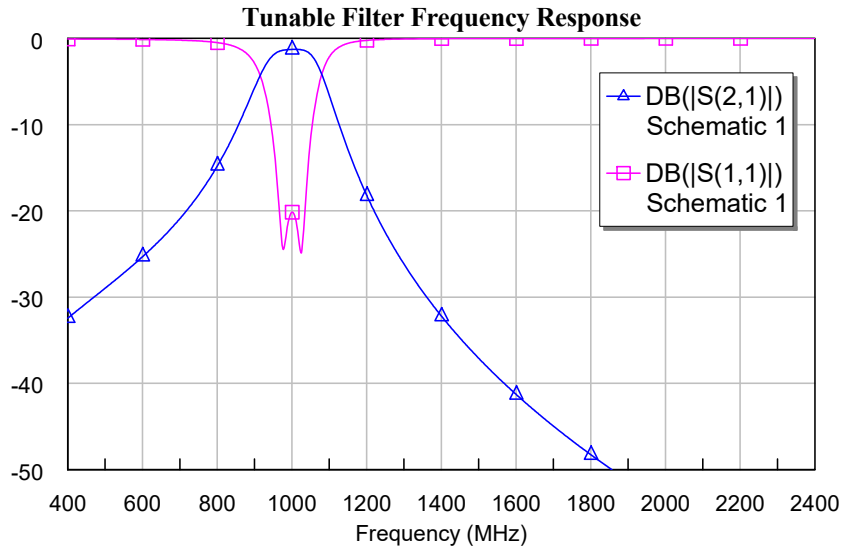


Figure 57 Filter response associated with Figure 56 with C_1 = 10.7 pF and C_2 = 14.8 pF with transmission line length of 600 mils

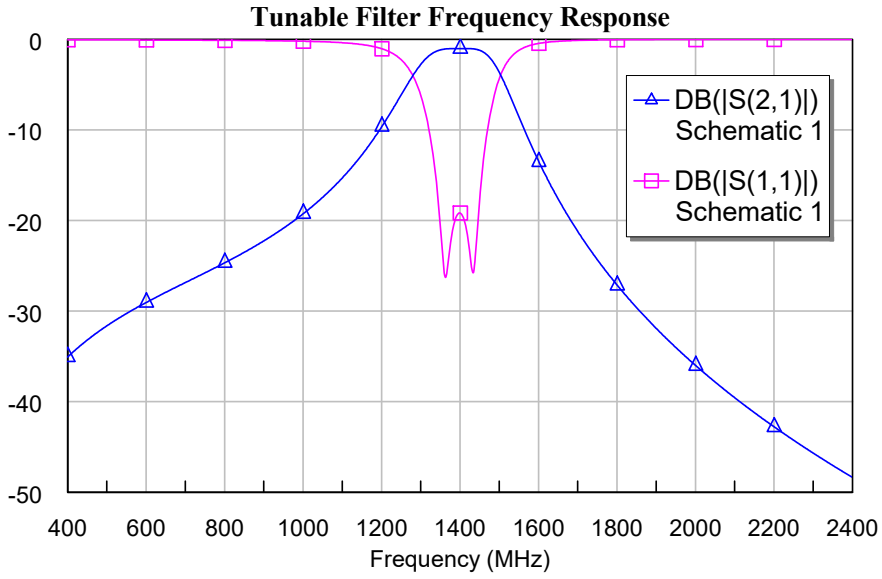


Figure 58 Filter response associated with Figure 56 with C_1 = 5.3 pF and C_2 = 6.7 pF with transmission line length of 600 mils

3.4 Automatic Level Control

Output automatic level control (ALC) is based upon

i. Sensing a portion of the output post-filtering signal using a precision coupler
ii. Measuring the coupled power level using a LT5581 and reading the associated power measurement with the Arduino MEGA2560
iii. Close a software control loop within the Arduino MEGA2560 to first compute a corrective attenuation control value, which is provided to a 16-bit D/A converter (DAC8552 from TI)
iv. Apply the analog control voltage to the attenuation control element

Additional details about the control software and algorithms will be provided in the Arduino software section of Part III.

After doing the background investigation for a low-frequency variable attenuator, I stumbled on to a rather unique device from *IDT* which covers 1 MHz through 3000 MHz: IDTF2255. This device can be used for both the low and high frequency ranges as shown in Figure 4. Performance charts for this device are shown in Figure 59 and Figure 60.

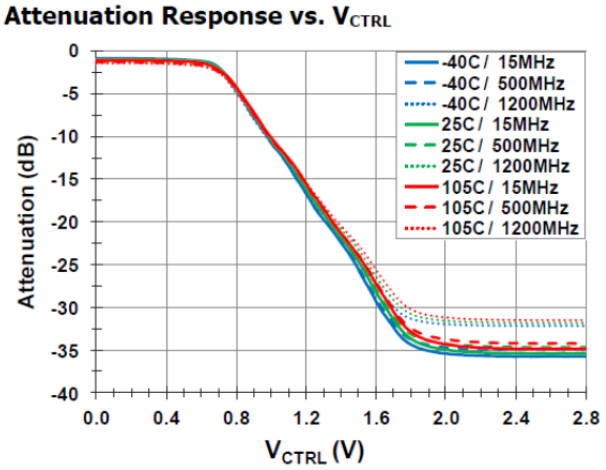


Figure 59 Attenuation control characteristic of the IDTF2255

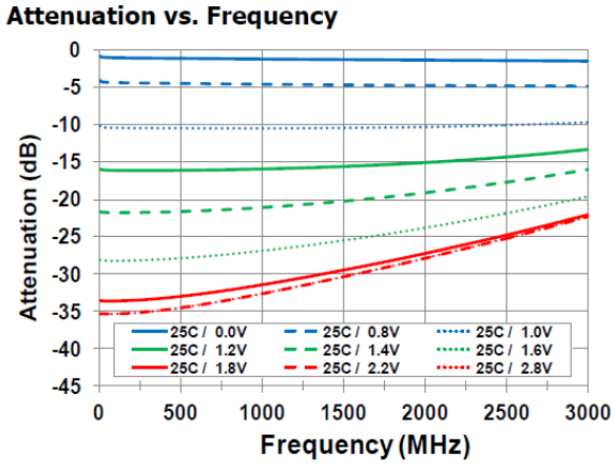


Figure 60 Frequency response of the IDTF2255

4 References

1. James A. Crawford, “AM1-S100 Frequency Synthesizer, Part I”, U24872, 29 Oct. 2017.
2. _____, “Tunable Bandpass Filters- Part I,” U24143.
3. _____, “Tunable Bandpass Filters- Part II,” U24143.
4. _____, “Tunable Bandpass Filters- Part III,” U24143.
5. _____, “Bandpass Filters Feature Wide Tuning Ranges,” *Microwaves & RF*, 28 Nov. 2017.
6. USPAT 4,975,604, “Automatic Return-Loss Optimization of a Variable FET Attenuator,”, 4 Dec. 1990.

5 Appendix: Phase Noise Analysis of 100 MHz PLL

Working Directory: G:_My Projects_Projects_RF Related Projects_Synthesizer AM1-S100\Phase Noise Analysis
Project File Name: 100MHzPLL_Trial_01.prm
Date & Time: 1/1/2018 7:36:25 PM

1> Comment:
Comment Here: 100 MHz PLL for AM1-S100
2> Comment:
Comment Here:
3> Comment:
Comment Here:
4> Source1 (RF): SRC1x
RF Signal Source Output: 10
Filename for Source PSD: 10MHz_ocxo.psd
Source Spectrum: On
5> Comment:
Comment Here:
6> Phase Detector: Charge-Pump: PDx
+/-Ref RF Input: 10
+/-Feedback RF Input: 100
Baseband Charge-Pump Output: 30
Phase Detector Gain, A/rad: 0.000318
PDCP Figure of Merit, dBc/Hz: -225
1/f Noise Corner, Hz: 1e3
Phase Comparison Frequency, Hz: 10e6
Figure of Merit: On
7> Capacitor: C01
+ Node: 30
- Node: 0
Capacitance, Farads: 1e-6
8> Capacitor: C02
+ Node: 40
- Node: 0
Capacitance, Farads: 33e-6
9> Capacitor: C03
+ Node: 50
- Node: 0
Capacitance, Farads: 0.1e-6
10> Capacitor: C04
+ Node: 60
- Node: 0
Capacitance, Farads: 0.1e-6
11> Resistor: R01
+ Node: 30
- Node: 40
Resistance, Ohms: 510
Nyquist Noise: On
12> Resistor: R02
+ Node: 30
- Node: 50
Resistance, Ohms: 1e3
Nyquist Noise: On
13> Resistor: R03
+ Node: 50
- Node: 60
Resistance, Ohms: 1e3
Nyquist Noise: On
14> Comment:
Comment Here:
15> VCO2 (PSD File for Self-Noise): VCOx
VCO Tuning Port: 60

VCO RF Output: 70
Tuning Sensitivity, Hz/V: 2500
VCO Self-Noise PSD: 100MHz_cvhd950.psd
Oscillator Self-Noise: On

16> Splitter (RF): SPLx
RF Input Signal: 70
RF Output #1: 80
RF Output #2: 90

17> Resistor: Rxx
+ Node: 80
- Node: 0
Resistance, Ohms: 50
Nyquist Noise: On

18> Probe Point: PRBx
Probe Input: 80
Name for Probe: Loop_Out

19> Comment:
Comment Here:

20> Digital Divider: DIVx
RF Input Signal: 90
RF Output Signal: 100
Divide Ratio: 10
Input-Referred Noise Figure, dB: 10
Input Carrier Level, dBm: 0
1/f Noise Corner, Hz: 1000
Output Phase Noise Floor, dBc/Hz: -160
Noise Figure Related Noise: On
Output Noise Floor Limit: On

21> Comment:
Comment Here:

22> Comment:
Comment Here:

23> Comment:
Comment Here: 100MHz VCXO

24> Comment:
Comment Here:

25> Source1 (RF): SRC1x
RF Signal Source Output: 200
Filename for Source PSD: 100MHz_cvhd950.psd
Source Spectrum: On

26> Resistor: Rxx
+ Node: 200
- Node: 0
Resistance, Ohms: 50
Nyquist Noise: On

27> Probe Point: PRBx
Probe Input: 200
Name for Probe: VCXO_Alone

28> Comment:
Comment Here:

29> Comment:
Comment Here: Perfectly Multiplied OCXO

30> Comment:
Comment Here:

31> Source1 (RF): SRC1x
RF Signal Source Output: 300
Filename for Source PSD: 10MHz_ocxo.psd
Source Spectrum: On

32> Frequency Multiplier: FMXx
RF Input Signal: 300
RF Output Signal: 310
Frequency Multiplication Factor: 10
Input Carrier Level, dBm: 0

Input-Referred Noise Figure, dB: 1
1/f Noise Corner, Hz: 1
Noise Figure Related Noise: On

33> Resistor: Rxx

+ Node: 310
- Node: 0
Resistance, Ohms: 50
Nyquist Noise: On

34> Probe Point: PRBx

Probe Input: 310
Name for Probe: MultipliedOCXO

35> Comment:

Comment Here:

36> Minimum Frequency for Analysis:

Frequency Minimum, Hz: 10

37> Maximum Frequency for Analysis:

Frequency Maximum, Hz: 10e6

38> Number of Frequency Points:

Number of Points: 256

5.1 SPICE-Like Script File

```
xxx 100 MHz PLL for AM1-S100
xxx
xxx
src1 SRC1x 10 10MHz_ocxo.psd
xxx
pdcp PDx 10 100 30 0.000318 -225 1e3 10e6
cap C01 30 0 1e-6
cap C02 40 0 33e-6
cap C03 50 0 0.1e-6
cap C04 60 0 0.1e-6
res R01 30 40 510
res R02 30 50 1e3
res R03 50 60 1e3
xxx
vco2 VCOx 60 70 2500 100MHz_cvhd950.psd
splt SPLx 70 80 90
res Rxx 80 0 50
prb PRBx 80 Loop_Out
xxx
div DIVx 90 100 10 10 0 1000 -160
xxx
xxx
xxx 100MHz VCXO
xxx
src1 SRC1x 200 100MHz_cvhd950.psd
res Rxx 200 0 50
prb PRBx 200 VCXO_Alone
xxx
xxx Perfectly Multiplied OCXO
xxx
src1 SRC1x 300 10MHz_ocxo.psd
fmx FMXx 300 310 10 0 1 1
res Rxx 310 0 50
prb PRBx 310 MultipliedOCXO
xxx
fmin 10
fmax 10e6
npts 256
```

6 Appendix: ALC Background Material

6.1 160 MHz to 1344 MHz Voltage-Controlled Attenuator (RFSA2013)

The RFSA2013 attenuator operates from 50 MHz through 6 GHz and provides 30 dB of attenuation range. Its control characteristic is linear in dB. The device is very simple to use schematically so no additional explanation will be provided here.

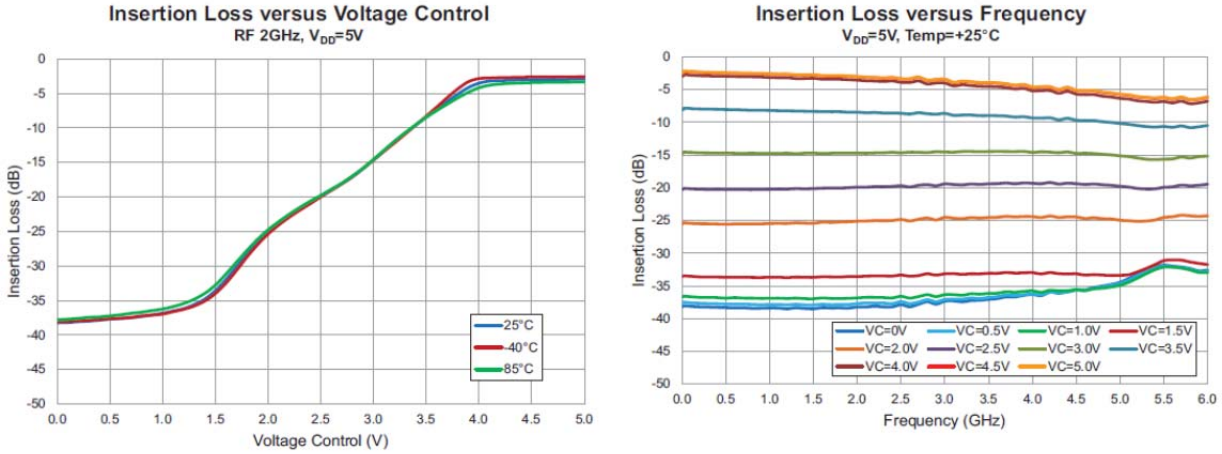


Figure 61 RFSA2013 attenuation characteristics

6.1.1 10 MHz to 160 MHz Variable Attenuator

The RFSA2013 voltage-controlled attenuator is only specified for operation down to 50 MHz, and consequently does not work down to 10 MHz. An alternative means for controlled attenuation needed to be found. In addition, many discrete devices are being discontinued by manufacturers like Avago/Broadcom thereby making old circuit designs less viable.

A number of attractive bridged-tee, pi-, and tee-attenuators using FET devices are disclosed in [6]. Since FET devices can provide controlled resistance even down to DC frequency, this attribute can be used to provide a controlled amount of attenuation while simultaneously delivering excellent input and output return loss. One of the disclosed circuits from [6] is shown in Figure 62 with two additional concepts shown in Figure 63. A complete replica circuit is not required in order to deliver excellent impedance matching, however, and one such concept is shown in Figure 64. To be viable, the attenuator-FETs must have a reasonably low on-resistance and their input/output capacitances must be appropriately small for the frequencies involved. For 160 MHz in a 50Ω system, these capacitances should ideally be less than roughly 5 pF and the on-resistance less than 10Ω.

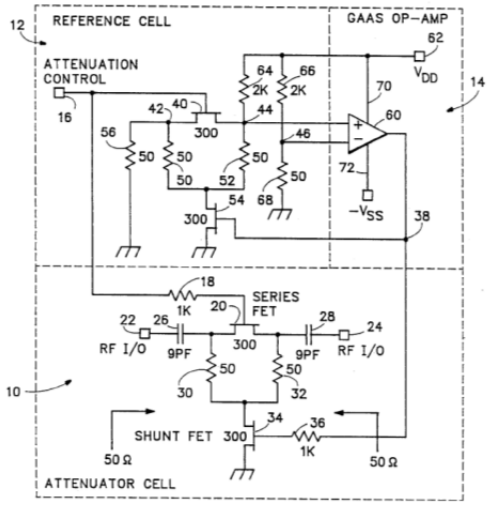


Figure 62 Bridged-tee variable attenuator from [6]

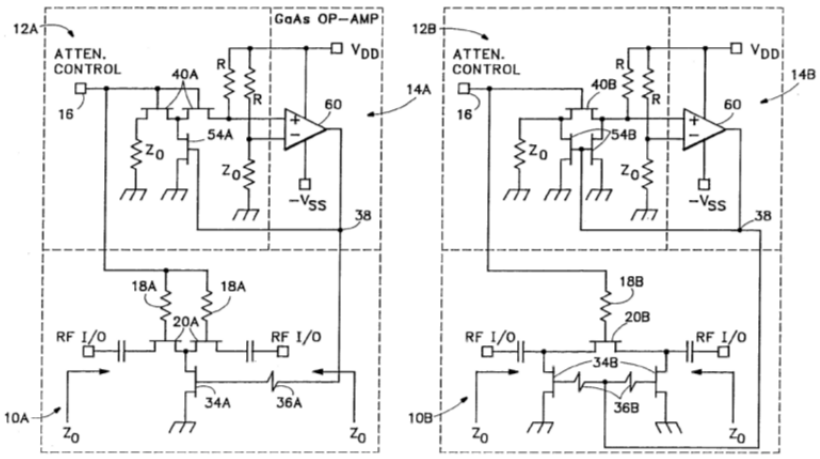


Figure 63 Pi- and tee-attenuator circuits from [6]

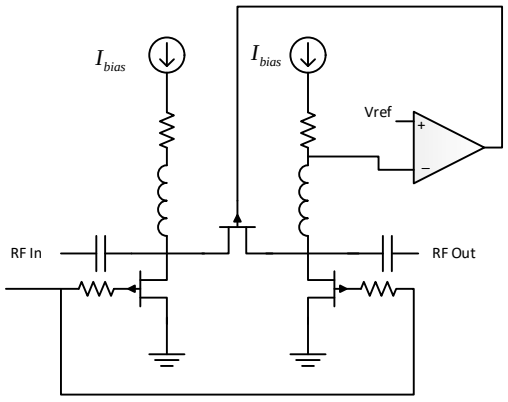
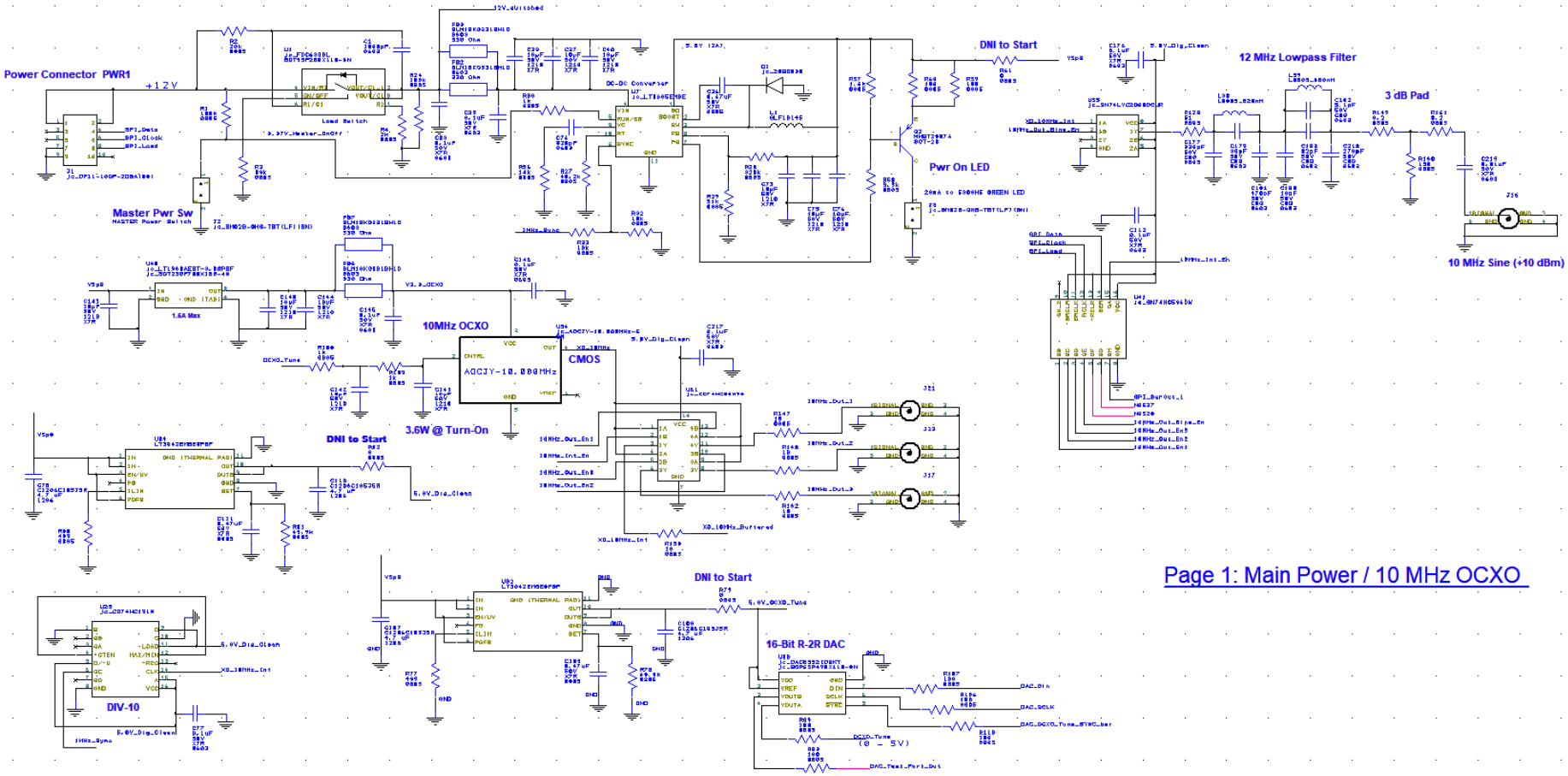


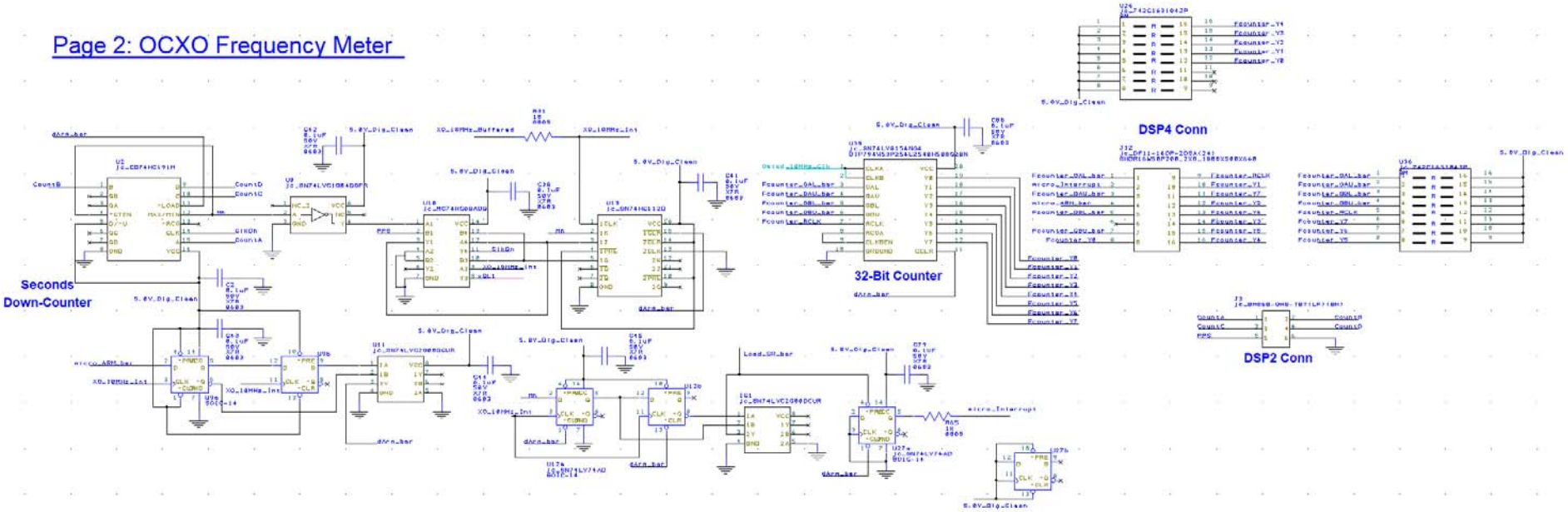
Figure 64 Automatic return loss optimization without necessitating a complete reference circuit

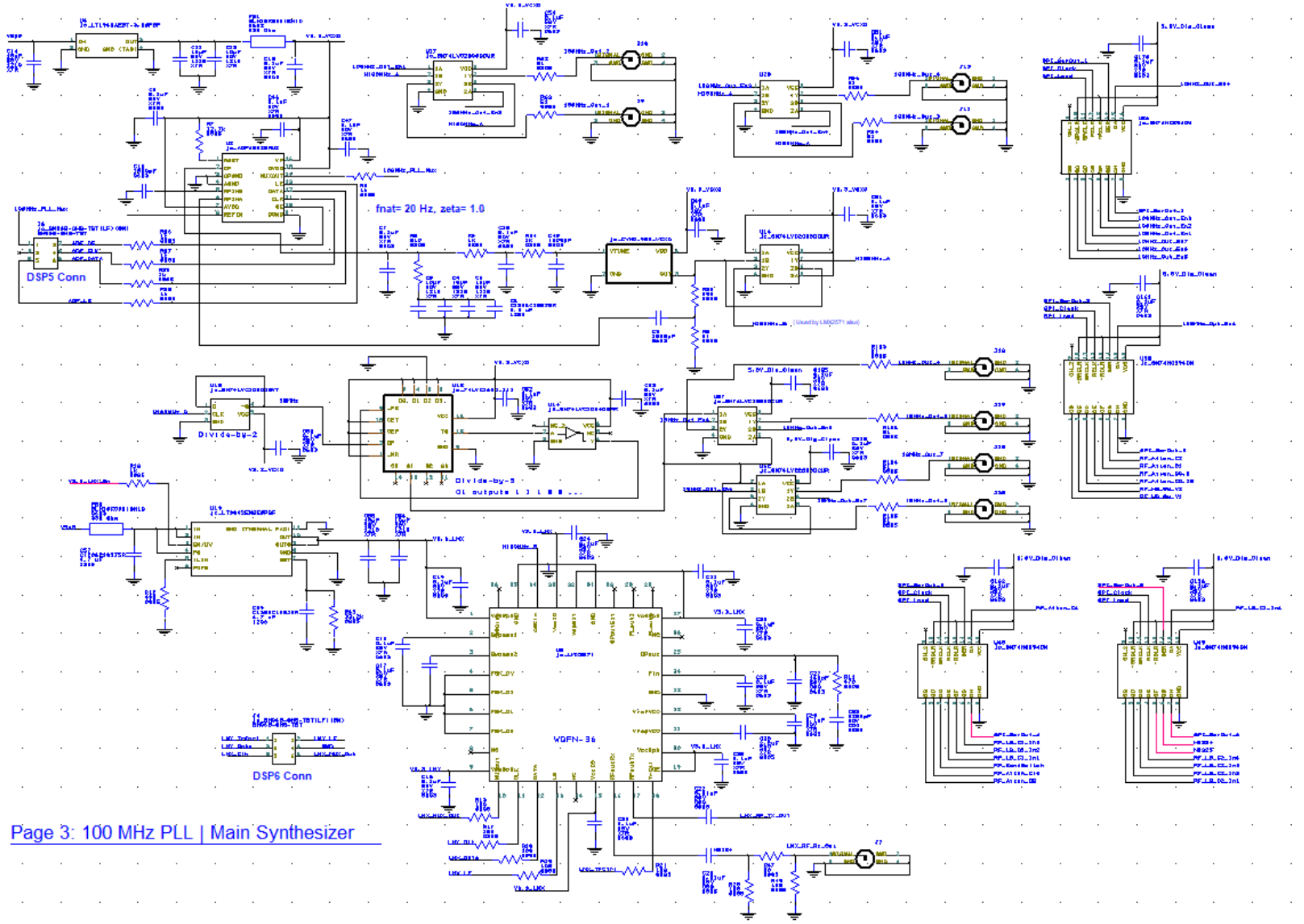
I do have quite a few HSMP-3814 and HSMP-3810 PIN diodes on hand, however. Otherwise, a quad-PIN diode pi-attenuator appears to still be active from NXP (BAP70Q) which is very attractive. A similar product (MA4P7455-1225) is available from MACOM.

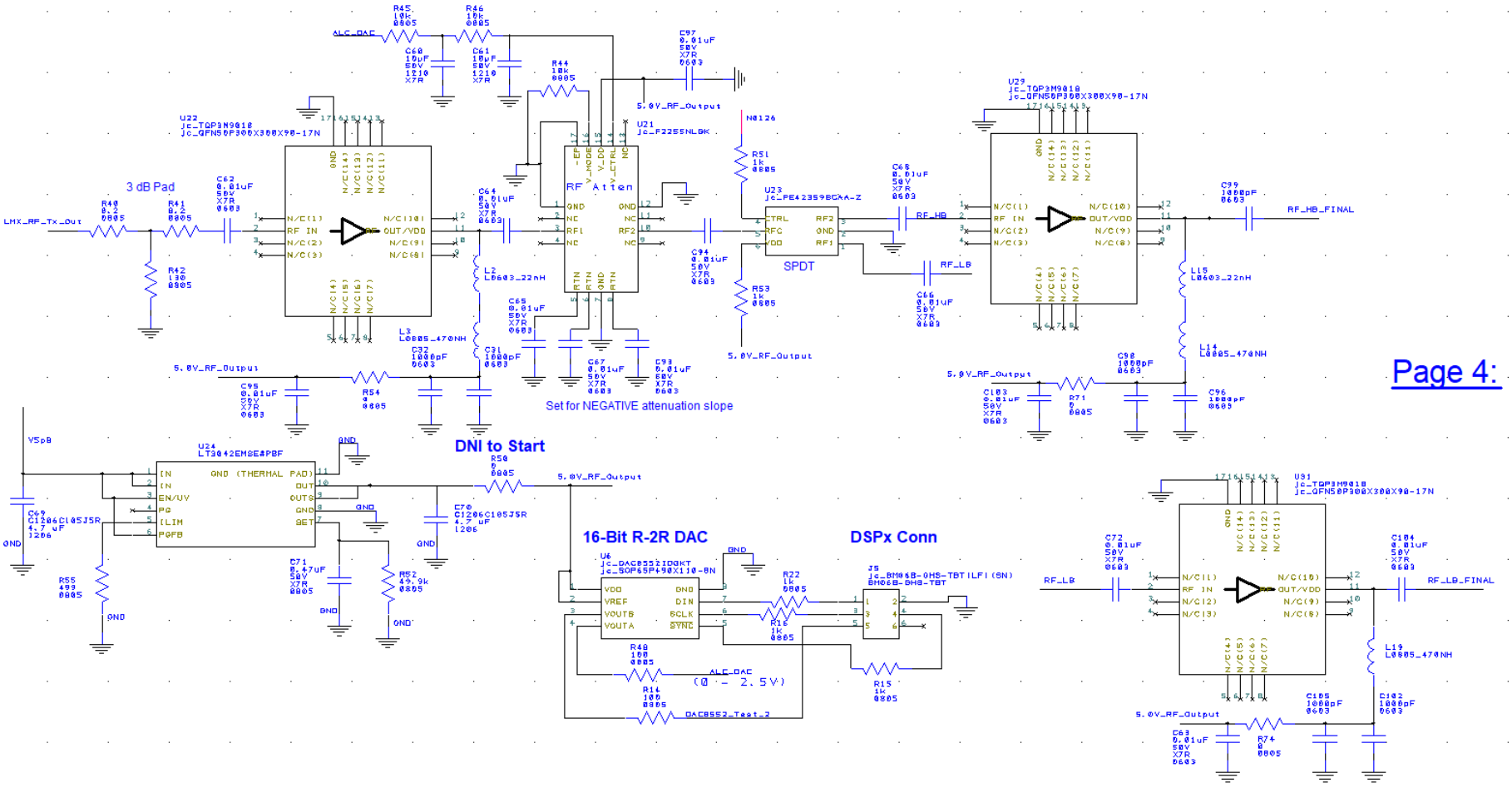
7 Appendix: Preliminary Schematics



Page 1: Main Power / 10 MHz OCXO

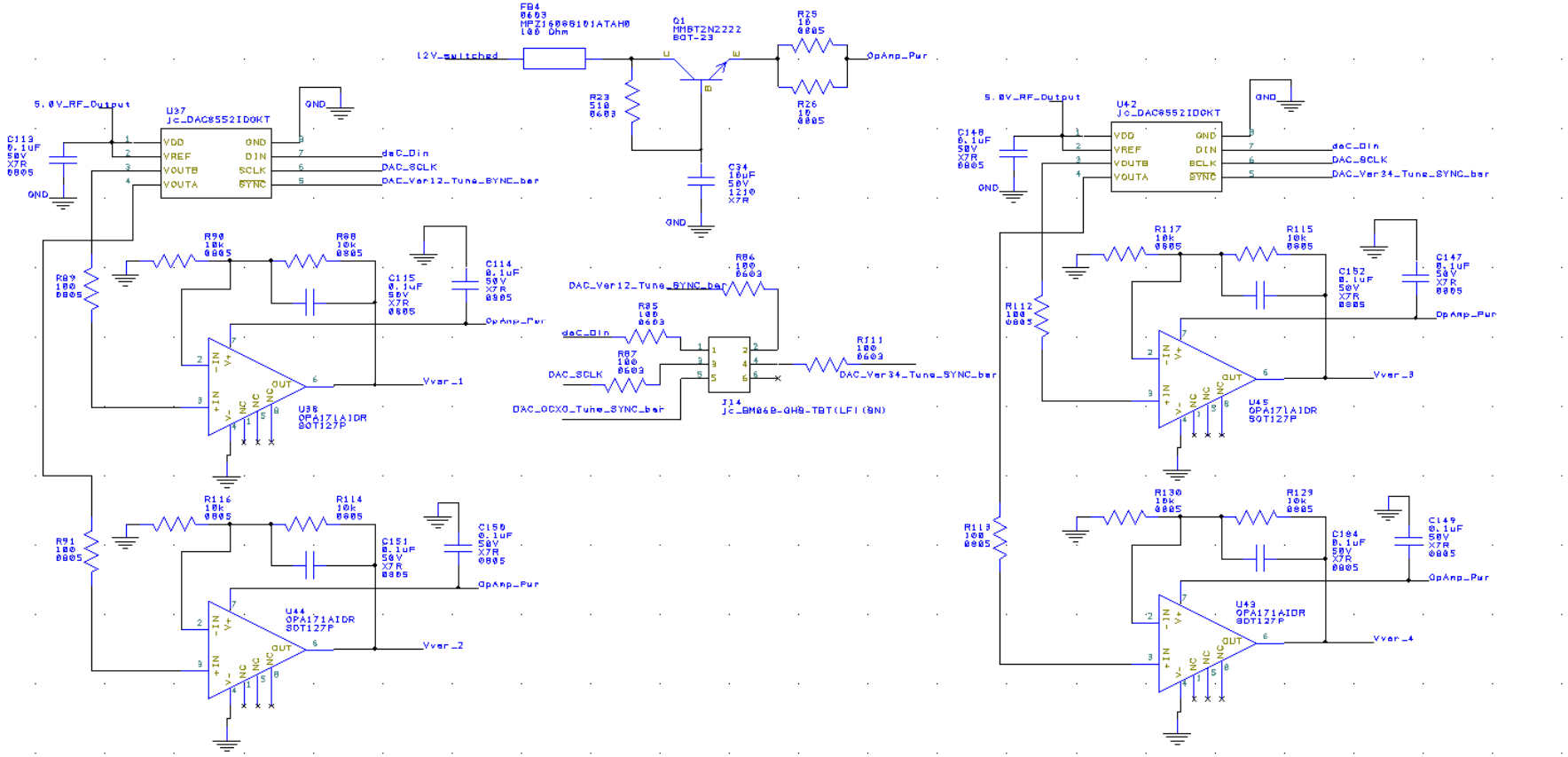

Page 2: OCXO Frequency Meter
Seconds
Down-Counter
32-Bit Counter
DSP4 Conn
DSP2 Conn

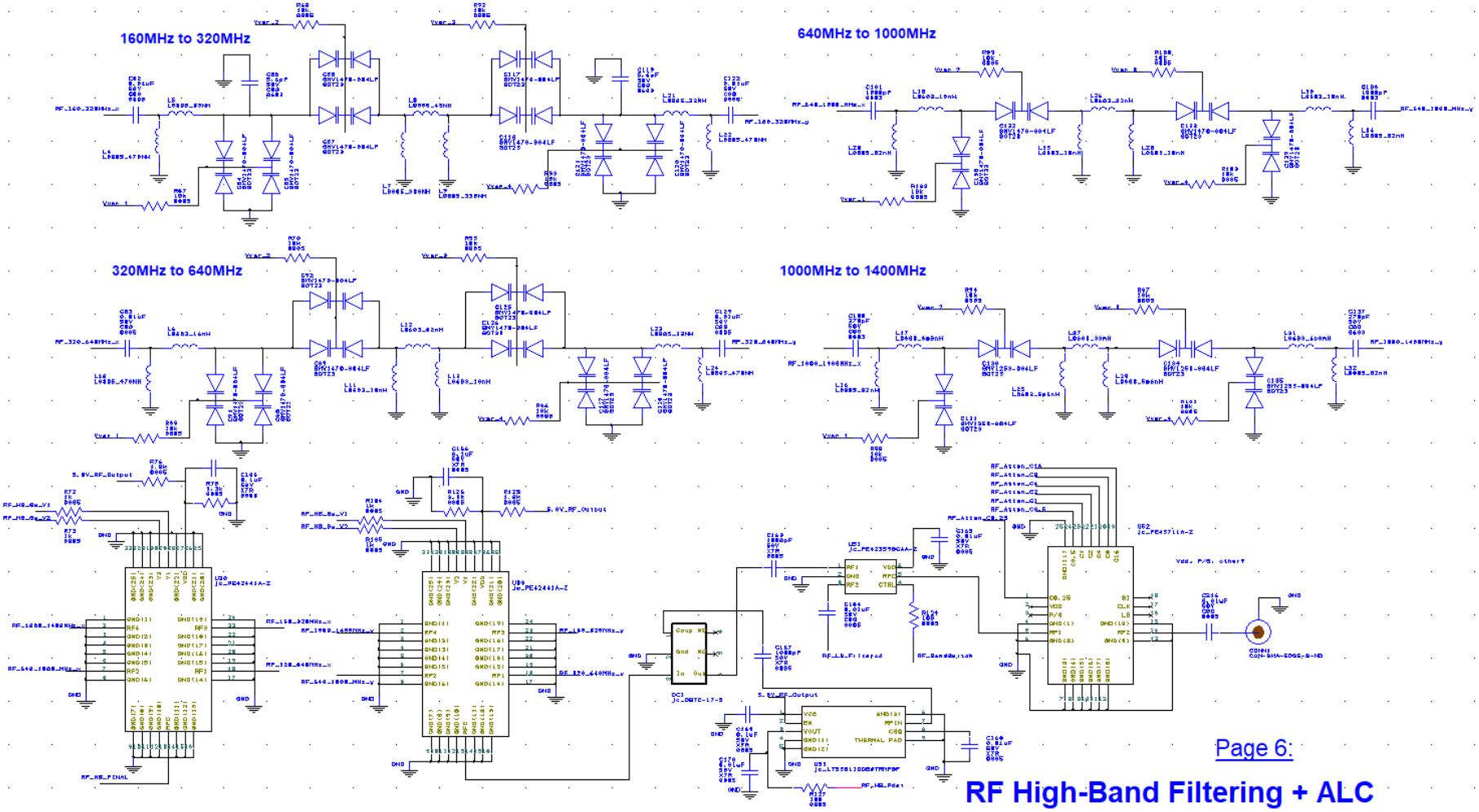

fnat= 20 Hz, zeta= 1.0
DSP5 Conn
Divide-by-2
Divide-by-5
WQFN-36
DSP6 Conn
Page 3: 100 MHz PLL | Main Synthesizer


3 dB Pad
RF Attn
SPDT
Set for NEGATIVE attenuation slope
DNI to Start
16-Bit R-2R DAC
DSPx Conn
Page 4:

Varactor Tune Voltage Generation

Page 5:

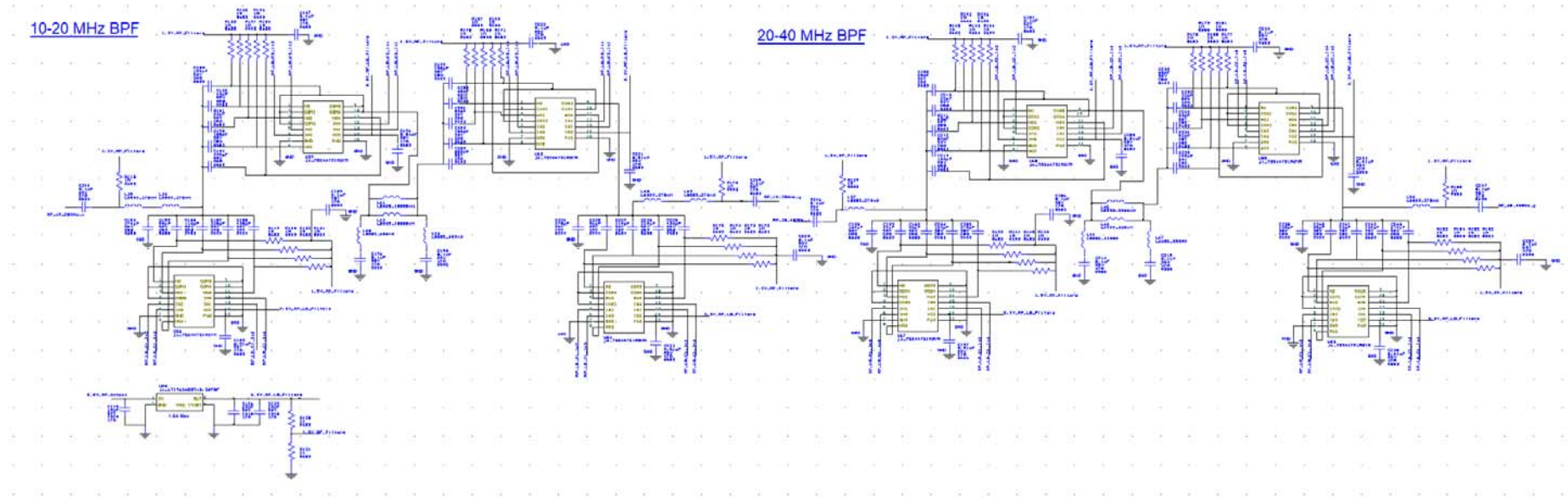


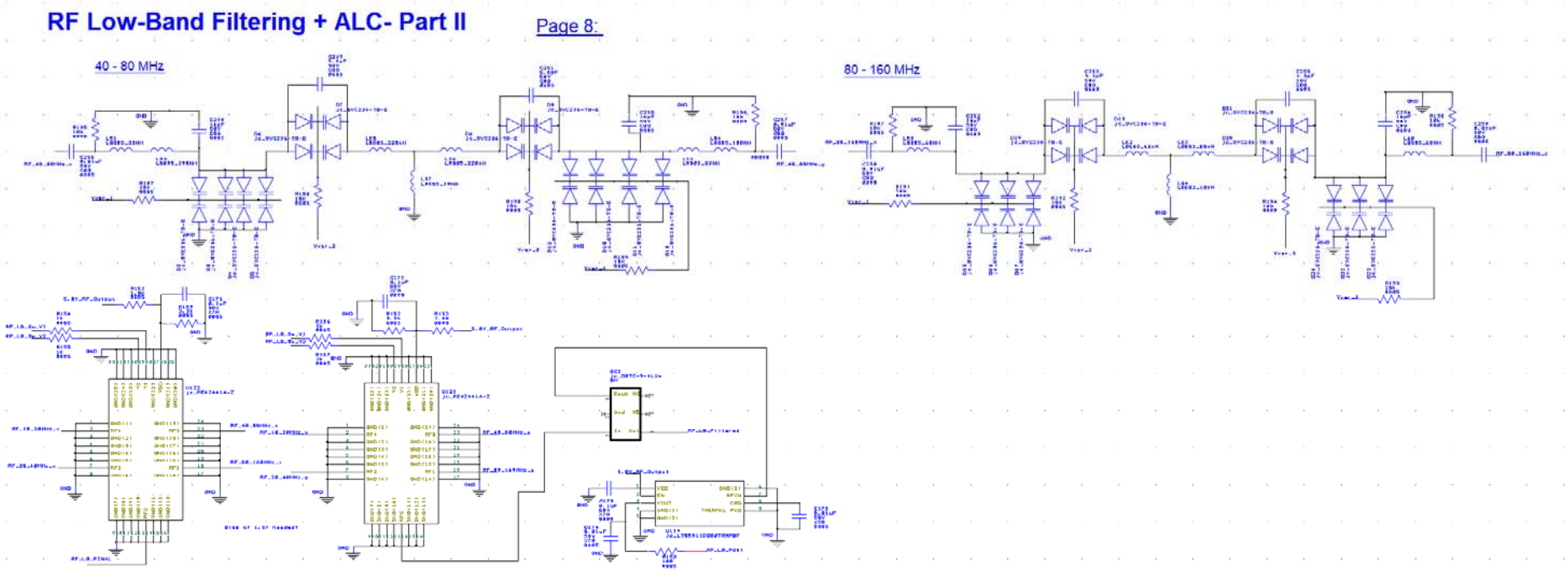


Page 6:

RF High-Band Filtering + ALC

RF Low-Band Filtering + ALC- Part I Page 7:




RF Low-Band Filtering + ALC- Part II
Page 8
40 - 80 MHz
80 - 160 MHz

Part III- Partial Listing

Algorithms
- Exact Frequency Tuning
- Frequency Locked Loop
- Automatic Level Control

Software
- Arduino
- C#

Performance Assessment
Final Schematics
Bill of Materials