Chapter 7

Appendix 7A: Additional Closed-Form Results for Sampled PLLs

Closed-loop results are provided for a number of additional PLL cases in the following sections. The same analysis techniques used in Section 7.6 are employed here.

7A.1 Type-1 with Inefficient Sample-Hold

The open-loop gain function for the continuous-time PLL is given by

$$G_{OL}(s) = \frac{K_d}{N}\frac{1-e^{-sT_s}}{sT_s}\left[\frac{\eta}{1-(1-\eta)e^{-sT_s}}\right]\frac{K_v}{s} \tag{7A.1}$$

where η is the sampling efficiency[1] of the sample-and-hold phase detector. The bracketed term in (7A.1) arises from the sampling inefficiency. The open-loop gain for the system with sampling can be expressed in *z*-transforms as

$$\begin{aligned} G_{OL}(z) &= \frac{K_d K_v}{N}\eta\frac{1-z^{-1}}{1-(1-\eta)z^{-1}}\mathbf{Z}\left(\frac{1}{s^2}\right) \\ &= \frac{\eta K_d K_v T_s}{N}\frac{z}{(z-1)(z-1+\eta)} \end{aligned} \tag{7A.2}$$

The frequency at which the phase of (7A.2) is $-\pi$ occurs for $\omega = \pi/T_s^{-1}$. This result combined with (7A.2) results in a system gain margin of

$$G_M = -20\log_{10}\left(\frac{K}{2}\right) + 20\log_{10}\left(\frac{2}{\eta}-1\right) \quad \text{dB} \tag{7A.3}$$

In this result, $K = K_d K_v T_s/N$ once more. The first term in (7A.3) is the gain margin for the ideal type-1 PLL case that was just considered in Section 7.6.1. The second term in this result is due to the inefficient sampling. The increase in system gain margin predicted by (7A.3) can be somewhat misleading because it really results from a decrease in the closed-loop bandwidth rather than a real improvement in the system stability. If the gain margin analysis is performed while keeping the closed-loop bandwidth constant, this apparent improvement will be lost.

[1] See [1] for additional details about this phase detector type.

The phase margin result is considerably more complex to compute. First of all, the open-loop unity-gain frequency ω_u must be found. It is given by

$$\omega_u = \frac{1}{T_s}\cos^{-1}(x) \tag{7A.4}$$

where x is the admissible solution (i.e., $|x| < 1$) of

$$x^2 - \frac{4(1-\eta)+2+2(1-\eta)^2}{4(1-\eta)}x + \frac{2+2(1-\eta)^2-\gamma^2}{4(1-\eta)} = 0 \tag{7A.5}$$

The parameter γ is given by $\gamma = K\eta = K_d K_v T_s \eta \quad /N$. Once the solution x has been found, the phase margin is given by

$$\varphi_M = \frac{\pi}{2} + \frac{1}{2}\cos^{-1}(x) - \tan^{-1}\left(\frac{\sqrt{1-x^2}}{x+\eta-1}\right) \tag{7A.6}$$

The phase margin versus bandwidth parameter K and sampling efficiency η is shown plotted in Figure 7A-1.

The transient output phase error response of the system to a step change in output frequency can be found using z-transforms as discussed in Section 7.5. The z-transform of the error response is given by

$$\begin{aligned}\varphi_e(z) &= 2\pi\Delta F \frac{T_s z}{(z-1)^2}\frac{1}{1+\dfrac{\gamma z}{(z-1)(z+\eta-1)}} \\ &= 2\pi\Delta F\, T_s \frac{z(z+\eta-1)}{z^3+z^2(\gamma+\eta-3)+z(3-\gamma-2\eta)+(\eta-1)}\end{aligned} \tag{7A.7}$$

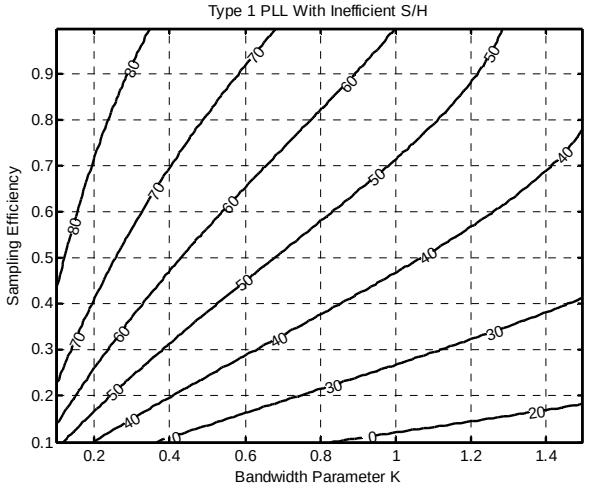

Figure 7A-1 Phase margin for the inefficient type-1 sampled PLL.[2]

[2] Book CD:\Ch7\u12686_ch7_ineff_type1_pll.m.

Repeated long-hand division of (7A.7) easily produces the example transient error responses shown in Figure 7A-2. All of the cases shown there are for $K = 1$ with a range of sampling efficiency values.

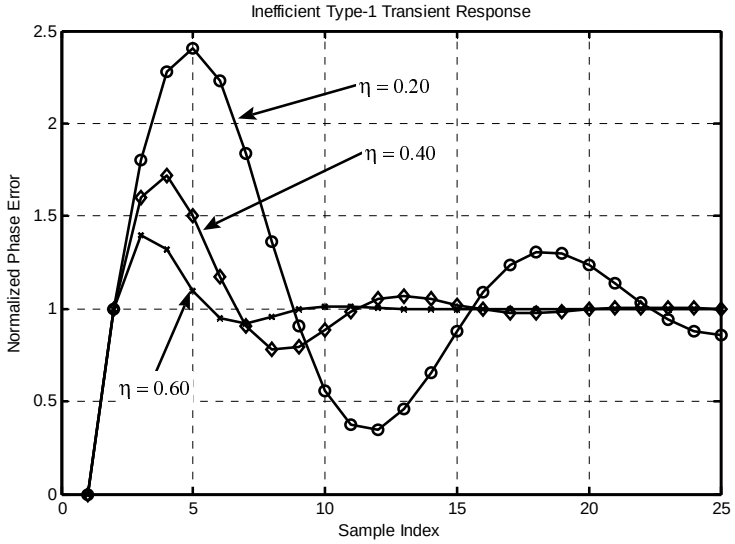

Figure 7A-2 Transient error responses for the inefficient type-1 sampled PLL[3] ($K = 1$ for all).

7A.2 Type-1 with Sample-Hold and Internal Time Delay

The open-loop gain function for this continuous-time PLL is given by

$$G_{OL}(s) = \frac{K_d}{N}\frac{1-e^{-sT_s}}{sT_s}\frac{K_v}{s}e^{-s\tau_d} \tag{7A.8}$$

The explicit time-delay is included by using the $\exp(-s\tau_d)$ term. If the time delay is greater than T_s, it is necessary to separate the term into a product of terms like $\exp(-snT_s)\exp(-s\tau_r)$ such that $\tau_d = nT_s + \tau_r$. It is assumed that $n = 0$ for the material that follows. Modified z-transforms are required to deal with the presence of τ_d. The open-loop gain function is given by

$$\begin{aligned} G_{OL}(z) &= \frac{K_d K_v}{N}\left(1-z^{-1}\right)\mathbf{Z}_m\left(\frac{1}{s^2}\right) \\ &= \frac{K_d K_v T_s}{N}\frac{mz+(1-m)}{z-1}z^{-1} \end{aligned} \tag{7A.9}$$

where $m = 1 - \tau_d/T_s$ and it is assumed that $\tau_d < T_s$. (Additional factors of z^{-1} can be appended to (7A.9) as required to avert this limitation.) The frequency at which the open-loop gain equals $-\pi$ is given by

[3] Book CD:\Ch7\u12686_ch7_ineff_type1_pll.m.

$$\omega_\pi = \frac{1}{T_s}\begin{cases} \pi & \text{for } 0 \le \dfrac{\tau_d}{T_s} \le \dfrac{1}{4} \\ 2\cos^{-1}\left(\sqrt{1-\dfrac{T_s}{4\tau_d}}\right) & \text{for } \dfrac{1}{4} < \dfrac{\tau_d}{T_s} \le 1 \end{cases} \tag{7A.10}$$

With this result, the gain margin for this system is given by

$$G_M = -20\log_{10}\left(\frac{K}{2}\right) - 20\log_{10}\left(1-\frac{2\tau_d}{T_s}\right) \qquad \text{for } 0 \le \frac{\tau_d}{T_s} \le \frac{1}{4} \tag{7A.11}$$

$$G_M = -20\log_{10}\left[\frac{K}{2\sin\left(\omega_\pi T_s/2\right)}\right] - 10\log_{10}\begin{Bmatrix}\left[m\cos\left(\omega_\pi T_s\right)+1-m\right]^2 + \\ m^2\sin^2\left(\omega_\pi T_s\right)\end{Bmatrix} \qquad \text{for } \frac{1}{4} \le \frac{\tau_d}{T_s} \le 1 \tag{7A.12}$$

This is a particularly interesting result because the first term in the result corresponds to the gain margin of an ideal type-1 PLL whereas the second term is due to the internal time-delay alone. Gain margin contours using these results are provided in Figure 7A-3.

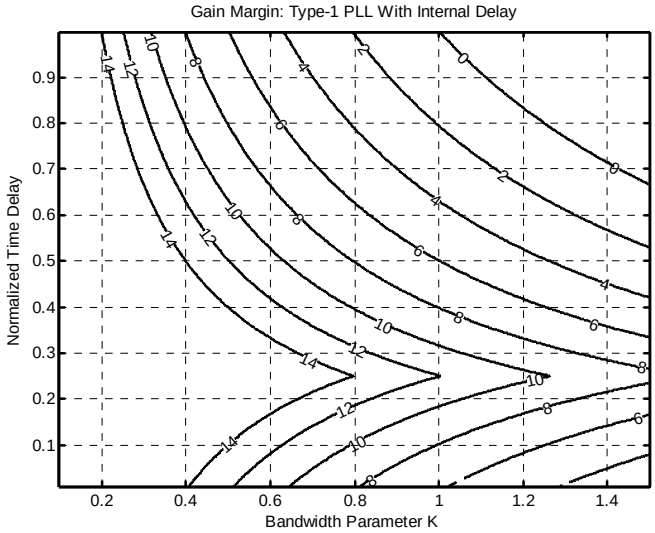

Figure 7A-3 Gain margin for the type-1 PLL with internal time delay.[4]

The system phase margin calculation requires the normal calculation of the unity-gain frequency. In this case, the frequency corresponds to the value of *z* that satisfies

$$\left|K\frac{mz+(1-m)}{z-1}\right| = 1 \tag{7A.13}$$

[4] Book CD:\Ch7\u14044_ch7_type1_pll_delay.m.

The unity-gain frequency that results is

$$\omega_u = \frac{1}{T_s}\cos^{-1}\left[\frac{2-K^2\left(2m^2-2m+1\right)}{2+2K^2m\left(1-m\right)}\right] \tag{7A.14}$$

and the corresponding system phase margin is then given by

$$\varphi_M = \frac{\pi}{2}-\frac{3}{2}\omega_u T_s + \tan^{-1}\left[\frac{m\sin\left(\omega_u T_s\right)}{m\cos\left(\omega_u T_s\right)+1-m}\right] \tag{7A.15}$$

The system phase margin (7A.15) is only defined for situations in which the system gain margin is greater than 0 dB. Phase margin contours for this case are plotted in Figure 7A-4.

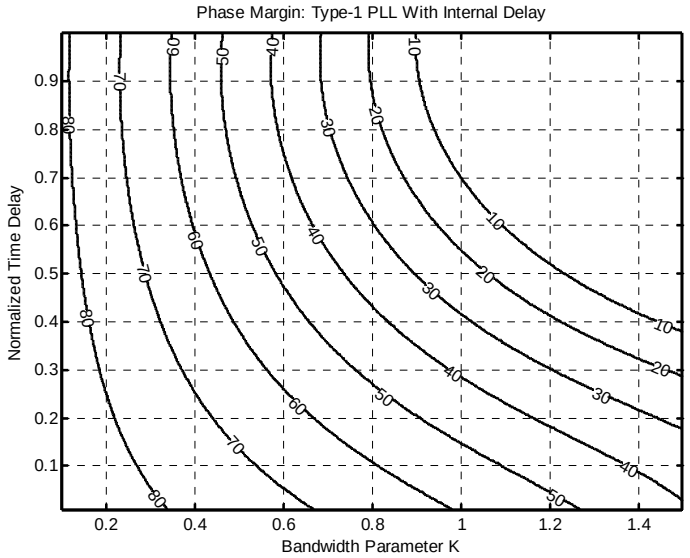

Figure 7A-4 Phase margin for the type-1 PLL with internal time delay.[5]

The transient output phase error response of this system to a step change in output frequency is given by

$$\varphi_e\left(z\right) = 2\pi\Delta f\, T_s \frac{z^2}{z^3+z^2\left(Km-2\right)+z\left[K\left(1-2m\right)+1\right]-K\left(1-m\right)} \tag{7A.16}$$

This response is plotted for several time-delay values in Figure 7A-5. For the speed-optimized case (K = 1), the oscillatory behavior clearly becomes severe as the delay approaches one sample-time T_s. In general, stability margins are more frail when the design parameters have been optimized for speed. Improved transient performance can be achieved when τ_d is nonzero by reducing the loop gain parameter K.

[5] Book CD:\Ch7\u14044_ch7_type1_pll_delay.m.

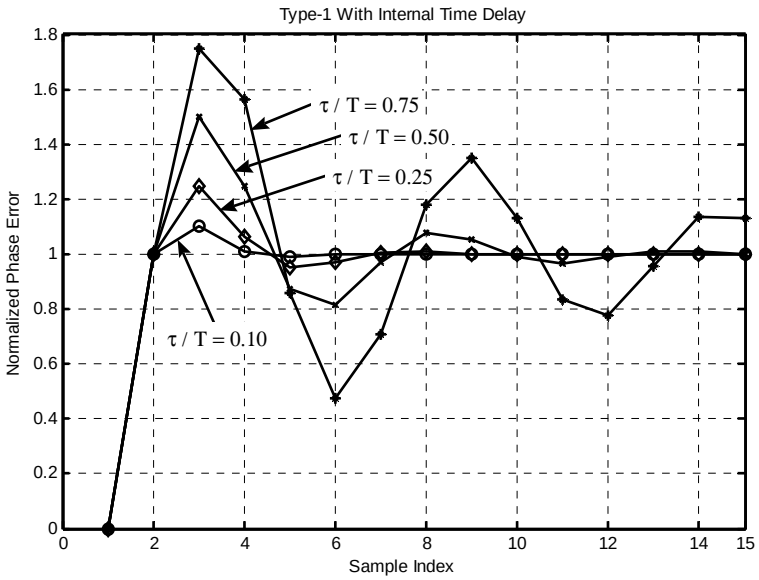

Figure 7A-5 Transient error responses for the type-1 sampled PLL with internal time delay (K = 1 for all).[6]

7A.3 Type-2 PLL with Inefficeint Sample-Hold

The open-loop gain function for the continuous-time PLL is given by

$$G_{OL}(s) = \frac{K_d}{N}\frac{1-e^{-sT_s}}{sT_s}\left[\frac{\eta}{1-(1-\eta)e^{-sT_s}}\right]\frac{1+s\tau_2}{s\tau_1}\frac{K_v}{s} \tag{7A.17}$$

The portion of $G_{OL}(s)$ attributed to the inefficiency of the sample-and-hold phase detector is shown in brackets in (7A.17). The z-transform corresponding to (7A.17) is given by

$$G_{OL}(z) = (\omega_n T_s)^2 \frac{\eta z}{z-(1-\eta)} \frac{z\left(\frac{1}{2}+\frac{2\zeta}{\omega_n T_s}\right)+\left(\frac{1}{2}-\frac{2\zeta}{\omega_n T_s}\right)}{(z-1)^2} \tag{7A.18}$$

It can be shown that the system gain margin is given by

$$G_M = -20\log_{10}(\zeta\omega_n T_s) + 20\log_{10}\left(\frac{2}{\eta}-1\right) \tag{7A.19}$$

so long as

$$\zeta > \frac{\omega_n T_s}{4}\left(\frac{2}{\eta}-1\right) \tag{7A.20}$$

[6] Book CD:\Ch7\u14044_ch7_type1_pll_delay.m.

This is a concise result for the system gain margin, and simply related to the result found for the ideal type 2 PLL (7.48).

The phase margin for the system does not lend itself to a simple closed-form solution.

References

[1] Crawford, J.A., “Advanced Phase-Lock Techniques Applied,” working papers, unpublished.