Chapter 6

Appendix 6D: Admittance Matrix Methods for Analyzing Complex Loop Filters

6D.1 Admittance Matrix Formulation

Linear network analysis using admittance matrices was used in Chapter 8 of [1] as the basis for a general PLL analysis program. The PLL design tool mentioned near the end of Section 6.7 makes use of this same analysis approach. A very brief introduction to the admittance matrix method is provided in this appendix.

In general, the loop filter of a PLL will consist of a circuit like Figure 6D.1 that can be described with a nodal-based data description. Each data entry consists of the component type, the circuit nodes that it is connected to, and component values and/or parameters. Without loss of generality, it will be assumed that node "0" corresponds to ground and that all other nodes in the schematic are sequentially indexed.

Assume that the linear network portion of the loop filter is represented by $H(\omega)$ and that the network is described by the admittance description

$$[I] = [Y][V] \tag{6D.1}$$

where Y is a complex admittance matrix, V is the vector of circuit node voltages, and I is the vector of external current inputs at each network node. In the general case, all of the node voltages in (6D.1) must be computed.

In general, this is not necessary in order to compute $H(\omega)$ since it represents a single-input/single-output transfer function. In this special case, it can be advantageous to use floating admittance matrix concepts [2] and reduce the $N \times N$ admittance matrix to an equivalent 2×2 matrix retaining only the input and output nodes as the network ports. This method is based on a generalization of Kirchhoff's current law in which the datum node voltage (which is normally taken as node zero) is included in the matrix equation formulation. The simple example using Figure 6D.1 illustrates this computational technique.

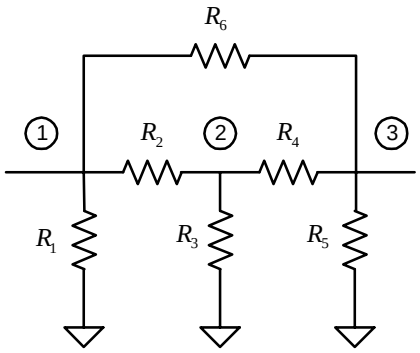

Figure 6D.1 Simple resistive network for illustrating floating-admittance matrix concept.

The floating-admittance matrix description for (6D.2) is given by

$$Y = \begin{bmatrix} G_1+G_3+G_5 & -G_1 & -G_3 & -G_5 \\ -G_1 & G_1+G_2+G_6 & -G_2 & -G_6 \\ -G_3 & -G_2 & G_2+G_3+G_4 & -G_4 \\ -G_5 & -G_6 & -G_4 & G_4+G_5+G_6 \end{bmatrix} \tag{6D.2}$$

where each conductance is given by $G_i = R_i^{-1}$. Unlike the more typical admittance matrix used, the datum node (i.e., ground node) has been retained in (6D.2) making Y a "floating" or indefinite admittance matrix. Each row and each column of Y must individually sum to zero as a direct result of Kirchhoff's current law. This fact may be used to reduce the dimensions of Y by eliminating embedded network nodes whose explicit solutions are not required.

To further this discussion, equation (6D.1) may be rewritten as

$$\begin{bmatrix} I_0 \\ I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} g_{00} & g_{01} & g_{02} & g_{03} \\ g_{10} & g_{11} & g_{12} & g_{13} \\ g_{20} & g_{21} & g_{22} & g_{23} \\ g_{30} & g_{31} & g_{32} & g_{33} \end{bmatrix} \begin{bmatrix} V_0 \\ V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{6D.3}$$

Assume now that node 2 is an internal inaccessible node and it is to be eliminated from any explicit appearance in (6D.3). From the matrix equation for node 2 in (6D.3),

$$\begin{aligned} & g_{20}V_0 + g_{21}V_1 + g_{22}V_2 + g_{23}V_3 = I_2 = 0 \\ \therefore \quad & V_2 = -\frac{1}{g_{22}}\left[g_{20}V_0 + g_{21}V_1 + g_{23}V_3 \right] \end{aligned} \tag{6D.4}$$

Substituting this result into (6D.3), the reduced matrix description for the network is given by

$$\begin{bmatrix} I_0 \\ I_1 \\ I_3 \end{bmatrix} = \begin{bmatrix} \left(g_{00} - \frac{g_{02}g_{20}}{g_{22}}\right) & \left(g_{01} - \frac{g_{02}g_{21}}{g_{22}}\right) & \left(g_{03} - \frac{g_{02}g_{23}}{g_{22}}\right) \\ \left(g_{10} - \frac{g_{12}g_{20}}{g_{22}}\right) & \left(g_{11} - \frac{g_{12}g_{21}}{g_{22}}\right) & \left(g_{13} - \frac{g_{12}g_{23}}{g_{22}}\right) \\ \left(g_{30} - \frac{g_{32}g_{20}}{g_{22}}\right) & \left(g_{31} - \frac{g_{32}g_{21}}{g_{22}}\right) & \left(g_{33} - \frac{g_{32}g_{23}}{g_{22}}\right) \end{bmatrix} \begin{bmatrix} V_0 \\ V_1 \\ V_3 \end{bmatrix} \tag{6D.5}$$

which is itself a floating admittance matrix. For larger networks, this node elimination method may be used repeatedly as necessary to reduce the network description to an equivalent *m*-port. Ignoring the datum node in (6D.5) by setting $V_0 = 0$, the final 2×2 admittance matrix for this example is given as

$$\begin{bmatrix} \left(g_{11} - \frac{g_{12}g_{21}}{g_{22}}\right) & \left(g_{13} - \frac{g_{12}g_{23}}{g_{22}}\right) \\ \left(g_{31} - \frac{g_{32}g_{21}}{g_{22}}\right) & \left(g_{33} - \frac{g_{32}g_{23}}{g_{22}}\right) \end{bmatrix} \tag{6D.6}$$

References

[1] Crawford, J.A., *Frequency Synthesizer Design Handbook*, Norwood, MA: Artech House, 1994.

[2] Daruvala, D.J., "Unify Two-Port Calculations with a Single Analysis Technique- the Indefinite Matrix," *Electronic Design*, Vol. 1, January 1974, pp. 112-116.