

Title:	<i>Phase Noise Analysis Tool</i>
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Abstract:	Phase noise analysis becomes rather tedious when systems get complicated. This is particularly true with coherence factors need to be included. This tool makes it possible to analyze any general architecture in a straight-forward manner.
Date:	19 Sept 2014
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1 Introduction

Facing completely arbitrary and fairly complicated RF system topologies, an improved tool for phase noise calculation is needed. The spreadsheet route is fine for a fixed topology, but facing ever-changing topologies during the inevitable *what if* engineering design phase is very painful. The tool described herein reduces the problem to extracting a Spice-like netlist for the system to be analyzed and the required phase noise analysis follows directly using the phase noise analysis tool described herein. The tool is basically an expansion of the MATLAB tool presented in Chapter 4 of [9], but written in C#.

A generic example illustrates the capabilities of this tool quickly. Consider the fairly complicated RF system shown in Figure 1. A spreadsheet-based analysis of this system would be quite painful, especially if coherency issues between the different internal LOs had to be included precisely. The phase noise tool described herein makes the analysis of even complicated RF systems like this fairly straight forward.

The first step involved with analyzing Figure 1 is to assign node numbers to assist with topology entry into the tool like that shown in Figure 2. The numbering sequence is fairly arbitrary as shown in this example. All of the available modeling blocks and their entry syntax are described in §3 and these are used to describe the RF system in detail.

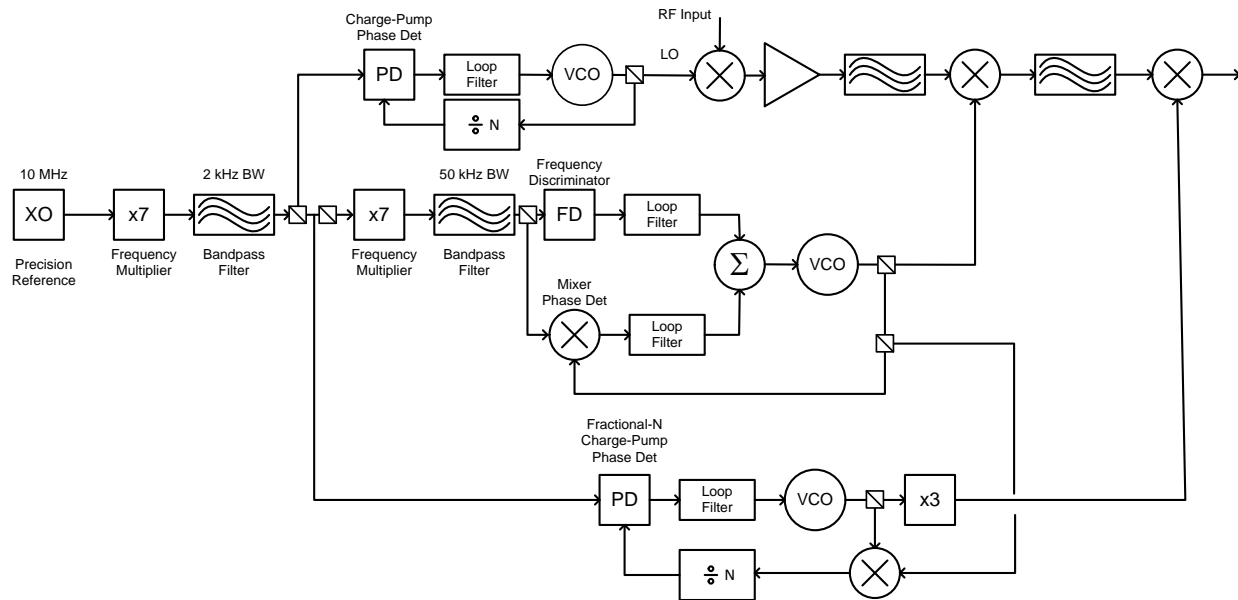


Figure 1 Complicated RF system example

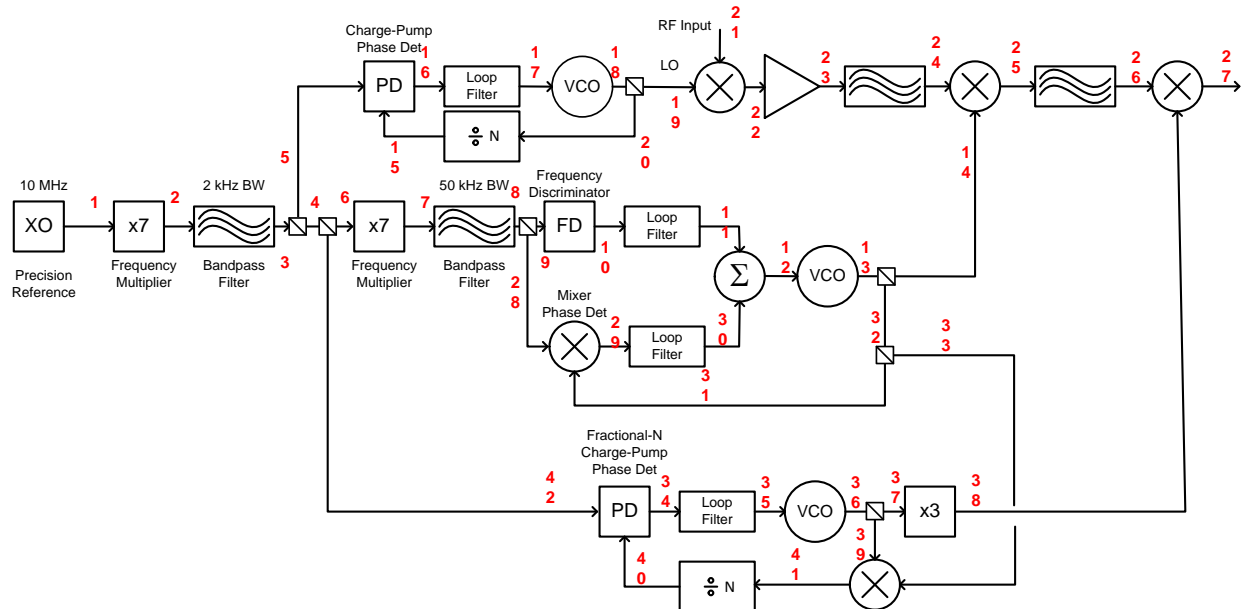


Figure 2 Node numbers added to Figure 1. Node-numbering does not need to be sequential which makes it easy to add/subtract/modify the design later.

The circuit parameter file associated with Figure 2 would begin as shown below:

```

xxx
xxx
fmin 1
fmax 1e6
Npts 4096
xxx
src1 SRC1_XO_Ref 1 xo.psd
fmx FMX_01 1 2 7 0 5 1e3
fil FIL_01 2 3 1e3 5 70 0 0.001 2
spl SPL_01 3 4 5
spl SPL_02 4 42 6
fmx FMX_700MHz 6 7 7 0 8 1e3
fil FIL_02 7 8 0 7 60 5 2e-6 3
spl SPL_03 8 28 9
xxx
xxx Bottom PLL
xxx
pdcp PD_01 42 40 34 0.50 -215 2e3 70e6
divf DIV_01 41 40 43 20 3 200 -155 3 70e6
...
...
    
```

1.1 Real Example #1: Single-Loop PLL

The first example is for the single PLL shown in Figure 3. The associated input file for this example is given in Figure 4. Phase noise analysis results are shown in Figure 5.

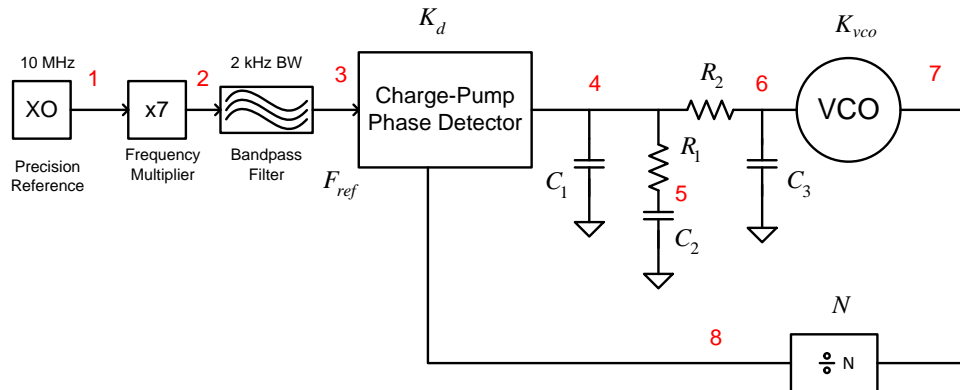


Figure 3 Example #1: single PLL. Simplified example showing numbered nodes. $K_v = 20$ MHz/V, $K_d = 0.000318$ A/rad, $N = 20$, loop natural frequency ≈ 50 kHz, loop damping factor ≈ 0.707 .

```

xxx    PN Tool Test #1
xxx    28 Feb 2012
xxx    J.A. Crawford
xxx
//
//
fmin   10
fmax   10e6
Npts   512
src1   SRC1 1  fref.psd
fmx    FMX01 1 2 7 10 5 1e3
fil    FIL01 2 3 1e3 6 70 10.0 5e-6 1.5
pdcp   PD01 3 8 4 0.000318 -216 2e3 70e6
cap    C01 4 0 470e-12
res    R01 4 5 222
cap    C02 5 0 20.26e-9
res    R02 4 6 1e3
cap    C03 6 0 160e-12
vco1   VCO1 6 7 20e6 3 0 1400e6 10 1e3
div    DIV1 7 8 20 20 10 2000 -150
prb    PRB01 1  Ref-source-output
prb    PRB02 2  At multiplier output
prb    PRB03 3  Fref-at-PD-Input
prb    PRB04 7  VCO-Output
prb    PRB05 8  Div-N-Output

```

Figure 4 pntool_test1.prm file listing for schematic shown in Figure 3.

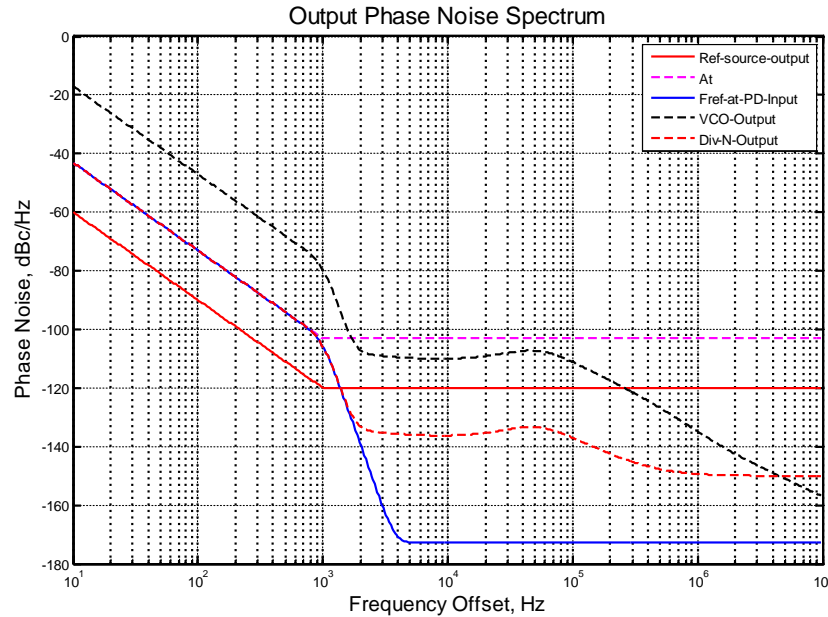


Figure 5 Phase noise analysis results for example 1

1.2 Real Example #2: Expanded Single-Loop PLL

An expanded version of the PLL which includes a 3rd-order elliptic lowpass filter is shown in Figure 6 and the associated parameter file listing provided in Figure 7. The phase noise analysis results are shown in Figure 6.

The top-5 noise sources with the greatest excursion above the spectral mask are plotted along with the mask itself as shown in Figure 9. These results clearly show that the charge-pump phase detector’s noise floor is the primary factor in the output spectrum exceeding the desired design goals.

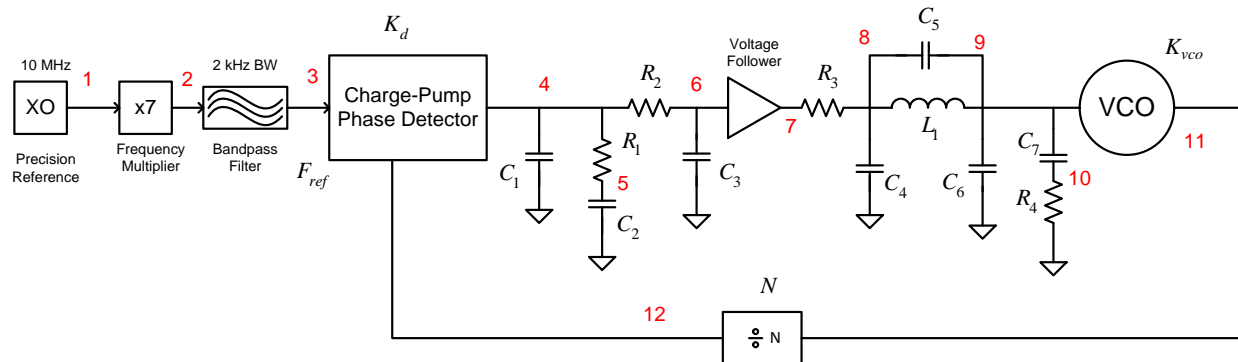


Figure 6 Example #2: single PLL. Simplified example showing numbered nodes. $K_v = 40$ MHz/V, $K_d = 0.000318$ A/rad, $N = 20$, loop natural frequency ≈ 50 kHz, loop damping factor ≈ 0.707 , 3rd-order elliptic filter with ripple bandwidth of 500 kHz, $\rho = 20\%$, $\theta = 15^\circ$.

```

xxx
xxx  PN Tool Example 2
xxx  10 May 2012
xxx  J.A. Crawford
xxx
fmin 10
fmax 10e6
npts 512
xxx
src1 SRC1 1 fref.psd
fmx FMXx 1 2 7 0 5 100
fil FILx 2 3 1e3 5 70 0 0.001 2
pdcp PDx 3 12 4 0.000318 -215 1e3 70e6
cap C01 4 0 470e-12
res R01 4 5 222
cap C02 5 0 20.26e-9
res R02 4 6 1e3
cap C03 6 0 160e-12
xxx
xxx Elliptic LPF, Fc=500 kHz, rho= 20% theta= 15 degrees
xxx
vbuf VBUFx 6 7
res R03 7 8 100
cap C04 8 0 3.68e-9
cap C05 8 9 146e-12
cap C06 9 0 3.68e-9
ind L01 8 9 35.2e-6
cap C07 9 10 10e-6
res R04 10 0 100
xxx
vco1 VCOx 9 11 40e6 3 0 1400e6 20 1e3
div DIVx 11 12 20 20 10 2000 -150
xxx
prb PRB01 3 Fref_at_PD_Input
prb PRB02 11 VCO_Output
prb PRB03 12 DivN_Output

```

Figure 7 pntool_test2.prm file listing for Figure 6

In Figure 9, the tight bandpass filtering be seen cutting in at 1 kHz offset. If the y-axis scale is extended lower, the elliptic lowpass filter can be seen reducing the phase detector and loop filter noise as well. The output noise floor of the divider was set to -150 dBc/Hz in the parameter file and with the divide-by-20 in the feedback loop, this floor is effectively increased to -124 dBc/Hz at the VCO output as shown. The *line 22* resistor entry (R03) corresponds to the 100Ω resistor immediately following the voltage buffer preceding the VCO. Its associated open-circuit Nyquist noise voltage density is about 1.27 nV RMS $\text{Hz}^{-0.50}$ and when combined with the VCO's effective tuning sensitivity of 20 MHz/V, its phase noise contribution at the loop bandwidth edge (taken to be the 1.5 x natural frequency here or 75 kHz) of is expected to be

$$\mathcal{L} \approx 20 \log_{10} \left(\frac{v_{res} \sqrt{2} \times 20 \text{MHz}}{2 \times 75 \text{kHz}} \right) = -132.5 \text{ dBc/Hz} \quad (1)$$

The maximum value shown in the figure is larger (about -128.6 dBc/Hz) due to the additional gain-peaking caused by the PLL action.

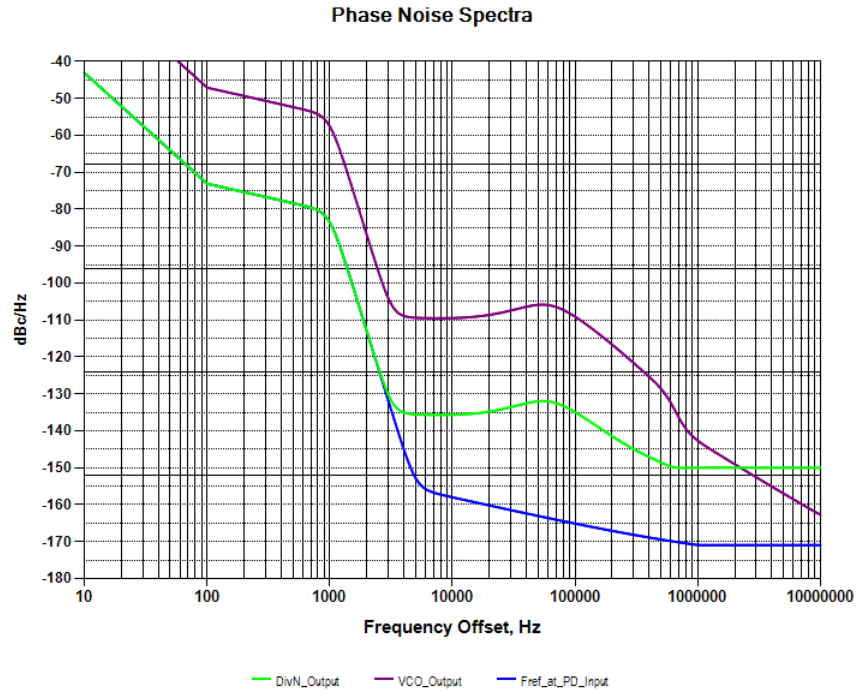


Figure 8 Phase noise analysis results for example 2 shown in Figure 6

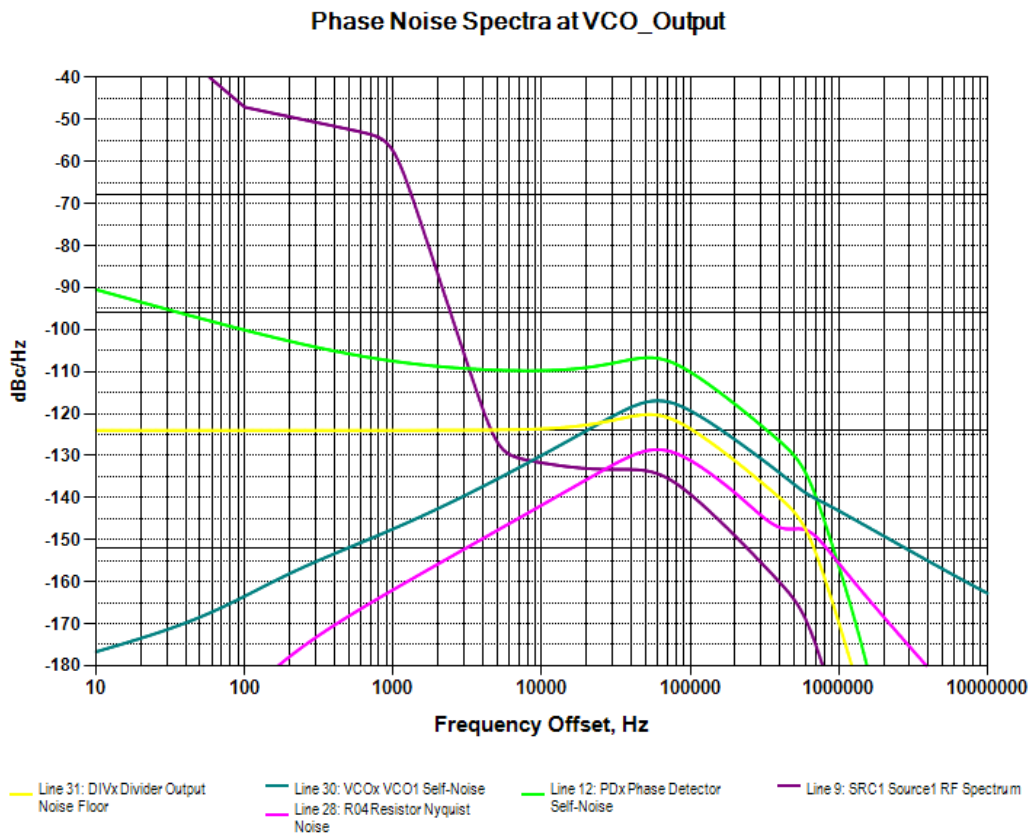


Figure 9 Major phase noise contributors for example-2 shown in Figure 6

2 References

1. Kroupa, V.F., "Noise Properties of PLL Systems," *IEEE Trans. Communications*, Oct. 1992.
2. Puglia, K.V., "Phase Noise Analysis of Component Cascades," *IEEE Microwave Magazine*, Dec. 2002.
3. Caprio, S.J., "Specifying Upper Bounds on Phase Noise in Phase-Locked Oscillators in Electronic Warfare Systems- Part I," *IEEE Microwave Magazine*, Dec. 2011.
4. Crawford, J.A., "Delta-Sigma Analog Interface Update in Long-Loop Context," Version 1.0, 24 Jan. 2012.
5. Crawford, J.A., "U18074 Digital Transponder Δ - Σ Tradeoffs," 12 Sept. 2011.
6. Kroupa, V.F., *Frequency Stability: Fundamentals and Measurement*, IEEE Press, 1983.
7. Robins, W.P., *Phase Noise in Signal Sources*, Peter Peregrinus Ltd., 1982.
8. Crawford, J.A., "U17370 Digital Transponder Phase Noise Details," 11 March 2011.
9. _____, *Advanced Phase-Lock Techniques*, Artech House, 2008.
10. _____, *Advanced Phase-Lock Applications- Synthesis*, Chapter 5, pub TBD.

3 Appendix: Block-Oriented Phase Noise Analysis

Detailed phase noise models for the key constituent blocks used in the phase noise analysis tool are described in detail in the material which follows. Some general comments are helpful at the outset.

The focus of this analysis is phase noise of course. In this context, phase noise and amplitude noise are differentiated in the analysis. For example, if a carrier signal is at -20 dBm and the noise floor is at -174 dBm/Hz, the C/N ratio is 154 dB-Hz whereas the phase noise portion would be 3 dB lower at -157 dBc/Hz. This is due to the equi-partition of random noise between AM and PM contributions (no angular preference). The noise calculations are consequently done by keeping separate track of the AM noise, the PM noise, and the carrier level.

All phase noise calculations done in this document obey the following rules:

- All RF signals are described in terms of their *single-sideband* phase noise power spectral densities which have a two-sided density (positive and negative frequencies). The colloquial language for this density is to represent it by $\mathcal{L}_{dB}(f)$. This is the same phase noise spectrum which would be observed on a spectrum analyzer and its units are always dBc/Hz. All RF input and output ports use the same characteristic impedance $R_o = 50\Omega$. Unused or unterminated RF ports *must be* terminated in 50Ω in order to get proper results. Internal program calculations are performed using $\sqrt{\mathcal{L}(f)}$ rad/ $\sqrt{\text{Hz}}$. Reiterating, this is a two-sided density but only the positive-frequency side is computed or displayed.

The key relationship which guides all of the computations between RF and baseband domains is

$$\begin{aligned}\mathcal{L}_{dB}(f) &= 20\log_{10}\left[\frac{\theta_{RMS}(f)}{\sqrt{2}}\right] \text{ dBc/Hz} \\ &= 20\log_{10}[\theta_{RMS}(f)] - 3.01 \text{ dBc/Hz}\end{aligned}\quad (2)$$

The units for \mathcal{L} are always rad^2/Hz which leads to

$$\sqrt{2\mathcal{L}(f)} = \theta_{RMS}(f) \quad (3)$$

All phase noise quantities are assumed to be *RMS* quantities and the *RMS* subscript is implied but not carried in through the notation.

- All baseband signals are one-sided (only positive frequencies) power spectral densities of phase $S_\theta(f)$, or baseband noise voltage or noise current. In the context of loop filters associated with PLLs, noise voltages predominate. All such baseband signals *do not* make use of any input/output characteristic impedance terminations.

Only a subset of the available design blocks can be used to interface between RF and baseband domains. Specifically,

Baseband to RF:

- Voltage-Controlled Oscillators (vco1, vco2, vco3)
- Modulator (mod)
- Direct-Digital Synthesizers (dds1, dds2)

RF to Baseband:

- Phase Detectors (pdcp, pdmx, pdvo)
- Analog-to-Digital Converters (adc1, adc2)
- Frequency Discriminator (fds)

It is a relatively simple matter to check a netlist to ensure that these guidelines are followed but this feature will only be implemented in subsequent releases.

All calculations are done assuming ambient temperature $T_o = 290^\circ$ Kelvin.

All of the phase noise calculations are also done based upon first-order principles. In the case of a mixer which has separate RF and LO inputs each with their own phase noise signatures, the output spectrum is technically a frequency-domain convolution of the two power spectral densities¹ involved (plus more terms if higher-order nonlinearities are also considered). However, if the two spectra each have -80 dBc/Hz sideband levels for example, the output portion due to this convolution would have a power spectral density level on the order of -160 dBc/Hz which would fall well below the first-order power spectral density terms in most cases where the densities simply power-add. These convolutions are not included in the computations considered here.

3.1 Analog-to-Digital Converter 1

adc1	$\pm n_1$	n_2	f_{clock}	N_{bits}	f_{sig}	HR_{dB}	σ_a	psd _{clock}
	n_1							input node (\pm sign determines if noise is added or subtracted)
		n_2						output node
			f_{clock}					ADC clock frequency, Hz
				N_{bits}				Number of effective bits
					f_{sig}			Center frequency of signal being digitized, Hz
						HR_{dB}		Headroom from full-scale, dB
							σ_a	ADC aperture jitter, sec RMS
								Filename for clock's power spectral density (phase noise)

Phase noise performance for an A-to-D converter (presumably digitizing a carrier-like signal at its input) is primarily degraded by quantization noise and sampling-clock jitter. There are certainly other degradations present, but these are the two dominant factors which are included in this modeling effort.

Assuming that the quantization noise is uniformly distributed and uncorrelated, the phase noise contribution referred to the ADC's input is a flat spectrum floor with level

$$\begin{aligned} \mathcal{L}_{Qfloor} &= 10 \log_{10} \left(\frac{2}{3} 2^{-2N_{bits}} f_{clock}^{-1} \right) + \gamma_{dB} \\ &= -1.76 - 10 \log_{10} (f_{clock}) - 6.02 N_{bits} + \gamma_{dB} \quad \text{dBc/Hz} \end{aligned} \quad (4)$$

The phase noise floor contribution from quantization is effectively dB for dB worse when the input carrier is less than full-scale by $\gamma_{dB} = HR_{dB}$.

The ADC clock jitter contribution to the phase noise spectrum is due to the aperture jitter within the ADC itself along with the phase noise spectrum associated with the clock to the ADC. The aperture jitter contributes a phase noise floor referenced to the ADC's input of

$$\mathcal{L}_{jitter} = 10 \log_{10} \left(\frac{\sigma_a^2 \omega_o^2}{f_{clock}} \right) - \gamma_{dB} \quad \text{dBc/Hz} \quad (5)$$

where the amount of aperture jitter is σ_a (seconds RMS) and the input signal's radian carrier frequency is ω_o . If the input carrier is less than full-scale, this floor contribution is dB-for-dB *smaller* as this result shows.

¹ rigorously true only for wide-sense stationary random processes.

If the ADC clock has a non-ideal phase noise spectrum (anything other than a Dirac delta function in frequency), its phase noise spectrum also gets directly added to the resultant output phase noise.² Clock noise produces other degradations also (e.g., (5.84) in [9]) but these fall in the multiplicative noise ratio category rather than phase noise per say and are not included here.

The modeling parameters associated with this model are

$\mathcal{L}_{in}(f)$	Input signal carrier's phase noise spectrum
N_{bits}	Number of effective ADC bits
HR_{dB}	Input sine wave signal head-room relative to a full-scale sine wave in dB
f_{clock}	ADC sampling rate, Hz
f_{sig}	Input signal's carrier frequency, Hz
σ_a	ADC's internal aperture jitter, seconds RMS
$\mathcal{L}_{Clock}(f)$	Phase noise spectrum of ADC's clock, dBc/Hz

The circuit simulation model for the ADC's phase noise performance is shown in Figure 10 and expanded into more detail in Figure 11. The different RMS noise quantities are all uncorrelated and given at node n_3 in Figure 11 with

$$S_1 = sign(n_1) \tag{6}$$

Context is used to distinguish the units for \mathcal{L} (dBc/Hz or rad^2 / Hz) rather than be burdened with additional notation to carry this distinction along.

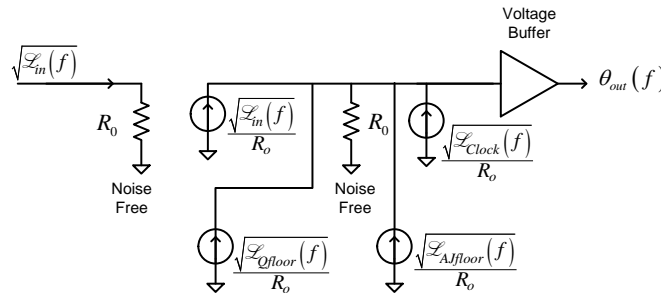


Figure 10 Circuit simulation model for ADC-related phase noise

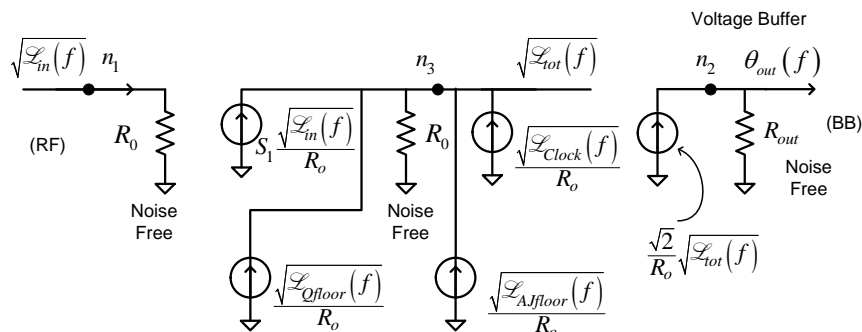


Figure 11 Detailed circuit simulation model³ for ADC-related phase noise, expanded from Figure 10. The input and output nodes are n_1 and n_2 respectively whereas node n_3 is an added internal node used to assist in computations. The voltage buffer is implemented in a convenient admittance-representation form using $R_{out} = 1 \Omega$ thereby representing a nearly ideal voltage source. The $\sqrt{2}$ factor arises from converting the RF phase noise spectrum to baseband.

² [9] §5.10.

³ Block diagram from *U18856 Phase Noise Modeling.vsd*.

The admittance matrix for the diagram shown in Figure 11 is given by

$$\begin{matrix}
 n_1 & \begin{bmatrix} R_o^{-1} & 0 & 0 \\ 0 & R_{out}^{-1} & -R_{out}^{-1} \\ -R_o^{-1} & 0 & R_o^{-1} \end{bmatrix} \\
 n_2 & \\
 n_3 & \\
 & \begin{matrix} n_1 & n_2 & n_3 \end{matrix}
 \end{matrix} \tag{7}$$

where the node numbers (n_1, n_2, n_3) are also shown for the rows and columns.

3.2 Analog-to-Digital Converter 2

adc2	$\pm n_1$	n_2	$\pm n_3$	f_{clock}	N_{bits}	f_{sig}	HR_{dB}	σ_a
	n_1							input node (\pm sign determines if noise is added or subtracted)
	n_2							output node
	n_3							clock node (\pm sign determines if noise is added or subtracted)
	f_{clock}							ADC clock frequency, Hz
	N_{bits}							Number of effective bits
	f_{sig}							Center frequency of signal being digitized, Hz
	HR_{dB}							Headroom from full-scale, dB
	σ_a							ADC aperture jitter, sec RMS

This ADC is the same as that described in §3.1 except that the phase noise spectrum associated with the clock is given by a signal elsewhere in the circuit rather than by a datafile. This block also makes it possible to control whether clock phase is added or subtracted. The associated circuit simulation model⁴ is shown in Figure 12. Following the same convention as used with adc1 in §3.1, $R_{out} = 1\Omega$ and define

$$S_1 = sign(n_1) \tag{8}$$

$$S_3 = sign(n_3) \tag{9}$$

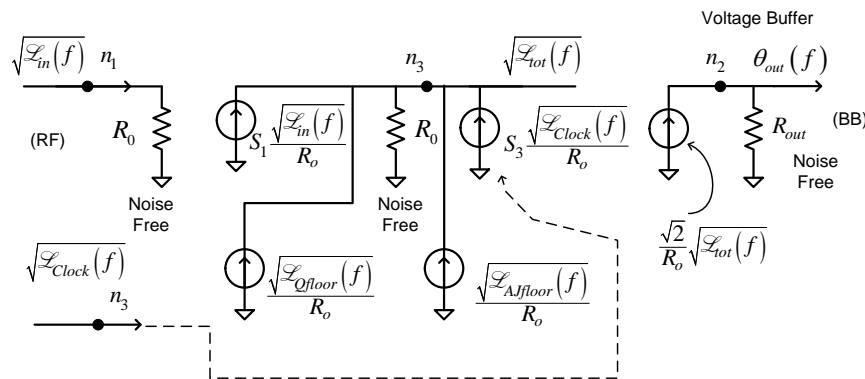


Figure 12 Circuit simulation model for ADC with node-based clock spectrum

⁴ Ibid.

3.3 Attenuator

att	n_1	n_2	P_{c_dBm}	L_{dB}
	n_1			Input node
		n_2		Output node
			P_{c_dBm}	Input carrier level, dBm
				L_{dB} Attenuator loss, dB

Assume that a standard attenuator with a loss of L_{dB} is under consideration. Given an input carrier level of P_{c_dBm} the output carrier level is of course $P_{c_dBm} - L_{dB}$. For simplicity, assign $L = 10^{(L_{dB}/10)}$. The carrier level and noise level at the attenuator output are then as separately shown in Figure 13 where $S_n(f)$ is a total power spectral density for the noise in mW / Hz.

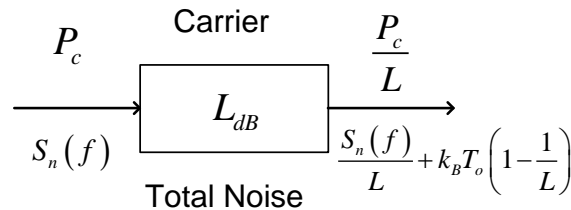


Figure 13 Computing phase noise transfer function for an impedance-matched attenuator (loss). The Boltzmann constant is represented by k_B and the absolute temperature by T_o which is normally taken to be 290° K.

Rigorously speaking, the power spectral density $S_n(f)$ contains both AM and PM noise, but given the assertions (assumptions) stated earlier, only the phase noise portion is of interest here. Similarly speaking, the $k_B T_o$ term has equal portions of AM and PM noise for completely random noise. Putting these elements together, the output phase noise spectrum is given by

$$\mathcal{L}_{out} = 10 \log_{10} \left[10^{(\mathcal{L}_{in}/10)} + \frac{k_B T_o}{2P_c} (L - 1) \right] \text{ dBc/Hz} \tag{10}$$

where the input phase noise spectrum is represented by \mathcal{L}_{in} , the output phase noise spectrum is represented by \mathcal{L}_{out} both with dBc/Hz units, and the carrier power (in consistent units) is represented by P_c . Note that if $L = 1$ (no loss), the output phase noise spectrum is identical to the input phase noise spectrum as expected. Similarly, if the attenuator loss is 30 dB, the input carrier power 0 dBm, and the input phase noise level at 10 kHz offset equal to -145 dBc/Hz, (10) predicts the output phase noise level will be -142.9 dBc/Hz which is reasonable since the output carrier level will be -30 dBm which is only 144 dB above the thermal noise floor.

This model can be modeled in a standard circuit simulator by letting the input voltage to the block represent the phase noise at the block input in radians RMS / $\text{Hz}^{0.50}$ with the standard impedance level ($R_o = 50\Omega$) as shown in Figure 14. Assuming here that $n_1 = 1$ and $n_2 = 2$ for convenience, the admittance matrix for the RF attenuator is given by

$$Y = \begin{bmatrix} R_o^{-1} & 0 \\ -\frac{2}{R_o} & R_o^{-1} \end{bmatrix} \tag{11}$$

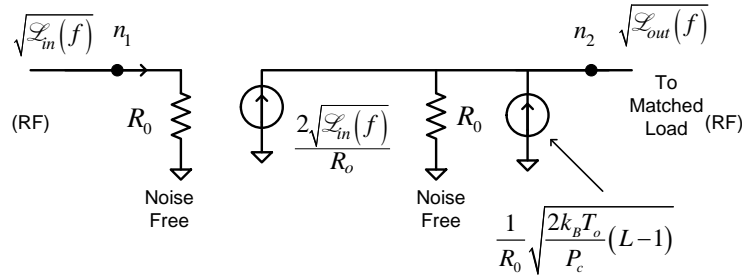


Figure 14 Circuit simulator model for phase noise through an impedance-matched RF attenuator

3.4 Capacitor

- cap n₁ n₂ C
- n₁ Positive node
 - n₂ Negative node
 - C Capacitance value, Farads

The capacitor is one of the more simple elements available in the phase noise analysis tool. It is modeled as a simple noiseless admittance between nodes n₁ and n₂ with value sC where s is complex-frequency and C is the capacitance value.

3.5 Digital Divider

- div n₁ n₂ N NF_{dB} P_{dBm} f_{one} L_{dBc}
- n₁ Input node
 - n₂ Output node
 - N Divide ratio
 - NF_{dB} Input-referred noise figure, dB
 - P_{dBm} Input carrier level, dBm
 - f_{one} Flicker corner frequency, Hz
 - L_{floor} Achievable phase noise floor at divider output, dBc/Hz

The frequency divider model is very similar to that used for the frequency multiplier except that an additional noise floor term has been added to ensure that output noise levels remain reasonable for even very large values of divide-ratio N . The governing equation is

$$L_{out}(f) = 10 \log_{10} \left[\frac{10^{[L_{in}(f)/10]}}{N^2} + \frac{k_B T_o}{2 P_c N^2} (F - 1) \left(1 + \frac{f_{one}}{f} \right) + 10^{(L_{floor}/10)} \right] \text{ dBc/Hz} \quad (12)$$

where $L_{in}(f)$ is the input phase noise spectrum in dBc/Hz, the input carrier power is P_c , the input-referred noise factor is F , the flicker noise corner is f_{one} , and the frequency division ratio is N . The minimum phase noise floor observable at the divider's output is governed by L_{floor} which has units of dBc/Hz. The associated circuit simulator model is shown in Figure 15.

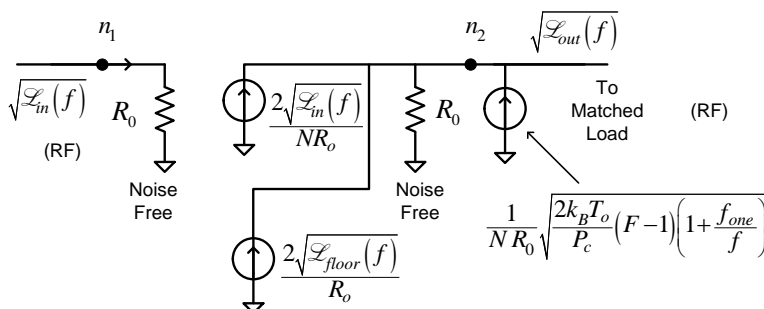


Figure 15 Circuit simulation model for digital frequency divider

3.6 Fractional-N Divider

divf	n ₁	n ₂	N	NF _{dB}	P _{dBm}	f _{one}	L _{dBc}	M	f _{ref}
	n ₁	Input node							
	n ₂	Output node							
	N	Divide ratio							
	NF _{dB}	Input-referred noise figure, dB							
	P _{dBm}	Input carrier level, dBm							
	f _{one}	Flicker corner frequency, Hz							
	L _{floor}	Achievable phase noise floor at divider output, dBc/Hz							
	M	Δ-Σ order (e.g., 1 to 3)							
	f _{ref}	Reference frequency, rate of Δ-Σ update, Hz							

The model used is identical to that used for the digital divider except that an additional input-referred phase noise source is added to account for the fractional-N ingredient. The input-referred phase noise attributable to fractional-N operation is given by⁵

$$L_{frac}(f) = 10 \log_{10} \left\{ \frac{(2\pi)^2}{12 f_{ref}} \left[2 \sin \left(\frac{\pi f}{f_{ref}} \right) \right]^{2(M-1)} \right\} \text{ dBc/Hz} \tag{13}$$

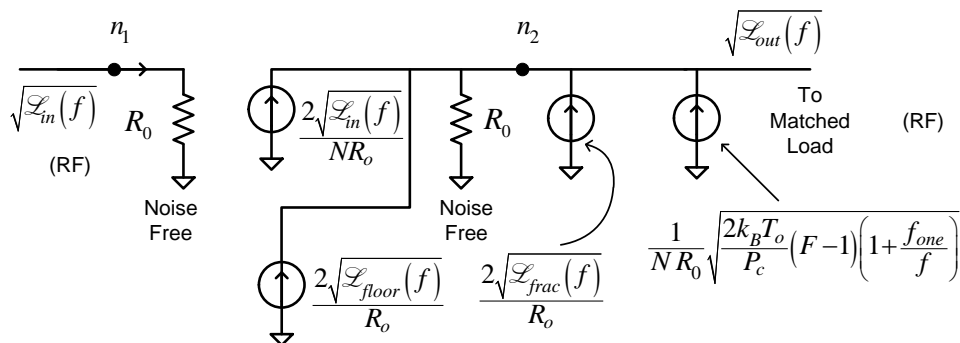


Figure 16 Circuit simulation model for digital fractional-N divider

⁵ Equ. (2.96) of [10].

3.7 Direct-Digital Synthesizer 1

dds1	$\pm n_1$	n_2	f_{clock}	N_{bits}	f_{sig}	jitter	σ_a	psd _{clock}
	n_1							Input node (\pm sign determines if noise is added or subtracted)
		n_2						Output node
			f_{clock}					Clock frequency, Hz
				N_{bits}				Number of effective bits
					f_{sig}			Carrier frequency, Hz
						σ_a		DAC's internal aperture jitter, sec RMS
							psd _{clock}	Filename for clock's phase noise

The phase noise contribution to the output signal from the clock's phase noise spectrum is given by⁶

$$\mathcal{L}_{clk}(f) = \mathcal{L}_{clock}(f) + 20 \log_{10} \left(\frac{f_{sig}}{f_{clock}} \right) \text{ dBc/Hz} \quad (14)$$

The clock's phase noise spectrum is given in the file named psd_{clock} in terms of frequency offsets and dBc/Hz. The quantization-related phase noise floor contribution is given by

$$\begin{aligned} \mathcal{L}_{Qfloor} &= 10 \log_{10} \left(\frac{2}{3} 2^{-2N_{bits}} f_{clock}^{-1} \right) \\ &= -1.76 - 10 \log_{10} (f_{clock}) - 6.02 N_{bits} \text{ dBc/Hz} \end{aligned} \quad (15)$$

Internal aperture jitter within the DAC itself sets another phase noise floor. The aperture jitter contributes a phase noise floor of

$$\mathcal{L}_{jitter} = 10 \log_{10} \left(\frac{\sigma_a^2 \omega_o^2}{f_{clock}} \right) \text{ dBc/Hz} \quad (16)$$

where $\omega_o = 2\pi f_{sig}$. These different noise mechanisms lead to the DDS phase noise circuit simulation model shown in Figure 17 where

$$\gamma = \frac{f_{sig}}{f_{clock}} \quad (17)$$

The DDS-DAC is output is assumed to operate with a full-scale output.

⁶ From §5.5.1 of *Advanced Phase-Lock Applications*, J.A. Crawford, to be published [10].

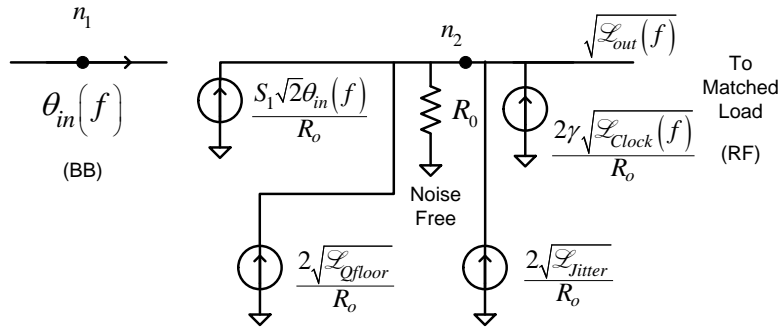


Figure 17 Circuit simulation model for direct digital synthesizer phase noise

3.8 Direct-Digital Synthesizer 2

dds2	$\pm n_1$	$\pm n_2$	$\pm n_3$	f_{clock}	N_{bits}	f_{sig}	$jitter_{ps}$
	n_1						
	n_2						
	n_3						
	f_{clock}						
	N_{bits}						
	f_{sig}						
	σ_a						

- n_1 Input node (\pm sign determines if noise is added or subtracted)
- n_2 Output node
- n_3 Clock node (\pm sign determines if noise is added or subtracted)
- f_{clock} Clock frequency, Hz
- N_{bits} Number of effective bits
- f_{sig} Output carrier frequency, Hz
- σ_a DAC's internal aperture jitter, sec RMS

This block is very similar to the previous DDS block described in §3.7, the primary difference being that the clock's phase noise is given by an internal node within the system rather than by a datafile.

The phase noise contribution to the output signal from the clock's phase noise spectrum is given by⁷

$$\mathcal{L}_{clk}(f) = \mathcal{L}_{clock}(f) + 20 \log_{10} \left(\frac{f_{sig}}{f_{clock}} \right) \text{ dBc/Hz} \tag{18}$$

The quantization-related phase noise floor contribution is given by

$$\begin{aligned} \mathcal{L}_{Qfloor} &= 10 \log_{10} \left(\frac{2}{3} 2^{-2N_{bits}} f_{clock}^{-1} \right) \\ &= -1.76 - 10 \log_{10} (f_{clock}) - 6.02 N_{bits} \text{ dBc/Hz} \end{aligned} \tag{19}$$

Internal aperture jitter within the DAC itself sets another phase noise floor. The aperture jitter contributes a phase noise floor of

$$\mathcal{L}_{jitter} = 10 \log_{10} \left(\frac{\sigma_a^2 \omega_o^2}{f_{clock}} \right) \text{ dBc/Hz} \tag{20}$$

where $\omega_o = 2\pi f_{sig}$. These different noise mechanisms lead to the DDS phase noise circuit simulation model shown in Figure 18 where

⁷ From §5.5.1 of *Advanced Phase-Lock Applications*, J.A. Crawford, to be published [10].

$$\gamma = \frac{f_{sig}}{f_{clock}}$$

$$S_1 = \text{sign}(n_1)$$

$$S_3 = \text{sign}(n_3)$$
(21)

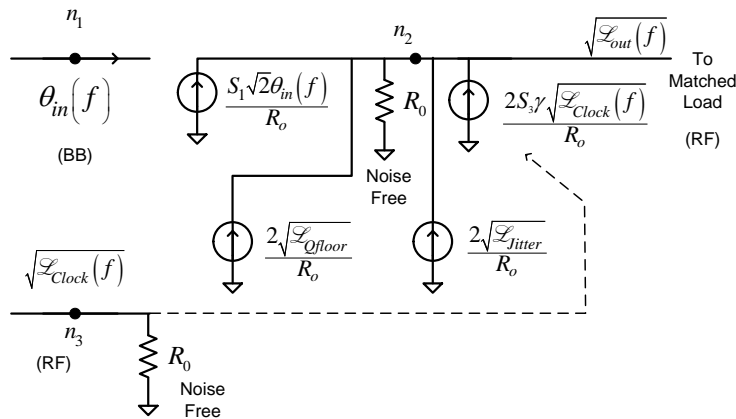


Figure 18 Circuit simulation model for direct digital synthesizer phase noise

3.9 Time Delay

dly	n_1	n_2	τ_d
	n_1	Input node	
	n_2	Output node	
	τ_d	Time delay	

The circuit simulation model for the ideal time-delay is shown in Figure 19.

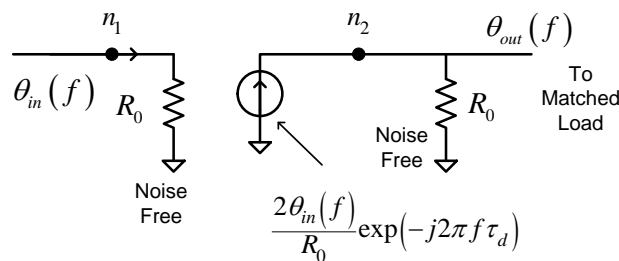


Figure 19 Circuit simulation model for ideal time-delay

3.10 Frequency Discriminator

fds	n_1	n_2	τ_d	K_{fd}	NF _{dB}	P _{RF}
	n_1	Input node				
	n_2	Output node				
	τ_d	Time delay, sec				
	K_{fd}	Discriminator voltage gain, V/rad				
	NF _{dB}	Input-referred noise figure, dB				
	P _{dBm}	Input carrier power, dBm				

A frequency discriminator is fundamentally a differentiator of signal phase. The model assumed here is based upon using an ideal delay-line and ideal multiplier forming the discriminator function. The ideal transfer function for this block is

$$\begin{aligned} V_{out}(s) &= K_o \theta_{in}(s) [1 - e^{-s\tau_d}] \\ &= K_o \sqrt{2\mathcal{L}_{in}(f)} [1 - e^{-s\tau_d}] \end{aligned} \quad (22)$$

where it is assumed that the discriminator has been perfectly aligned with the input carrier center frequency a priori. In this formulation, τ_d is the time delay used in the discriminator, and K_o is the gain of the discriminator.

Aside from circuit-related noise in the discriminator, the finite input SNR also creates a colored noise spectrum at the discriminator output. As given by (22), the discriminator output in the time domain is given by

$$v(t) = K_o [\theta(t) - \theta(t - \tau_d)] \quad (23)$$

and its autocorrelation function (assuming wide-sense stationarity) is given by

$$\begin{aligned} R_v(\tau) &= K_o^2 E \{ [\theta(t) - \theta(t - \tau_d)] [\theta(t + \tau) - \theta(t + \tau - \tau_d)] \} \\ &= K_o^2 [2R_\theta(\tau) - R_\theta(\tau - \tau_d) - R_\theta(\tau + \tau_d)] \end{aligned} \quad (24)$$

Using the Wiener-Khintchine theorem, this can be expressed in terms of power spectral densities as

$$R_v(\tau) = 4K_o^2 \int_{-\infty}^{+\infty} S_\theta(f) \sin^2(\pi f \tau_d) e^{j2\pi f \tau} df \quad (25)$$

which makes it possible to finally conclude that the power spectral density of $v(t)$ is given by

$$S_v(f) = 4K_o^2 S_\theta(f) \sin^2(\pi f \tau_d) \quad \text{V}^2 / \text{Hz} \quad (26)$$

where in this form, both power spectral densities are two-sided (i.e., positive and negative Fourier frequencies). The discriminator output is, however, at baseband and this factor must be taken into account.

The overall gain of the discriminator is a function of the offset frequency from the carrier frequency as captured in the circuit simulation model shown in Figure 20. Note that

$$\begin{aligned} F &= 10^{NF_{dB}/10} \\ P_c &= 10^{(P_{dBm} - 30)/10} \text{ W} \end{aligned} \quad (27)$$

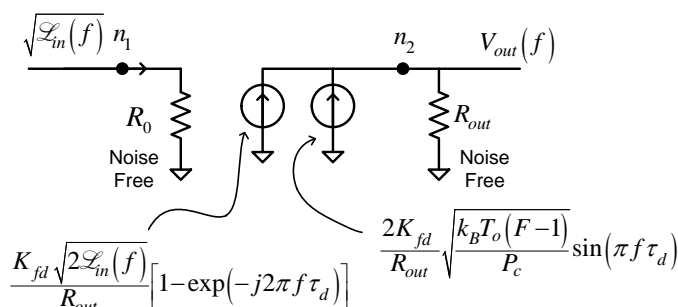


Figure 20 Circuit simulation model for time-delay based frequency discriminator

3.11 RF Filter

fil	n_1	n_2	f_c	N	$L_{max_{dB}}$	P_{dBm}	τ_d	IL_{dB}
	n_1							Input node
		n_2						Output node
			f_c					-3 dB corner frequency, Hz
				N				(Butterworth) lowpass filter order
					$L_{max_{dB}}$			Maximum stopband loss achievable, dB
						P_{dBm}		Input carrier level, dBm
							τ_d	Nominal group delay, sec
								Insertion loss, dB

RF filters are considered to be lowpass filters centered on the signal carrier in the phase noise context. The model is based upon a frequency-dependent loss function but is otherwise very similar to the model used in §3.3. The model is based upon cascading a lossless filter attenuation function with a flat-loss of L . For the lossless (Butterworth) filter portion

$$A_{NoLoss}(f) = 1 + \left(\frac{f}{f_c}\right)^{2N} \tag{28}$$

where $A_{NoLoss}(f)$ is the ideal numerical power-attenuation of the filter versus offset frequency from the carrier. The insertion loss L is given by $L = 10^{IL_{dB}/10}$. The maximum stopband loss is represented here by $L_{max} = 10^{L_{max_{dB}}/10}$. It is a simple matter to limit the stopband attenuation by defining

$$A(f) = \left(\frac{1}{A_{NoLoss}(f)} + \frac{1}{L_{max}}\right)^{-1} \tag{29}$$

Putting these factors together, the corresponding circuit simulation diagram is shown in Figure 21.

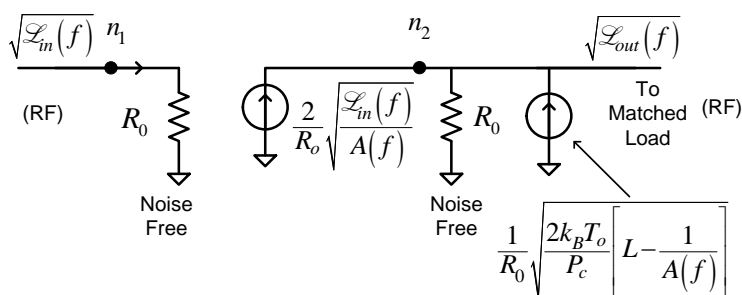


Figure 21 Circuit simulator model for phase noise through an impedance-matched RF filter with loss through the filter represented by $A(f)$. Note that in this form, $A(f) \geq 1$.

Side Note: The filter block requires the carrier input power level to be entered in order to do its calculations. Strange results can be obtained as shown in Figure 22 if input source spectrums are used with a noncommensurate carrier power level. In the example shown, the input phase noise to the filter is supposedly as low as -160 dBc, but the input carrier level to the attenuator was erroneously set to -40 dBm. At this carrier level, the best phase noise floor possible is $-134 - 3 = -137$ dBc/Hz rather than -160 dBc/Hz. Raising the input carrier level to -10 dBm produces the expected (and correct) result shown in Figure 23.

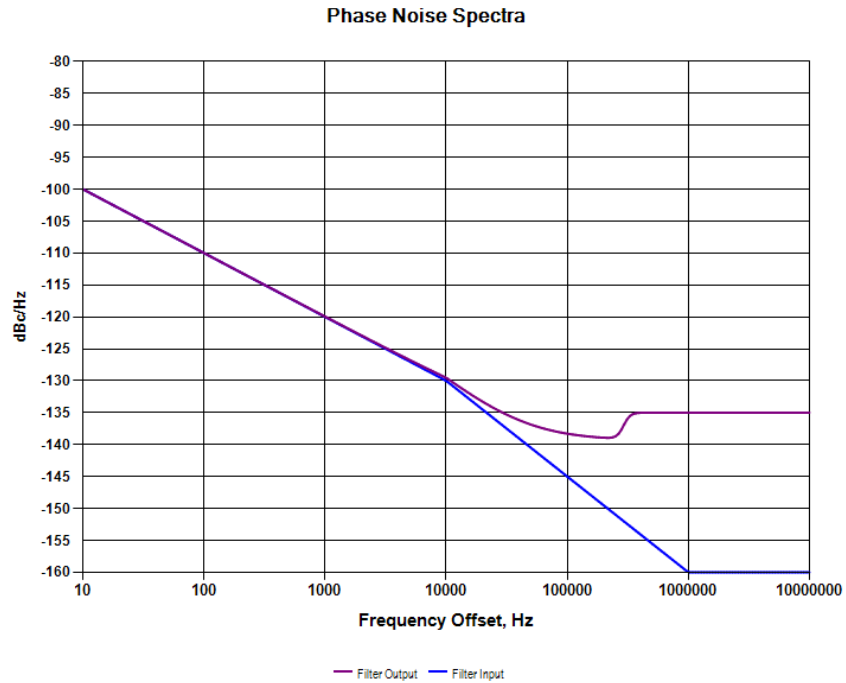


Figure 22 Example of an erroneous phase noise calculation through an RF filter

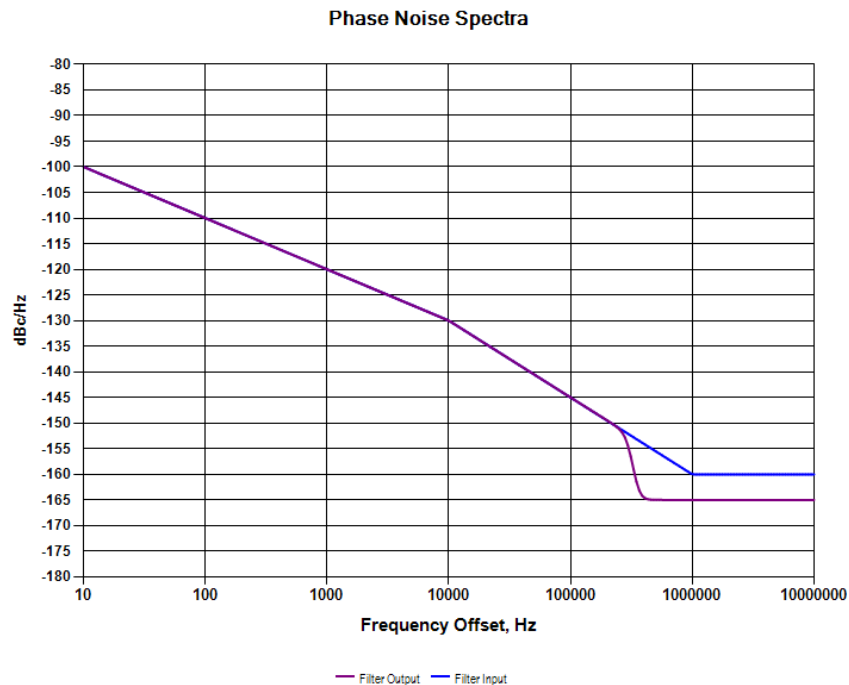


Figure 23 Example of a correctly computed phase noise spectrum at the filter output

3.12 Frequency Multiplier

fmx	n_1	n_2	N	P_{dBm}	NF_{dB}	f_{one}
	n_1					Input node
		n_2				Output node
			N			Frequency multiplication factor
				P_{dBm}		Carrier input power level, dBm
				NF_{dB}		Input-referred noise figure, dB
					f_{one}	1/f corner frequency, Hz

The frequency multiplier is modeled here based upon the equation

$$\mathcal{L}_{out}(f) = 10 \log_{10} \left[10^{\left[\frac{\mathcal{L}_{in}(f)}{10} \right]} + \frac{k_B T_o}{2P_c} (F - 1) \left(1 + \frac{f_{one}}{f} \right) \right] + 20 \log_{10}(N) \text{ dBc/Hz} \quad (30)$$

where $\mathcal{L}_{in}(f)$ is the input phase noise spectrum in dBc/Hz, the input carrier power is P_c , the input-referred noise factor is F , the flicker noise corner frequency is f_{one} , and the frequency multiplication factor is N . The associated circuit simulation model is shown in Figure 24.

Specifying the noise performance in terms of an input-referred noise figure should avoid having to change this parameter for every different multiplication factor N .

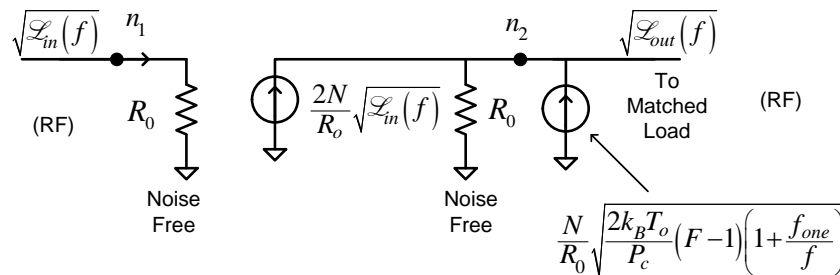


Figure 24 Circuit simulator model for phase noise through a frequency multiplier

3.13 Inductor

ind	n_1	n_2	L
	n_1		Positive node
		n_2	Negative node
			L Inductor value, Henries

The inductor is one of the more simple elements available in the phase noise analysis tool. It is modeled as a simple noiseless admittance between nodes n_1 and n_2 with value $1/(sL)$ where s is complex-frequency and L is the inductance value.

3.14 Modulator (Linear Baseband to RF)

mod	n_1	n_2	K
	n_1	Input node	
	n_2	Output node	
	K	Gain term, rad/V	

This block is best thought of as a noiseless modulator which accepts a baseband voltage input and converts it to an RF signal. The input impedance is ∞ whereas the output impedance is R_o . The model for this block is shown in Figure 25.

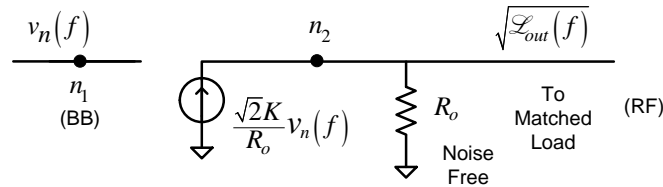


Figure 25 Linear baseband to RF modulator model

3.15 RF Mixer

mxr	$\pm n_1$	$\pm n_2$	n_3	P_{LO}	P_{RF}	f_{one}	NF_{RF}	NF_{LO}
	n_1	RF input port (\pm sign for sum or difference applies to the phase)						
	n_2	LO input port (\pm sign for sum or difference applies to the phase)						
	n_3	Output port						
	P_{LO}	Local oscillator input power level, dBm						
	P_{RF}	Input carrier level, dBm						
	f_{one}	Flicker frequency corner for LO port, Hz						
	NF_{RF}	Effective noise figure for the RF port, dB						
	NF_{LO}	Effective noise figure for the LO port, dB						

The primary mixer parameters which affect the output phase noise spectrum are the input carrier level at the RF port and the RF port – referred noise figure.⁸ Although any physical mixer also exhibits conversion loss (or gain), the affect on phase noise performance is captured in these previous two parameters. Technically speaking, the LO and RF ports exhibit their own effective noise figure values which are not the same. Any $1/f$ noise considerations are attributed to the LO port alone since it is primarily responsible for determining where the zero-crossings occur with time.

The effective RF input port referred phase noise can be written as

$$\mathcal{L}_{RF_{eff}} = 10 \log_{10} \left[10^{(\mathcal{L}_{RF}/10)} + \frac{k_B T_o}{2P_{RF}} (F_{RF} - 1) \right] \text{ dBc/Hz} \quad (31)$$

where the input carrier power level is represented by P_{RF} , the ideal RF-port input phase noise spectrum is represented by \mathcal{L}_{RF} (dBc/Hz), and the RF-port *noise factor* given by F_{RF} . This relationship properly captures the role of the carrier power and RF-port effective noise figure in determining the effective input phase noise spectrum to the mixer for this port.

A similar relationship applies for the LO port except an additional factor is included to account for possible $1/f$ noise which is to be included. This relationship is given by

⁸ Mixer discussion in [2].

$$\mathcal{L}_{LOeff} = 10 \log_{10} \left[10^{(\mathcal{L}_{LO}/10)} + \frac{k_B T_o}{2P_{LO}} (F_{LO} - 1) \left(1 + \frac{f_{one}}{f} \right) \right] \text{ dBc/Hz} \quad (32)$$

where the only real new term is the $1/f$ corner frequency represented by f_{one} . Treating the RF mixer as an ideal multiplier between the RF and LO signals, if the RF and LO signals are statistically independent of each other, the results given in (31) can be simply power-added. In more complicated frequency synthesis schemes where some coherence between terms may be present, however, this may not be the case. This situation can fortunately be handled nicely by the circuit simulation based approach being discussed for modeling phase noise by using the model shown in Figure 26.

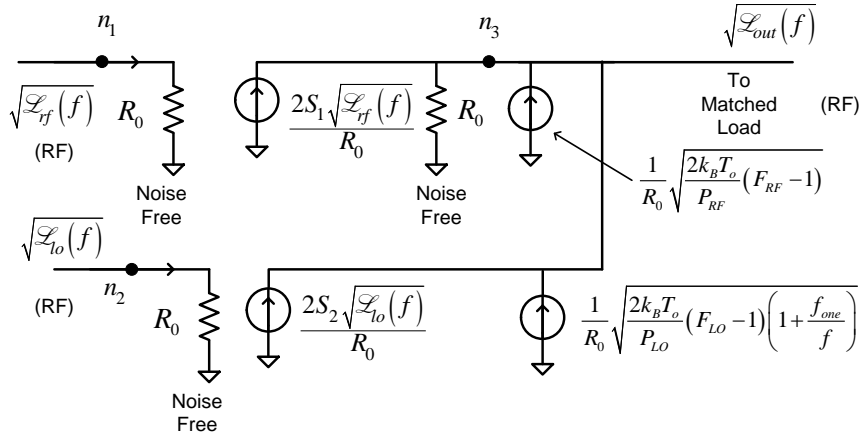


Figure 26 Circuit simulator model for phase noise through an impedance-matched RF mixer

The same convention is used where

$$\begin{aligned} S_1 &= \text{sign}(n_1) \\ S_2 &= \text{sign}(n_2) \end{aligned} \quad (33)$$

3.16 Operational Amplifier

opa	n_1	n_2	n_3	G_{dB}	f_{dp}	vnfile	infile
	n_1						Positive input node
		n_2					Negative input node
			n_3				Output node
				G_{dB}			Maximum open-loop gain, dB
					f_{dp}		Dominant pole, Hz
						vnfile	File name for equivalent input voltage noise, format frequency, dBVRMS/Hz ^{1/2}
						infile	File name for equivalent input current noise, format frequency, dBIRMS/Hz ^{1/2}

A simplistic model for an op-amp is shown in Figure 27. This model includes (uncorrelated) input noise current and noise voltage sources and provision for a dominant pole given by

$$f_{dp} = \frac{1}{2\pi R_p C_p} \text{ Hz} \quad (34)$$

Resistor R_p is chosen to be 10 kΩ without any loss of generality. In this model, the maximum voltage gain of the op-amp is assumed to be G_{dB} which leads to the transconductance g_m being given by

$$g_m = \frac{10^{(G_{dB}/20)}}{R_p} \tag{35}$$

Two internal nodes are created to implement the op-amp model as shown in Figure 27. Resistors R_u , R_p , and R_{out} are all noise-free. The output impedance R_{out} is taken to be 10Ω.

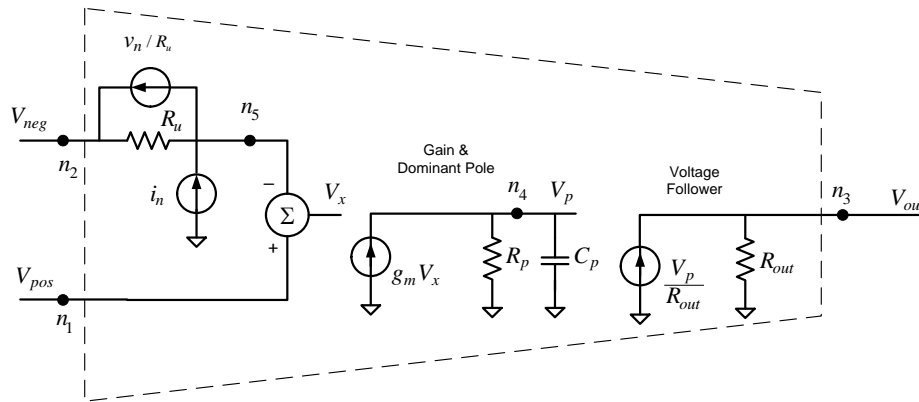


Figure 27 Simplistic op-amp model including input noise voltage and noise current source

3.17 PLL Digital Phase/Frequency Detector (Charge-Pump)

pdcp	$\pm n_1$	$\pm n_2$	n_3	K_d	FoM	f_{one}	f_{ref}
	n_1	f_{ref} port (\pm sign for phase)					
	n_2	feedback port (\pm sign for phase)					
	n_3	Charge-pump output					
	K_d	Phase detector gain, A/rad					
	FoM	Figure of merit, dBc/Hz					
	f_{one}	Flicker frequency corner, Hz					
	f_{ref}	Reference frequency, Hz					

The phase noise performance of a digital phase/frequency detector referenced to its output is governed by the equation⁹

$$\mathcal{L}_{pd}(f) = FoM + 10 \log_{10}(f_{ref}) + 10 \log_{10} \left(1 + \frac{f_{one}}{f} \right) \text{ dBc/Hz} \tag{36}$$

where FoM is known as the detector's *figure of merit* and f_{one} is the device's $1/f$ noise corner frequency. A typical FoM value for a PLL device from National Semiconductor is -215 dBc/Hz, for example. The circuit simulation model used for this block is shown in Figure 28.

In this model, it is assumed that the effective noise figure of the device's ports are effectively lumped into the figure of merit.

⁹ [9].

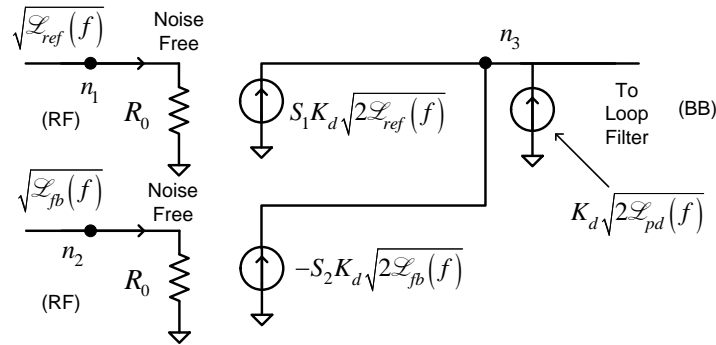


Figure 28 Circuit simulation model for modeling a charge-pump style digital phase detector in a PLL where K_d is the phase detector gain in A / rad

3.18 PLL Mixer-Based Phase Detector

pdmx	$\pm n_1$	$\pm n_2$	n_3	K_d	P_{LO}	P_{RF}	f_{one}	NF_{RF}	NF_{LO}
	n_1								
	n_2								
	n_3								
	K_d								
	P_{LO}								
	P_{RF}								
	f_{one}								
	NF_{RF}								
	NF_{LO}								

This phase detector is modeled as an ideal RF signal multiplier where the phase noise of the two signals being compared is added and a 1/f noise term is also included. The model is very similar to the RF mixer (see §3.15) except that a phase detector gain value K_d is included and the mixer output is a baseband voltage source. The circuit simulation details are shown in Figure 29 where K_d represents the detector's open-circuit gain in V / rad.

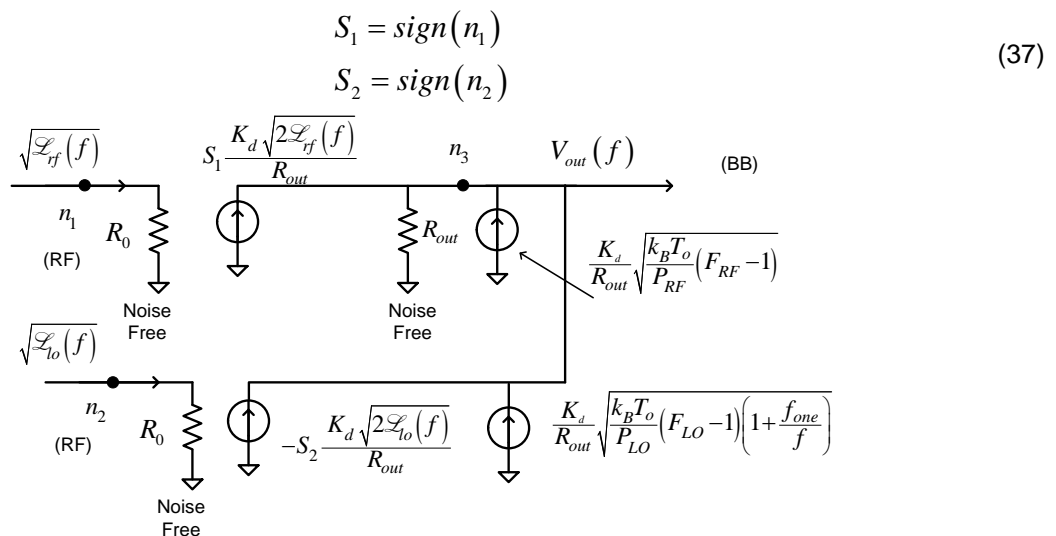


Figure 29 Circuit simulation model for the mixer-based linear phase detector. $R_{out} = 10\Omega$ is assumed. S_1 and S_2 are ± 1 sign-terms which make it easy to change polarities without having to change node-numbers. With both signs positive, the normal phase difference quantity computed is $\theta_{RF} - \theta_{LO}$.

3.19 Digital Phase Detector with Voltage Output

pdvo	$\pm n_1 \pm n_2 n_3 K_d FoM f_{one} f_{ref}$
n_1	Reference port node (\pm sign for phase)
n_2	Feedback port node (\pm sign for phase)
n_3	Output node
K_d	Phase detector gain, V / rad
FoM	Phase detector figure of merit, dBc/Hz
f_{one}	Flicker noise corner frequency, Hz
f_{ref}	Phase comparison frequency, Hz

This phase detector is very similar to the charge-pump phase detector, the primary difference being that its output is a voltage rather than a current.

The phase noise performance of a digital phase/frequency detector referenced to its output is governed by the equation¹⁰

$$\mathcal{L}_{pd}(f) = FoM + 10\log_{10}(f_{ref}) + 10\log_{10}\left(1 + \frac{f_{one}}{f}\right) \text{ dBc/Hz} \tag{38}$$

where *FoM* is known as the detector's *figure of merit* and f_{one} is the devices $1/f$ noise corner frequency. A typical *FoM* value for a PLL device from National Semiconductor is -215 dBc/Hz, for example. The circuit simulation model used for this block is shown in Figure 30.

In this model, it is assumed that the effective noise figure of the device's ports are effectively lumped into the figure of merit.

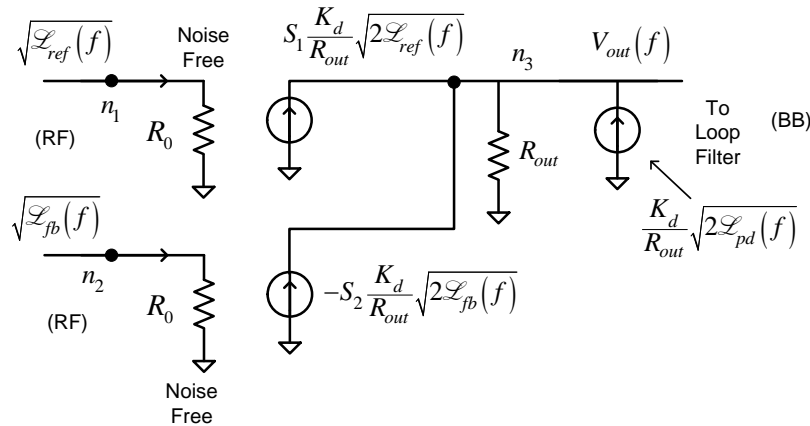


Figure 30 Circuit simulation model for the voltage-output linear phase detector. $R_{out} = 10\Omega$ is assumed. When both signs are positive, the phase error function formed is $\theta_{ref} - \theta_{fb}$.

¹⁰ [9].

3.20 Schematic Probe

prb n₁ title

n₁ Circuit node where probe is placed

title Continuous character string name for probe (e.g., PLL-times-4-output)

This block is strictly a monitoring point used to direct computation outputs. It has no bearing on the actual internal parameters used in the computations.

3.21 Resistor

res n₁ n₂ ±R

n₁ Positive node

n₂ Negative node

R Resistance value, Ohms (<0 to make noiseless)

The resistor is one of the more simple elements available in the phase noise analysis tool. It is modeled as a simple admittance between nodes n₁ and n₂ with value 1/R. If the resistance value is < 0, the resistor is assumed to be noiseless.

3.22 RF Amplifier

rfa n₁ n₂ NF_{dB} P_{dBm} f_{one}

n₁ Input node

n₂ Output node

NF_{dB} Noise figure, dB

P_{dBm} Input carrier level, dBm

f_{one} Flicker noise corner frequency, Hz

Using similar arguments to those made in §3.3, the output phase noise performance from an RF amplifier is given by

$$\mathcal{L}_{out} = 10 \log_{10} \left[10^{(\mathcal{L}_in/10)} + \frac{k_B T_o}{2P_c} (F - 1) \left(1 + \frac{f_{one}}{f} \right) \right] \text{ dBc/Hz} \quad (39)$$

where the noise factor is represented by F and the flicker noise corner by f_{one} . The noise factor and noise figure are related by

$$NF_{dB} = 10 \log_{10} (F) \text{ dB} \quad (40)$$

The circuit simulator model for the phase noise performance of an RF amplifier is shown in Figure 31.

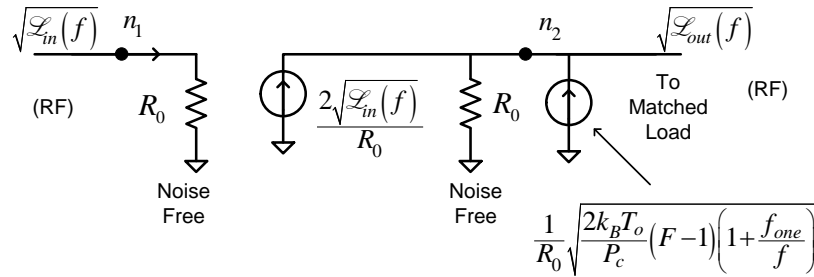


Figure 31 Circuit simulator model for phase noise through an impedance-matched RF amplifier with noise factor $F = 10^{(NF_{dB}/10)}$

3.23 Signal Splitter

splt n₁ n₂ n₃
 n₁ Input node
 n₂ First output
 n₃ Second output

The splitter block is lossless and noiseless. Its input impedance is R_o and both output ports have an output impedance of R_o .

3.24 RF Source1

src1 n₁ psdfile
 n₁ Output node of source
 psdfile File name for source's phase noise power spectral density, formatted [frequency offset, dBc/Hz]

This block makes it possible to input a source's phase noise power spectral density into the circuit. The block's output impedance is R_o .

3.25 RF Source2

src2 n₁ P_{carr} f_{one} L_{ped} f_c
 n₁ Output node of source
 P_{carr} Carrier power level, dBm
 f_{one} 1/f corner frequency, Hz
 L_{ped} Single sideband phase noise pedestal height, dBc/Hz
 f_c -3 dB corner frequency for the phase noise pedestal

This block makes it possible to input a source's phase noise power spectral density into the circuit parametrically. The block's output impedance is R_o .

3.26 Sum

sum $\pm n_1 \pm n_2 n_3$

n_1	Input port #1
n_2	Input port #2
n_3	Output port

The sum block is useful for combining baseband signals. As such, its input impedance for both ports is ∞ whereas the output impedance is 10Ω thereby modeling a voltage output. Unity-gain is provided through the block and the block is assumed to be noiseless. The signs of n_1 and n_2 are used to determine how the input phase arguments are applied to the sum-block.

3.27 Signal (Voltage) Buffer

vbuf $n_1 n_2$

n_1	Input node
n_2	Output node

The buffer block is a noiseless unity-gain isolation stage intended for use with baseband signals. The input impedance is ∞ whereas the output impedance is 10Ω which mimics a voltage-source output.

3.28 Template of Phase Noise Requirements

tplt filename

Provides a phase noise power spectral density which can be used to specify the phase noise requirements.

3.29 PLL Voltage-Controlled Oscillator 1 (Leeson's Model)

vco1 $n_1 n_2 K_{vHzV} NF_{dB} P_{dBm} f_o Q_L f_{one}$

n_1	Tuning port
n_2	Oscillator output
K_{vHzV}	Tuning sensitivity, Hz/V
NF_{dB}	Active device noise figure, dB
P_{dBm}	Resonator power, dBm
f_o	Oscillator carrier frequency, Hz
Q_L	Resonator's loaded-Q
f_{one}	1/f corner frequency, Hz

The VCO is modeled as an ideal integrator of its applied tuning voltage scaled by its characteristic gain ($2\pi K_{vHzV}$ in Hz/sec/V) along with an additive random phase noise contribution which is given in terms of a simplified Leeson's model. This contribution is mathematically given by [9]

$$\begin{aligned} \mathcal{L}_{vco}(f) &= 10 \log_{10} \left\{ \frac{F k_B T_o}{2P_o} \left(1 + \frac{f_{one}}{f} \right) \left[1 + \left(\frac{f_o}{2Q_L f} \right)^2 \right] \right\} \text{ dBc/Hz} \\ &= L_0 + 10 \log_{10} \left(1 + \frac{L_1}{f} + \frac{L_2}{f^2} + \frac{L_3}{f^3} \right) \text{ dBc/Hz} \end{aligned} \tag{41}$$

where

- F Oscillator active device's *noise factor*
- $k_B T_o$ Boltzmann constant time absolute temperature
- P_o Power extracted from the oscillator's resonator
- f_{one} 1/f corner frequency for the active device
- Q_L Resonator's loaded-Q
- f_o Oscillator's center frequency

$$L_0 = 10 \log_{10} \left(\frac{F k_B T_o}{2P_o} \right) \tag{42}$$

$$L_1 = f_{1/f}$$

$$L_2 = \left(\frac{f_o}{2Q_L} \right)^2 \tag{43}$$

$$L_3 = \left(\frac{f_o}{2Q_L} \right)^2 L_1$$

In the context of the circuit simulation model for the VCO shown in Figure 32,

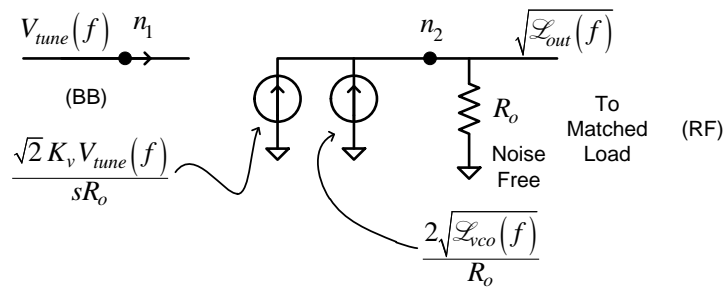


Figure 32 Circuit simulation model for VCO1 with phase noise where $K_v = 2\pi K_{vHzV}$

3.30 PLL Voltage-Controlled Oscillator 2

vco2 n₁ n₂ K_{vHzV} filename

n ₁	Tuning port
n ₂	Oscillator output
K _{vHzV}	VCO tuning sensitivity, Hz / V
filename	Filename for VCO self-noise power spectral density

The model for this VCO is very similar to vco1 except that the VCO's self-noise is given by a power spectral density file (which is interpolated by the program) rather than by using Leeson's model. In this respect, the models are identical (Figure 33 versus Figure 32). The phase noise is given by a file / table of values having the form [frequency offset, dBc/Hz] which are subsequently interpolated (on a log-frequency scale) within the program.

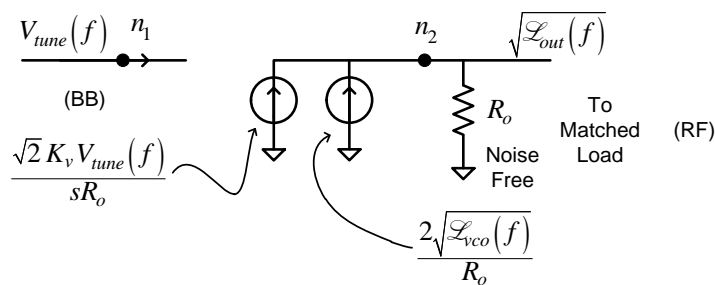


Figure 33 Circuit simulation model for VCO2 with phase noise where $K_v = 2\pi K_{vHzV}$

3.31 PLL Voltage-Controlled Oscillator 3

vco3 n₁ n₂ n₃ K_{vHzV} filename

n ₁	Tuning port
n ₂	Power supply pushing-port
n ₃	Oscillator output
K _{vHzV}	VCO tuning sensitivity, Hz / V
K _{vpHzV}	VCO pushing sensitivity, Hz / V
filename	Filename for VCO self-noise power spectral density

This VCO model is identical to vco2 except that an additional port for modeling power supply pushing has been added. This port assumes that baseband noise is potentially affecting the VCO's phase noise performance.

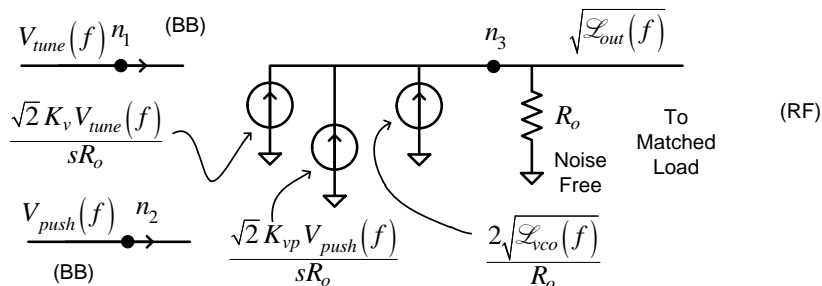


Figure 34 VCO3 model which includes the VCO pushing-port

4 Function Calls

In general, all of the functional call names are at most 4 letters in length. All fields must be delimited by at least one space and begin in column one in the text file. Line order in the circuit parameter file does not matter.

Table 1 Function Call Syntax ($R_o = 50\Omega$)

Cell #	Call Syntax	R_{in}	R_{out}	Parameter Details
1	fmin f	NA	NA	Minimum Fourier offset frequency for analysis, Hz
2	fmax f	NA	NA	Maximum Fourier offset frequency for analysis, Hz
3	Npts N	NA	NA	Number of frequency points to use in frequency analysis sweep
4	adc1 $\pm n_1$ n_2 f_{clock} , N_{bits} f_{sig} HR_{dB} σ_a psd_{clock}	R_o	1Ω	Analog-to-Digital Converter: n_1 : Input node (\pm sign for phase noise add/sub) n_2 : Output Node (1Ω) f_{clock} : Sampling clock rate, Hz N_{bits} : Number of quantization bits f_{sig} : Input carrier signal, Hz HR_{dB} : Headroom relative to full-scale, dB (≥ 0) σ_a : Internal aperture jitter, sec RMS psd_{clock} : File containing clock's phase noise psd
5	adc2 $\pm n_1$ n_2 n_3 f_{clock} , N_{bits} f_{sig} HR_{dB} σ_a	R_o	1Ω	Analog-to-Digital Converter: n_1 : Input node (R_o) (\pm sign for add/sub) n_2 : Output Node (1Ω) n_3 : Clock node (High-Z) f_{clock} : Sampling clock rate, Hz N_{bits} : Number of quantization bits f_{sig} : Input carrier signal, Hz HR_{dB} : Headroom relative to full-scale, dB (≥ 0) σ_a : Internal aperture jitter, sec RMS
6	att n_1 n_2 P_{dBm} L_{dB}	R_o	R_o	RF Attenuator: n_1 : Input node n_2 : Output node P_{dBm} : Input carrier level, dBm L_{dB} : Attenuation in matched 50 Ohm system, dB
7	cap n_1 n_2 C	NA	NA	Capacitor: n_1 , n_2 : Capacitor nodes C : Capacitance value, F
8	div n_1 n_2 N NF_{dB} P_{dBm} f_{one} L_{dBc}	R_o	R_o	Digital Divider: n_1 : Input node n_2 : Output node N : Divide ratio to be used NF_{dB} : Input-referred noise figure P_{dBm} : Input carrier level, dBm f_{one} : $1/f$ corner frequency, Hz L_{dBc} : Minimum output phase noise floor, dBc/Hz

Cell #	Call Syntax	R _{in}	R _{out}	Parameter Details
9	divf n ₁ n ₂ N NF _{dB} P _{dBm} f _{one} L _{dBc} M f _{ref}	R _o	R _o	Fractional-N Digital Divider: n ₁ : Input node n ₂ : Output node N : Divide ratio to be used NF _{dB} : Input-referred noise figure P _{dBm} : Input carrier level, dBm f _{one} : 1/f corner frequency, Hz L _{dBc} : Minimum output phase noise floor, dBc/Hz M : Δ-Σ order f _{ref} : Δ-Σ update rate, f _{ref} , Hz
10	dds1 ±n ₁ n ₂ f _{clock} , N _{bits} f _{sig} σ _a psd _{clock}	∞	R _o	Direct-Digital Synthesizer: n ₁ : Input node (±sign for phase noise add/sub) n ₂ : Output Node f _{clock} : Sampling clock rate, Hz N _{bits} : Number of quantization bits f _{sig} : Output carrier signal, Hz σ _a : Associated DAC aperture jitter, sec RMS psd _{clock} : File containing clock's phase noise psd
11	dds2 ±n ₁ n ₂ n ₃ f _{clock} N _{bits} f _{sig} σ _a	∞	R _o	Direct-Digital Synthesizer: n ₁ : Input node (±sign for phase noise add/sub) n ₂ : Output Node n ₃ : Clock input node f _{clock} : Sampling clock rate, Hz N _{bits} : Number of quantization bits f _{sig} : Output carrier signal, Hz σ _a : Associated DAC aperture jitter, sec RMS
12	dly n ₁ n ₂ τ _d	R _o	R _o	Time Delay: Pure Time Delay n ₁ : Input node n ₂ : Output node τ _d : Time delay
13	fds n ₁ n ₂ τ _d K _{fd} NF _{dB} P _{dBm}	R _o	1Ω	Frequency Discriminator: n ₁ : Input node n ₂ : Output node τ _d : Discriminator's time delay, sec K _{fd} : Frequency discriminator's gain, V / rad NF _{dB} : Input-referred noise figure, dB P _{dBm} : Input signal power, dBm
14	fil n ₁ n ₂ f _c N Lmax _{dB} P _{dBm} τ _g IL _{dB}	R _o	R _o	Filter: (Butterworth Always Assumed) n ₁ : Input node n ₂ : Output node f _c : Filter corner frequency, Hz (RF BW/2) N : Filter order (lowpass equivalent) Lmax _{dB} : Maximum filter attenuation possible, dB P _{dBm} : Input carrier level, dBm τ _g : Nominal group delay through filter, sec IL _{dB} : Insertion loss, dB
15	fmx n ₁ n ₂ N P _{dBm} NF _{dB} f _{one}	R _o	R _o	Frequency Multiplier: n ₁ : Input node n ₂ : Output node N : Frequency multiplication factor P _{dBm} : Input carrier power, dBm NF _{dB} : Input-referred noise figure, dB f _{one} : Flicker frequency corner, Hz

Cell #	Call Syntax	R _{in}	R _{out}	Parameter Details
16	ind n ₁ n ₂ L	NA	NA	Inductor: n ₁ , n ₂ : Inductor nodes L : Inductor value, H
17	mod n ₁ n ₂ K	∞	R _o	Linear Modulator: n ₁ : Baseband input node n ₂ : Output RF port K : Conversion factor rad/V
18	mxr ±n ₁ ±n ₂ n ₃ P _{LO} P _{RF} f _{one} NF _{RF} NF _{LO}	R _o	R _o	RF Mixer: n ₁ : RF input port (±sign for phase) n ₂ : LO input port (±sign for phase) n ₃ : Output port P _{LO} : Local oscillator power level, dBm P _{RF} : Input signal carrier level, dBm f _{one} : 1/f corner frequency for LO-port noise, Hz NF _{RF} : Effective noise figure for RF port, dB NF _{LO} : Effective noise figure for LO port, dB
19	opa n ₁ n ₂ n ₃ G _{dB} f _{dp} vnfile infile	∞	10Ω	Op-Amp: n ₁ , n ₂ : Positive and negative nodes of differential input n ₃ : Output voltage node of the op-amp G _{dB} : Maximum op-amp gain, at DC, dB f _{dp} : Dominant pole frequency for op-amp vnfile: File name for equivalent input voltage noise table infile: File name for equivalent input current noise table
20	pdcp ±n ₁ ±n ₂ n ₃ K _d FoM f _{one} f _{ref}	R _o	∞	Phase Detector with Charge-Pump: n ₁ : f _{ref} port (±sign for phase) n ₂ : Feedback port (±sign for phase) n ₃ : Charge-pump output port K _d : Phase detector gain, A / rad FoM : Figure of Merit, dBc/Hz f _{one} : 1/f corner frequency, Hz f _{ref} : Reference frequency, Hz
21	pdmx ±n ₁ ±n ₂ n ₃ K _d P _{LO} P _{RF} f _{one} NF _{RF} NF _{LO}	R _o	10Ω	Phase Detector: Mixer Type: n ₁ : RF input port (±sign for phase) n ₂ : LO input port (±sign for phase) n ₃ : Output port K _d : Phase detector gain, V / rad P _{LO} : Local oscillator power level, dBm P _{RF} : Input signal carrier level, dBm f _{one} : 1/f corner frequency for LO-port noise, Hz NF _{RF} : Effective noise figure for RF port, dB NF _{LO} : Effective noise figure for LO port, dB
22	pdvo ±n ₁ ±n ₂ n ₃ K _d FoM f _{one} f _{ref}	R _o	10Ω	Phase Detector: Digital Voltage-Out: n ₁ : f _{ref} port (±sign for phase) n ₂ : Feedback port (±sign for phase) n ₃ : Output port K _d : Phase detector gain, V / rad FoM : Figure of Merit, dBc/Hz f _{one} : 1/f corner frequency, Hz f _{ref} : Reference frequency, Hz

Cell #	Call Syntax	R _{in}	R _{out}	Parameter Details
23	prb n ₁ title	∞	NA	Phase Noise Probe (High Input Impedance Type): n ₁ : Node to probe title: Name for probe point
24	res n ₁ n ₂ ±R	NA	NA	Resistor: n ₁ : Positive node n ₂ : Negative node R : Resistor value (Ohms), < 0 if noiseless
25	rfa n ₁ n ₂ NF _{dB} P _{dBm} f _{one}	R _o	R _o	RF Amplifier: n ₁ : Input node n ₂ : Output node NF _{dB} : Noise figure, dB P _{dBm} : Input carrier power, dBm f _{one} : 1/f corner frequency, Hz
26	split n ₁ n ₂ n ₃	R _o	R _o	Lossless Splitter: n ₁ : Input port n ₂ : Output port #1 n ₃ : Output port #2
27a	src1 n ₁ psdfile	NA	R _o	Precision RF Reference Source: n ₁ : Node for source Phase noise density versus frequency offset given in file <i>psdfile</i> . Format is [frequency offset (Hz), dBc/Hz].
27b	src2 n ₁ P _{carr} f _{one} L _{ped} f _c	NA	R _o	Precision RF Reference Source: n ₁ : Node for source P _{carr} : Carrier power level, dBm f _{one} : 1/f corner frequency, Hz L _{ped} : Phase noise pedestal level, dBc/Hz f _c : Phase noise pedestal corner frequency, Hz
28	sum ±n ₁ ±n ₂ n ₃	∞	10Ω	Sum Node: (± indicate sign of input to assume) n ₁ : Input #1 n ₂ : Input #2 n ₃ : Output
29	tplt filename	NA	NA	Design goal power spectral density. File entry identical to that used for <i>src</i>
30	vbuf n ₁ n ₂	∞	10Ω	Ideal Voltage Buffer: n ₁ : Input voltage node n ₂ : Output voltage node
31	vco1 n ₁ n ₂ K _v NF _{dB} P _{dBm} f _o Q _L f _{one}	∞	R _o	Voltage-Controlled Oscillator: n ₁ : Frequency tuning port n ₂ : Oscillator output port K _v : Tuning sensitivity in Hz / V NF _{dB} : Device noise figure, dB P _{dBm} : Power extracted from resonator, dBm f _o : Oscillator frequency, Hz Q _L : Resonator loaded-Q f _{one} : Flicker corner frequency, Hz
32	vco2 n ₁ n ₂ K _v filename	∞	R _o	Voltage-Controlled Oscillator: n ₁ : Frequency tuning port n ₂ : Oscillator output port K _v : Tuning sensitivity, Hz / V filename: PSD tabular description of self-noise. Format is [frequency offset (Hz), dBc/Hz].

Cell #	Call Syntax	R _{in}	R _{out}	Parameter Details
33	vco2 n ₁ n ₂ n ₃ K _v K _{vp} filename	∞	R _o	Voltage-Controlled Oscillator: n ₁ : Frequency tuning port n ₂ : Oscillator output port n ₃ : Power supply (pushing) port K _v : Tuning sensitivity, Hz / V K _{vp} : Oscillator pushing sensitivity, Hz / V filename: PSD tabular description of self-noise. Format is [frequency offset (Hz), dBc/Hz].