Part 1

Understanding the specifics of sampling in synthesis

Phase-locked loops using sampling techniques offer big benefits in synthesizer performance. A better understanding of these techniques leads to better results.

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EARLY phase-locked loop (PLL) frequency synthesizers relied exclusively on continuous loop analysis and design. This trend for loop analysis in the continuous time domain has crept into the analysis of discontinuous sampled loops as well, even though this is correct only when the loop bandwidth is much less than the reference frequency. Rigorous analysis[1] has shown that continuous loop analysis must be abandoned for sampled loop analysis when the ratio of loop bandwidth to reference frequency is greater than about 1:6. Obviously, as the use of sampling spreads throughout the design community, a better understanding of sampling techniques is needed to correct possible misconceptions.

The many benefits of sampling are largely responsible for its increased use in frequency synthesizers. Digital phase detectors have significantly better capture range than their mixer counterparts. They also lend themselves easily to interfacing with digital divide-by-N counters, which are often used in the feedback portion of the control loop. Sampled PLL systems can also provide faster lock times for a given closed-loop bandwidth than the equivalent bandwidth in a continuous system. This can be the determining factor in systems that require fast phase-locking performance combined with the small loop bandwidth that may be necessary to keep the multiplied reference phase noise on the output signal as narrow as possible.

Control system analysis

Basically, any synthesizer that uses a digital divider in the feedback path of the control loop is essentially a sampled control system. New phase-error information is presented to the phase detector at discrete times because all of the phase-error information resides in the zero crossings of the feedback divider output. Most early PLLs were purposely designed with a loop bandwidth that was much less

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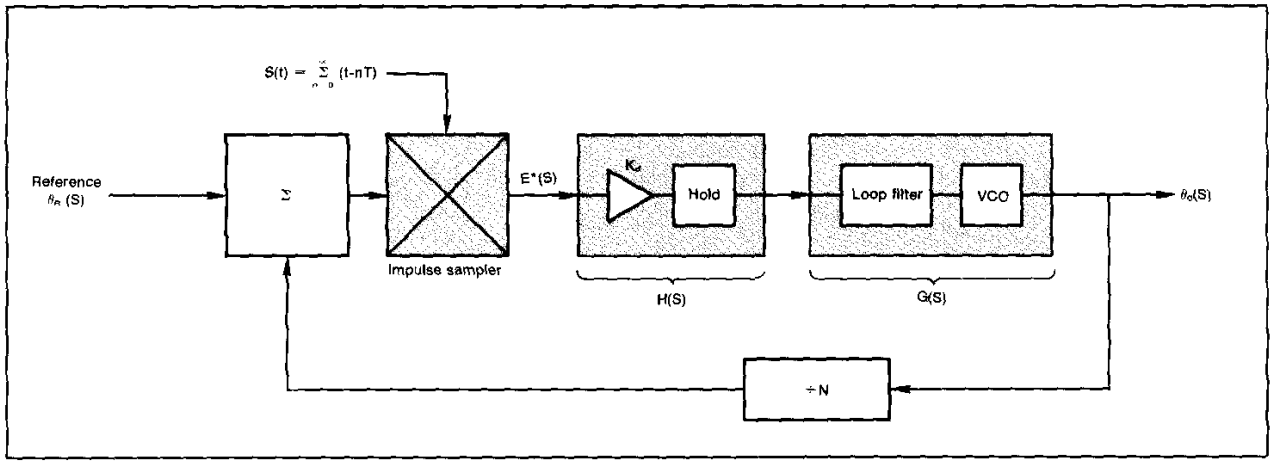

1. The general sampled PLL employs *an ideal impulse sampler that must be followed by some form of "hold" device, H(s).*

than the loop-reference frequency, and sampling effects could therefore be ignored.

A sampled PLL is shown in Fig. 1. Sampling is performed by the ideal impulse sampler whose output transform is represented by E*(s). The * denotes the input function as sampled in the time domain. Ideally, the function e*(t) is an infinite train of uniformly spaced impulses whose amplitudes vary with time. In order for the remaining analog electronics in the control loop to make use of this error signal, the sampler must be followed by some form of "hold" device that retains at least part of the error information between sampling instants. This hold device may take the form of a simple RC filter or a sophisticated true sample-and-hold circuit. This function is represented by H(s) in Fig. 1. K_d is the phase detector gain in volts per radian, and K_v is the VCO sensitivity in radians per second per volt.

As in continuous system analysis, the control system of Fig. 1 is most easily analyzed by solving for the sampled phase-error function E*(s). Use of the general transfer functions H(s) and G(s) will make the results applicable to any PLL. As a first step in the analysis, the phase-error function may be stated as

$$E^*(s) = [\theta_r(s) - \theta_o(s)/N]^* \quad (1)$$

$$E^*(s) = \left[\theta_r(s) - \frac{E^*(s)G(s)H(s)}{N}\right]^* \quad (2)$$

A basic theorem of sampled control systems[2] allows the sampling operation in Eq. 2 to be moved within the outer brackets, resulting in

$$E^*(s) = \theta_r^*(s) - \frac{E^*(s)\,GH^*(s)}{N} \quad (3)$$

The sampled error function terms may be collected in Eq. 3 to provide the sampled phase error as

$$E^*(s) = \frac{\theta_r^*(s)}{1 + GH^*(s)/N} \quad (4)$$

Equation 4 is a very important and basic result in sampled PLL analysis. The result may be extended to examine the system output phase-noise spectrum and phase-locking speed. Performance of the sampled control system is also embedded in this equation. The expression may be compared directly with the more familiar continuous control theory case by noting that if f(t) and F(s) are LaPlace transform pairs, then

$$L\{f^*(t)\} = \frac{1}{T}\sum_{n=-\infty}^{n=\infty} F(s + j\,n\omega_s) \quad (5)$$

where $W_s = 2\pi F_{ref}$ and $T = 1/F_{ref}$. Using the result, Eq. 4 may be rewritten in terms of LaPlace transforms as

$$E^*(s) = \frac{\frac{1}{T}\sum_{n=-\infty}^{n=\infty} \theta r(s+jn\omega_s)}{1+\frac{1}{NT}\sum_{n=-\infty} G(s+jn\omega_s)H(s+jn\omega_s)} \quad (6)$$

The closed-loop error for the sampled control loop given by Eq. 6 is considerably more complex than the parallel expression for the loop error in a continuous system. Continuous analysis would express this same error as

$$E(s) = \frac{\theta_r(s)}{1 + G(s)H(s)/N} \quad (7)$$

The process of sampling in the control system causes the continuous gain functions to be replaced with infinite sums of each respective term displaced about every harmonic of the sampling (reference) frequency. This is shown in Fig. 2. Sampling effects cannot be ignored where the higher order summation terms in Eq. 6 make significant contributions to the final result.

Sampling effects may be dealt with rigorously using LaPlace transforms, but in general, the infinite summations that appear as in Eq. 6 unnecessarily complicate matters. As the sampling operation is performed at a constant frequency, F_{ref}, it is advantageous to use Z-transform techniques to simplify the calculations.

Type I loops

Z-transforms are very convenient and powerful for sampled control system analysis and design because they not only generally eliminate the infinite summations that appear with LaPlace transforms, but they may also be algebraically manipulated similarly to those transforms. Substitution of each respective Z-transform may be made into Eq. 4 for any basic PLL analysis. Specifically, for the Type I sampled control loop,

$$H(s) = \frac{1-\exp(-sT)}{s} \quad (8)$$

and

$$G(s) = \frac{K_d K_v}{Ns} \quad (9)$$

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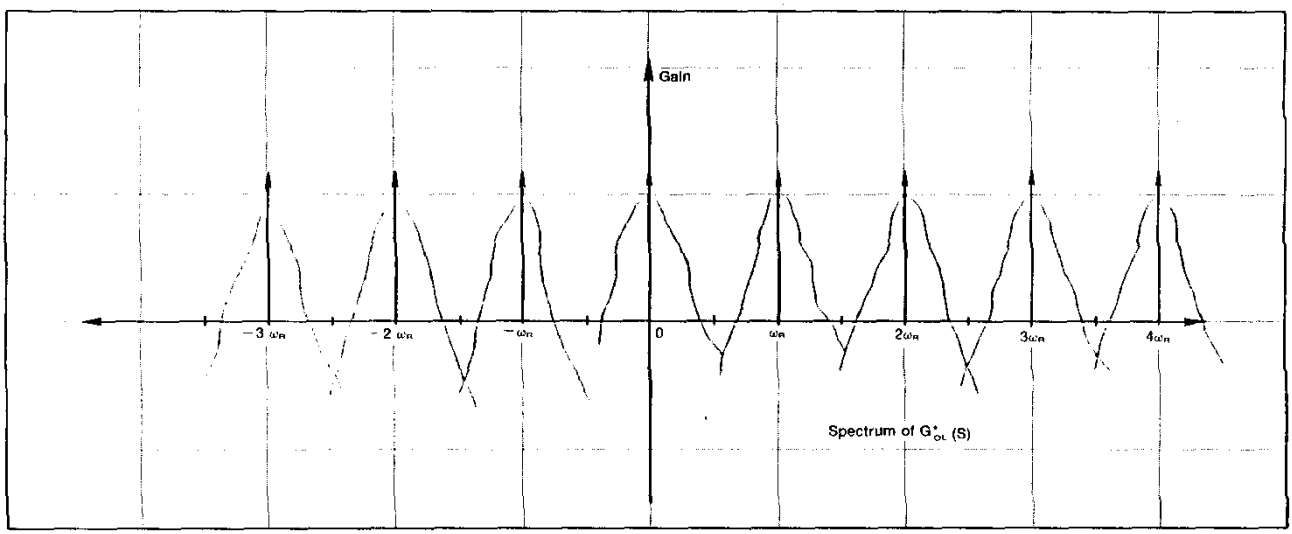

***2. Sampling causes continuous gain functions** to be replaced with infinite sums of each term, displaced around each harmonic of the sampling frequency.*

The Z-transform of H(s)G(s) is found using standard techniques:

$$Z\{H(s)G(s)\} = Z\left\{\frac{1-\exp(-sT)}{s}\,\frac{K_d K_v}{Ns}\right\} \quad (10)$$

where the $Z = \exp(sT)$ substitution has been made. The bracketed quantity's inverse LaPlace transform is simply $f(t) = t$. The corresponding Z-transform can be found in the literature[2, 3], or in standard mathematical handbooks.

$$Z\{H(s)G(s)\} = \frac{K_d K_v}{N}(1-1/Z)\,\frac{T\,Z}{(Z-1)^2} \quad (11)$$

or

$$G_{ol}(Z) = \frac{K_d K_v T}{N(Z-1)} \quad (12)$$

If the loop analysis had been performed using only LaPlace transforms, the appropriate open-loop gain transform would be

$$G_{ol}(s) = \frac{1}{T}\sum_{n=-\infty}^{n=\infty} \frac{1-\exp(-s-jn\omega_s)}{(s+jn\omega_s)^2}\,\frac{K_d\,K_v}{N} \quad (13)$$

The conditions for loop stability may be found quickly from examining Eq. 12. A sampled control system is by definition stable if all of the open-loop gain poles lie within the unit circle of the complex Z-plane. Eq. 12 has only one simple pole, which is given by

$$Z_r = 1 - \frac{K_d\,K_v\,T}{N} \quad (14)$$

For loop stability, the absolute value of Z_r must be less than 1, or (for stability)

$$\frac{K_d\,K_v\,T}{N} < 2 \quad (15)$$

The phase-locking speed may be calculated by examining the loop's error response to a step change in input frequency. For the Type I system, phase-lock is said to have occurred when the loop phase error has been reduced to within a specified tolerance of the final steady-state phase error. Following the guideline of Eq. 4, the error response for the sampled Type I loop will be

$$E(Z) = R(Z)\,\frac{1}{1+G_{ol}(Z)} \quad (16)$$

Note that in Fig. 1, the phase detector gain, K_d, is included after the sampler. Therefore, to convert the units of the error response from radians to volts, simply multiply Eq. 16 by K_d. The input error to the phase detector is represented by R(Z), which is caused by a step change in input frequency, ΔF. In the time domain, this phase error is

$$\theta_e(t) = \frac{\Delta F\,2\pi}{N}\,t \quad (17)$$

which is expressed in the Z-transform domain as

$$R(Z) = \frac{2\pi\,T\,Z}{N(Z-1)^2}\,\Delta F \quad (18)$$

Substituting Eq. 12 and Eq. 18 into Eq. 16, the loop error response is

$$E(Z) = \frac{2\pi\,\Delta F\,T\,Z}{N[Z^2 + (K-2)Z + (1-K)]} \quad (19)$$

where $K = K_d\,K_v\,T/N$.

If K is selected to be unity, a zero-beat error response occurs. This means that the steady-state final phase error occurs after only one sample period (phase-lock occurs in only one sample period).

$$E(Z) = \frac{2\pi\,\Delta F\,T}{N}\,\frac{1}{Z-1}\,K = 1 \quad (20)$$

$$e(t) = \frac{2\pi\,\Delta F}{K_d\,K_v}\,u(t-T) \text{ radians} \quad (21)$$

In the event that K is not unity, non-

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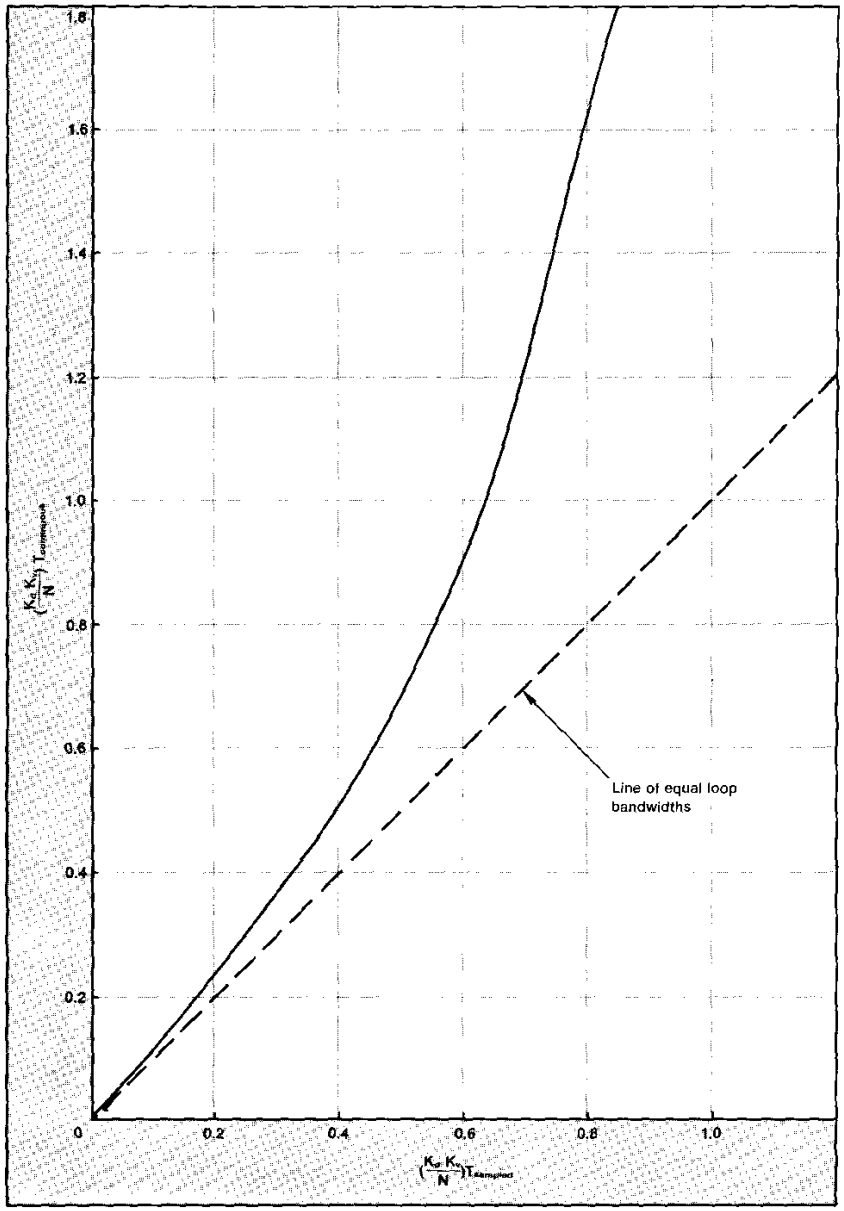

3. A comparison of continuous and sampled control system phase-locking speed *shows that as the best phase-locking condition is reached for the sampled control loop, the continuous control loop bandwidth must increase without limit in order to perform as well.*

optimum phase-locking speed occurs, and the resulting error response is

$$E(Z) = \frac{2\pi\ \Delta F\ T\ Z}{N(Z-a)(Z-b)} \qquad (22)$$

where

$a = 1$

$b = 1-K.$

The resulting phase-error time response may be found by performing the inverse Z-transform of Eq. 22, which gives

$$e(nT) = \frac{2\pi\ \Delta F}{K_d\ K_v}[1-(1-K)^n]$$

radians (23)

Analysis tools

For the design of wide-bandwidth PLL systems, significant design inaccuracies can result if continuous analysis techniques are used rather than sampled control system analysis. Designers will most likely be unaware of the possible fast zero-beat error responses possible with sampled systems; but more importantly, they will not know about the accompanying decrease in loop gain margin caused by sampling effects. If the gain margin is calculated using a continuous open-loop gain model for the speed-optimized Type I loop, the gain margin appears to be roughly 13.84 dB. Z-transform methods show that the true gain margin is only 6 dB.

The gain margin is substantially lower when calculated by sampled analysis techniques rather than by continuous methods. It is not difficult to show that the loop gain margin for a sampled loop is always calculated at one-half the reference frequency, and therefore it is not surprising that the margin is reduced about 6 dB with the inclusion of sampling effects ($n = 0$ and $n = -1$ terms in Eq. 6 contribute equally). The gain margin for an ideal sampled Type I PLL is given by

Gain Margin, dB =

$$20\ \text{Log}\ (\omega_s/(\omega_n\pi)) \qquad (24)$$

where $W_n = K_dK_v/N$.

If the PLL gain margin is very large, this gain margin inaccuracy between continuous and sampled anaylsis will have little impact on system stability and on the system output phase-noise spectrum. If the loop gain margin is small, the inclusion of sampling effects will correctly yield a loop gain-margin that is much less than the continuous analysis would indicate. Other helpful design criteria can be stated as well. The output spectral noise "peaking" at $F_{ref}/2$ will be less than 1 dB, provided the continuous system analysis shows an open-loop gain margin of at least 11.43 dB.

Phase-locking speed

Sampled and continuous Type I phase-locking speed may be compared with the analytical expressions that have been found thus far for the sampled Type I system. The error response for the continuous Type I loop can be easily calculated or found.[4] The phase detector error responses for the continuous and sampled Type I ideal loops are

$$E_c(t) = \frac{2\pi\ \Delta F}{K_v}$$

$$(1-\exp(-K_dK_v\ t/N))\ \text{volts} \qquad (25)$$

for the continuous system, and

$$E_s(t) = \frac{2\pi\ \Delta F}{K_v}$$

$$(1-(1-K)^n n)\ \text{volts} \qquad (26)$$

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for the sampled system. The sampled phase-detector error is calculable only at the sampling instants and in this case is constant between samples. The other control system error is time continuous. To compare the two systems, it is convenient to calculate which continuous system will produce phase-detector errors identical to the sampled control system at each sampling instant. For this situation, the equivalency of the two systems can be found easily by appropriately equating Eqs. 25 and 26 at the sampling instants. This is quite easy, as there is only one degree of freedom for the ideal Type I system. Equating the two error responses at the first sampling instant (t = T) demands that

$$[\exp(-T\,K_d\,K_v/N)] = \underset{\text{continuous}}{\underset{\text{sampled}}{[(1-K_dK_vT/N)]}} \qquad (27)$$

or

$$(K_d\,K_v\,T/N) = \underset{\text{continuous}}{\underset{\text{sampled}}{-\text{Log}\,(1-K_d\,K_v\,T/N)}} \qquad (28)$$

The quantity K_dK_v/N is a measure of the closed-loop bandwidth in each system and is a convenient parameter for comparison. As shown in Fig. 3, as the optimum phase-locking condition is reached for the sampled control loop, the continuous control-loop bandwidth must increase without bounds to perform phase-lock equally as fast. Here lies one of the powers of sampled control loops: the capability to perform phase-lock faster than any other control loop given a specified closed-loop bandwidth and channel spacing, 1/T.

Similar calculations have been performed[5] in the case of a Type II PLL. These calculations will be extended to Type II PLLs, as well as to phase-noise considerations and design practices leading to a working example, in the concluding article in this series. ●●

References

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