Topic: MACSET: Macroscopic Modeling of Phase-Locked Loops Used for Frequency Synthesis

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ABSTRACT:

A computer program is described which allows a designer to simulate the frequency step transient response of an arbitrary phase-locked loop which is used for frequency synthesis. A high-level library of building blocks is provided to permit a description of the candidate design including finite device slew-rates and supply voltages, nonlinear VCO tuning characteristics, and several commonly used phase detector types. The design is input in a Spice-like nodal description which permits completely arbitrary active/lumped filter designs to be included in the analysis. The program also provides a complete frequency domain analysis capability for Bode plots of important transfer function quantities with or without sampling effects. Substantial user I/O capability has been included to permit expedient design comparisons and documentation.

Introduction

A large number of simulation software tools are available on the market which permit various analyses of linear and nonlinear systems and circuits. Many of these are unsuitable for analyzing phase-locked loops as used for frequency synthesis however due to i) the inability to accommodate zero-crossing driven phase detectors, ii) requirements for vast amounts of low level circuit details which are not at issue during the system-level design phase, iii) high cost, iv) poor user interoperability, etc. Since this program is application specific, the user environment is already established as well.

A nodal description of the complete phase-locked loop is input using a full-screen editor and Spice-like format. The program is expressly written to help designers evaluate the effects of macroscopic design choices on the loop transient response. Such choices might include the loop natural frequency or damping factor, corner frequency for a post-detector 5th order elliptic lowpass filter, notch filter Q, lead-lag filter finite slew rate and gain-bandwidth requirements, etc. Normally, all but the first two choices are quite difficult to include in the loop transient analysis. Other nonlinear effects such as the behavior of a phase/frequency detector under various design conditions may also be examined.

A frequency domain analysis capability is also included to allow the designer to quickly assess gain and phase margin, reference or VCO phase noise peaking, etc. without necessarily requiring the user to enter the candidate design into yet another program to attain this information. Inclusion of sampling effects in the open loop gain function is automatically included. Having the time domain and frequency domain analyses readily available allow quick design assessments to be made or investigated.

Building Block Library

The component library may of course be appended to with additional blocks as the need arises. To date, the functional blocks which are accommodated in the analysis program MACSET are:

Voltage Controlled Oscillator
- linear/nonlinear tuning, voltage preset

Phase Detector
- Sample/Hold with finite sampling efficiency
- Phase/frequency detector

Feedback Divider (Ideal)

Active Elements
- Op-amp ideal
- Op-amp finite gain/bandwidth, slew rate, input/output Z, finite voltage supply rails, 1st two poles
- Voltage Follower
- Voltage Follower with ± Limiting

Passive Elements
- Resistors
- Capacitors
- Inductors

User input changes in the phase detector gain (S/H case only), the feedback divider ratio, or VCO preset voltage occur synchronously with the immediately following divide-by-N output zero crossing.

Phase-locked loop scenarios which use VCO offsetting or doubling of the VCO frequency, etc. must be properly massaged to permit macroscopic modeling of the design with the available library components.

Numerical Computation

The user-provided phase-locked provides a complete description of the system dynamics from which the transient response may be computed. A companion model approach is employed in the iterative solution process and the new system quantities are calculated at each time increment using an LU matrix factorization algorithm. A simple yet key point in the computational approach is that if a reference or divide-by-N zero crossing occurs during the next "normal" time increment, the integration is only performed up to the zero crossing. At such time, the phase detector outputs are appropriately changed and fixed-step integration is performed until the next such event.

Initially, a second-order variable time step Gear companion model was derived and implemented in the program. This choice led to severe numerical "ringing" with use of the phase/frequency detector because ideal square edge pulses were assumed in its model. Rather than necessitate inclusion of microscopic phase detector details such as internal delay, and finite device output slew rate (which really have negligible effect on transient response) and the correspondingly small time step increment which would be required for the interation, a backward Euler companion model approach was adopted instead.

Companion Models

The utility of companion models is best illustrated by deriving the model associated with a fixed capacitor as an example. The differential equation which describes the behavior of a fixed capacitor is

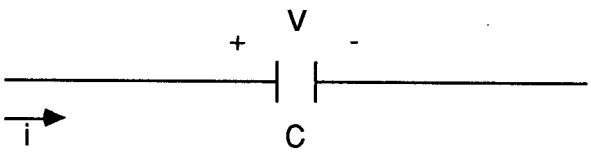

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Figure 1.

1) $$C \frac{dV}{dt} = i$$

At time instant t_{n+1}

2) $$i_{n+1} = C V'_{n+1}$$

Using backward Euler integration, the derivative may be approximated as

3) $$\frac{dV}{dt} \Big| t = t_{n+1} = V'_{n+1} \approx \frac{V_{n+1} - V_n}{h}$$

4) $$h = t_{n+1} - t_n$$

Substituting

5) $$i_{n+1} \approx \frac{C}{h} (V_{n+1} - V_n)$$

6) $$\approx \frac{C}{h} V_{n+1} - \frac{C}{h} V_n$$

Equivalently, a lumped fixed capacitor C may be represented by the time incremental model given below.

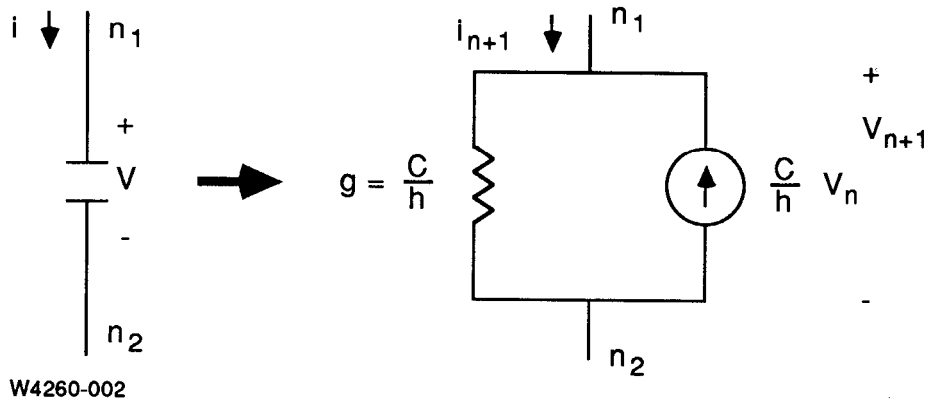

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Figure 2.

Therefore, every capacitor in the network may be replaced by a fixed conductance g in parallel with a current source. This results in a very systematic method for iteratively computing the transient response as will be shown shortly.

Similarly for fixed inductors,

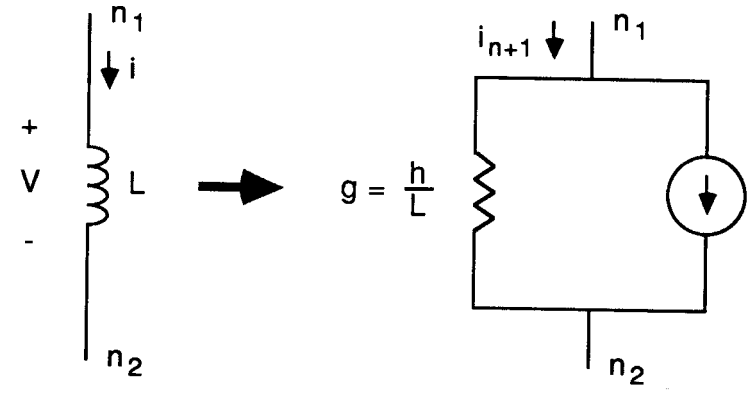

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Figure 3.

The voltage follower and limiter models are very straightforward as shown in Figures 4 and 5 respectively. Since an admittance matrix approach is used rather than a hybrid approach for solving the network node voltages at each time increment, both blocks must necessarily have finite input and output resistances. These impedances have been arbitrarily fixed to be 10^8 ohms and 1 ohm respectively.

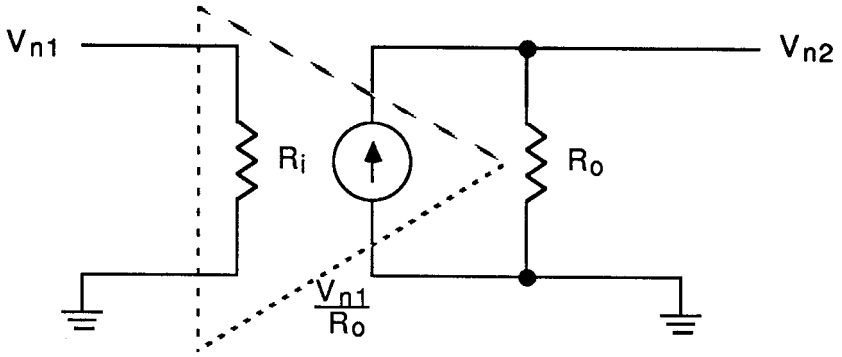

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Figure 4. Voltage Follower

The limiter action is symmetric in nature. Neither model has any finite bandwidth effects included.

The operational amplifier model is more complicated because finite slew-rate, the first two amplifier poles, finite input and output resistance, and the finite output voltage compliance range are all included.

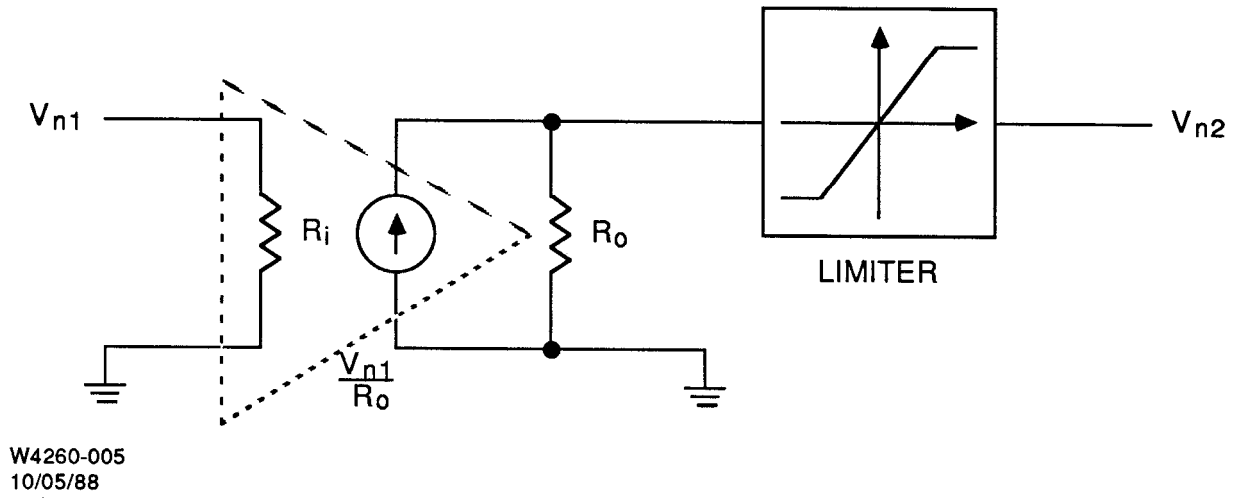

Figure 5. Ideal Symmetric Limiter

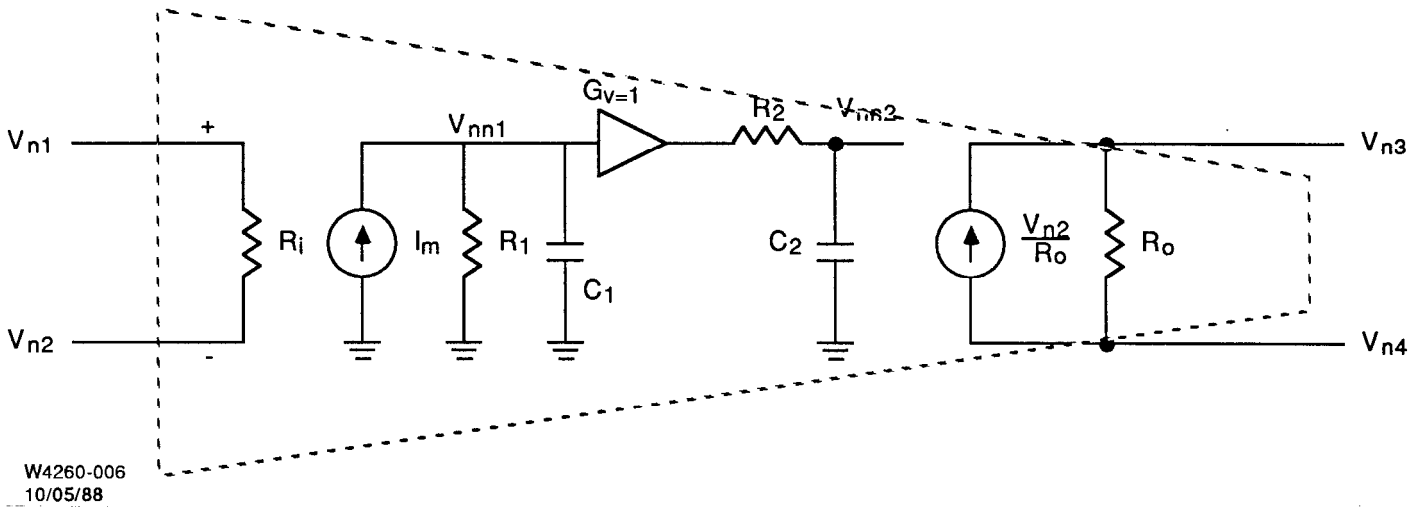

Figure 6. Operational Amplifier

The finite slew-rate is manifested in the current source Im.

Note that two internal nodes are created using this model and that both inverting and non-inverting op-amp outputs have been made accessible.

A model for the ideal operational amplifier has been included to allow easy analysis of the ideal case without resorting to very small integration time steps which would be required with the non-ideal op-amp model. Since the ideal op-amp model adds no internal nodes (e.g., V_{nn1} and V_{nn2} in the non-ideal op-amp model) the computational complexity is also reduced.

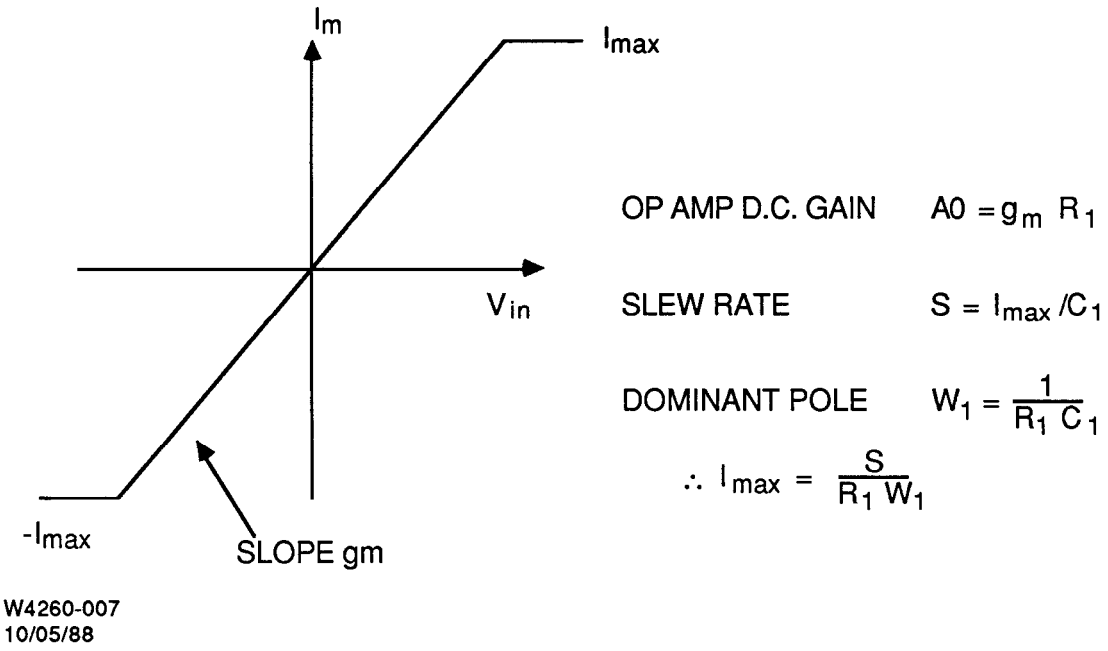

Figure 7. Current Source Im

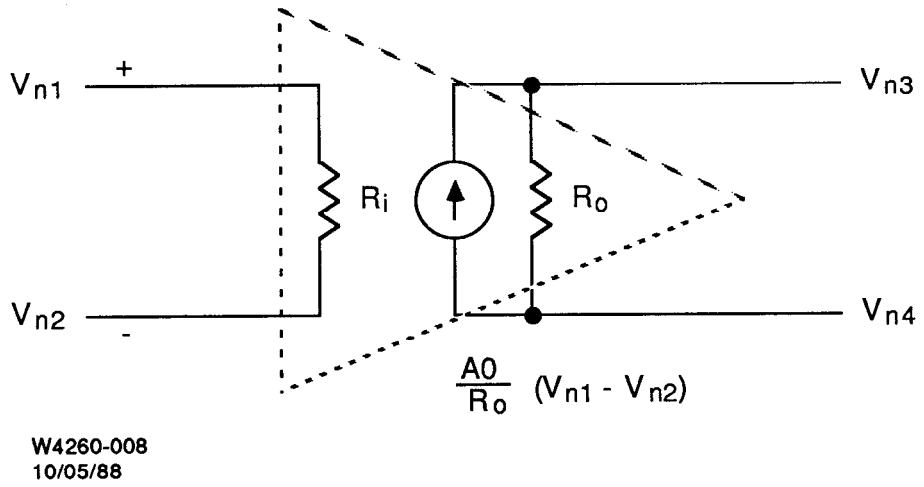

Figure 8. Ideal Operational Amplifier

At present, only two phase detector models are accommodated within the program; the sample-and-hold variety, and the classical phase/frequency detector. Other types can of course be added.

The phase/frequency detector is represented in Figure 9 where F1 and F2 are both ideal flip-flops.

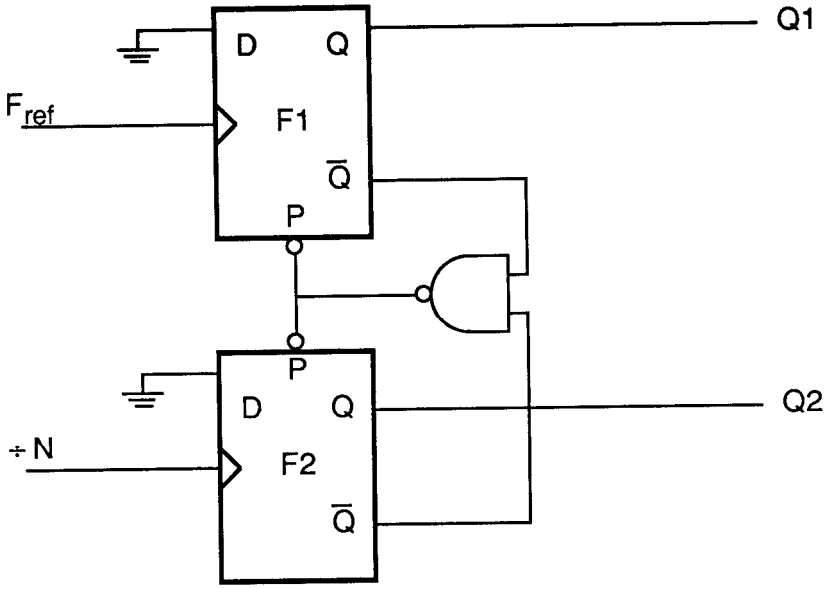

Figure 9. Phase/Frequency Detector

The TRUE and FALSE state voltages for outputs Q1 and Q2 are user-provided values from which the program automatically computes the effective phase detector gain, K_d.

Again, owing to the adopted admittance matrix description of the network, the flip-flop outputs are represented by current sources shunted by the device output resistance which is assumed to be 10 ohms.

The sample-and-hold phase detector operation is most clearly seen by using a timing diagram. Its operation is governed solely by the zero crossings of the reference and ÷ N signals.

The internal ramp is reset to V_{min} at the occurence of each F_{ref} zero-crossing. The ramp is sampled at the occurrence of a ÷ N zero crossing. Finite sampling efficiency is included in the model by making the sample-hold output dependent upon its previously held value.

7) $$V_{SH}(t_{n+1}) = V_{SH}(t_n) + \eta [V_{SHR} - V_{SH}(t_n)]$$

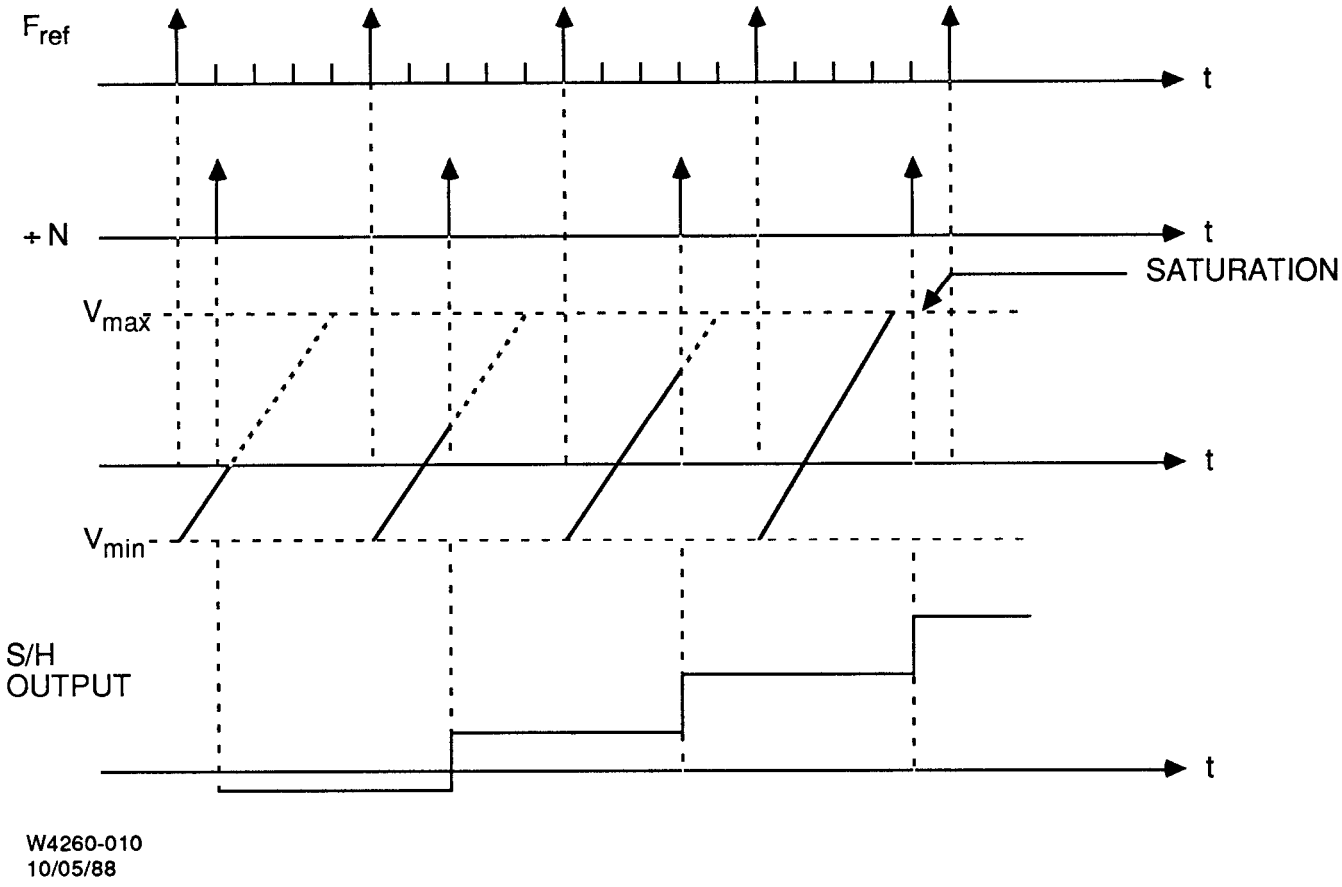

Figure 10. Sample/Hold Operation

V_{SH}	Sample/hold output voltage
V_{SHR}	Ideal ramp voltage at time t_{n+1} corresponding to ÷N zero crossing
η	sampling efficiency $0 < \eta \leq 1$

The sample/hold output impedance is assumed to be 10 ohms.

Network Iteration

Given companion models for all network elements, and the previous node voltages and inductor currents at time t_n, the new node voltages at time t_{n+1} are given by equation 8).

8) $$[\ Y\ ]\ [\ V\ (t_{n+1})\ ]\ =\ [\ I\ (V_n)\ ]$$

- $[\ Y\ ]$: Fixed network conductance matrix.
- $[\ V\ (t_{n+1})\ ]$: Nodal voltages at time t_{n+1} to be found.
- $[\ I\ (V_n)\ ]$: Network branch current sources given in companion models

The matrix equation may be solved using a variety of techniques. MACSET uses an LU factorization method to obtain the solution. Given the new node voltages, the inductor currents may be updated as required.

Frequency Domain Analysis

The frequency domain analysis is complicated by the sampling nature of the digital phase detectors involved. If a mixer were used for the phase detector, the Laplace transform techniques of continuous control systems would suffice.

The general sampled phase-locked loop employs an ideal impulse sampler which must be followed by some form of "hold" device. H(S)

A general sampled phase-locked loop is shown in Figure 11. The sampling action is performed by the ideal impulse sampler whose output transform is represented by E*(S). The * denotes that the input function has been sampled in the time domain. Ideally, the function e*(t) is an infinite train of uniformly spaced impulses whose amplitudes vary with time. In order for the remaining analog electronics in the control loop to make use of this error signal information, the sampler must be followed by some form of "hold" device which retains at least part of the error information between sampling instants. This hold device may take the form of a sample RC filter, or it may be as sophisticated as a true sample-and-hold circuit. This function is represented by H(S) in Figure 11.

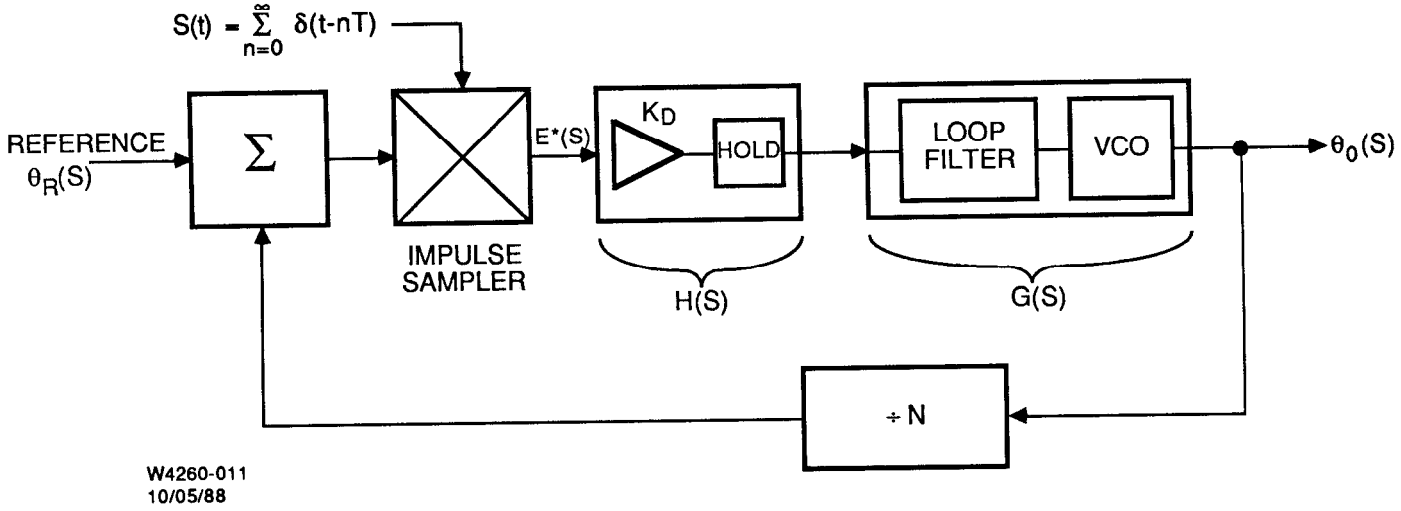

Figure 11.

As in continuous systems analysis, the control system of Figure 11 is most easily analyzed by solving for the sampled phase error function, E*(S). Use of the general transfer functions, H(S) and G(S), will make the results applicable to any phase-locked loop we may later wish to examine. As a first step in this analysis, we may write

$$E^*(S) = \left[\Theta_R(S) - \frac{\Theta_0(S)}{N}\right]^* \tag{9}$$

$$E^*(S) = \left[\Theta_R(S) - \frac{E^*(S)\,G(S)\,H(S)}{N}\right]^* \tag{10}$$

A basic theorem of sampled control systems allows the sampling operation in (10) to be moved within the outer brackets resulting in

$$E^*(S) = \Theta_R^*(S) - \frac{E^*(S)\,G^*(S)\,H^*(S)}{N} \tag{11}$$

The sampled error function terms may be collected in (11) to give the sampled phase error finally as

$$E^*(S) = \frac{\Theta^*_R(S)}{1 + \dfrac{G^*(S)\,H^*(S)}{N}} \tag{12}$$

Equation (12) is a very important and basic result for sampled phase-locked loop analysis.

This result may be extended to examine the system output phase noise spectrum and phase-locking speed performance.

Equation (12) represents the performance of a sampled control system. This expression may be compared directly with the more familiar continuous control theory case by noting that if f(t) and F(S) are Laplace transform pairs, then

$$\mathcal{L}\left[f^*(t)\right] = \frac{1}{T} \sum_{n=-\infty}^{\infty} F(S + jnW_s) \tag{13}$$

where $W_s = 2\ Pi\ F_{ref}$.

$T = 1/F_{ref}$

Using this result, equation (12) may be rewritten in terms of Laplace transforms as

$$E^*(S) = \frac{\frac{1}{T} \sum_{n=-\infty}^{\infty} \Theta_R(S + jnW_s)}{1 + \frac{1}{NT} \sum_{n=-\infty}^{\infty} G(S + jnW_s)\ H(S + jnW_s)} \tag{14}$$

The closed-loop error for the sampled control loop given by (14) is considerably more complex than the parallel expression for the loop in a continuous system. Continuous analysis would express this same error as

$$E(S) = \frac{\Theta_R(S)}{1 + \frac{G(S)\ H(S)}{N}} \tag{15}$$

The process of sampling in the control system causes the continuous gain functions to be replaced with infinite sums of each respective term displaced about every harmonic of the sampling (reference) frequency. Sampling effects cannot be ignored where the higher order summation terms in (14) make significant contributions to the final result.

Synthesizer Phase Noise

The phase noise performance of a candidate phase-locked loop frequency synthesizer may be accurately predicted using basic control theory concepts. This is possible because the noise contributions are typically very small compared to the desired signal and noise effects can therefore be conveniently power-added. A basic PLL synthesizer structure is shown in Figure 12 including the three most important noise sources which are generally considered. Other noise sources could be added as well if desired.

It is expedient in this noise analysis to once again solve for the error function, E*(S), first of all.

$$E^*(S) = \left[\Theta_R(S) - \Theta_{RN}(S) - \frac{\Theta_o(S)}{N} - \Theta_D(S)\right]^* \qquad (16)$$

The reference phase term may be ignored for the purposes of noise analysis which slightly simplifies equation (16) as

$$E^*(S) = \Theta_{RN}^*(S) - \Theta_D^*(S) - \frac{E^*(S)\,G^*(S) + \Theta_V^*(S)}{N} \qquad (17)$$

$$= \frac{\Theta_{RN}^*(S) - \Theta_o^*(S) - \Theta_V^*(S)/N}{1 + \frac{G^*(S)}{N}} \qquad (18)$$

Each noise term can be considered to be uncorrelated with respect to each other noise source. Therefore, each term may be considered independently and the end results simply power-added.

The general sampled phase-locked loop is quite similar to the continuous type except for the inclusion of the impulse sampler and internal "hold" function. Significant noise sources in the loop may be accounted for as shown.

The reference noise term effect upon the output phase noise can be found from (18) to be

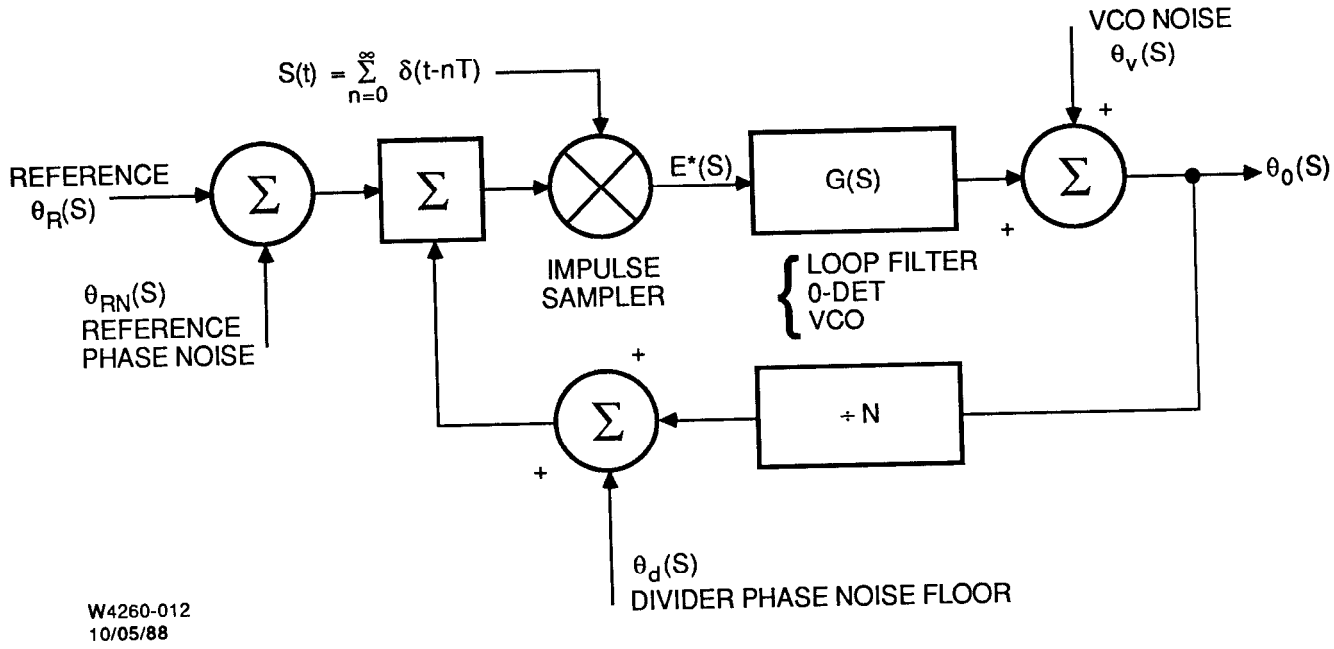

Figure 12.

$$\Theta_O(S)|_{Ref} = \frac{\Theta_{RN}^*(S)\ G(S)}{1 + \frac{G^*(S)}{N}} \tag{19}$$

In general, the phase detector cannot differentiate between feedback divider noise and reference-generated noise. The feedback contribution to the output phase noise is therefore similarly given by

$$\Theta_O(S)|_{Divider} = \frac{\Theta_d^*(S)\ G(S)}{1 + \frac{G^*(S)}{N}} \tag{20}$$

The leading minus sign has been dropped since it will not effect the final outcome.

The VCO phase noise contribution at first glance appears to be equally as simple to compute. We start out as before with the expression for E*(S). The resulting contribution to the output system phase noise is therefore

$$\Theta_o(S)|_{VCO} = \Theta_V(S) - \frac{\Theta_V^*(S)\ G(S)/N}{1 + \frac{G^*(S)}{N}} \tag{21}$$

$$= \frac{\Theta_V(S) + \left[\Theta_V(S)\ G^*(S) - \Theta^*(S)\ G(S)\ /N\right]}{1 + \frac{G^*(S)}{N}} \tag{22}$$

In general, the bracketed numerator quantity cannot be assumed to cancel to zero although this is precisely what would occur if a continuous loop analysis were assumed. For small loop bandwidths as compared to the reference frequency, the bracketed quantity may be readily ignored.

Phase Detector Transfer Functions in the Frequency Domain

The transfer function associated with an ideal zero-order sample-and-hold is

$$H(S) = \frac{1 - e^{-ST}}{S} \tag{23}$$

where T is the sampling interval. If the sample taking process is not completely efficient, the transfer function is modified to

$$H(S) = \frac{1-e^{-ST}}{S} \quad \frac{e^{ST}\ (1-A)}{e^{ST} - A} \tag{24}$$

where $A = e^{-\tau_{SH}/\tau_{RC}}$

τ_{SH} = sampling aperture, sec.

τ_{RC} = time constant of sampling bridge or switch, sec.

If the sampling action is inefficient, substantial degradation in loop gain margin can result. The H(S) function may be derived using first principles of Z-transforms.

In the case of the phase/frequency detector operating in steady-state, the phase detector outputs are ideally infinitesimal pulse widths whose areas are proportional to the prevailing phase error. The pulse widths are much less than the post-detection filter time

constants and the behavior may be modeled as ideal impulse functions driving the post-detection filter

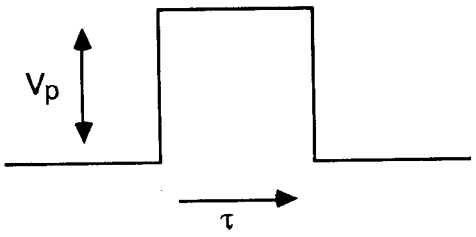

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Figure 13.

Output pulse width $\tau << T$

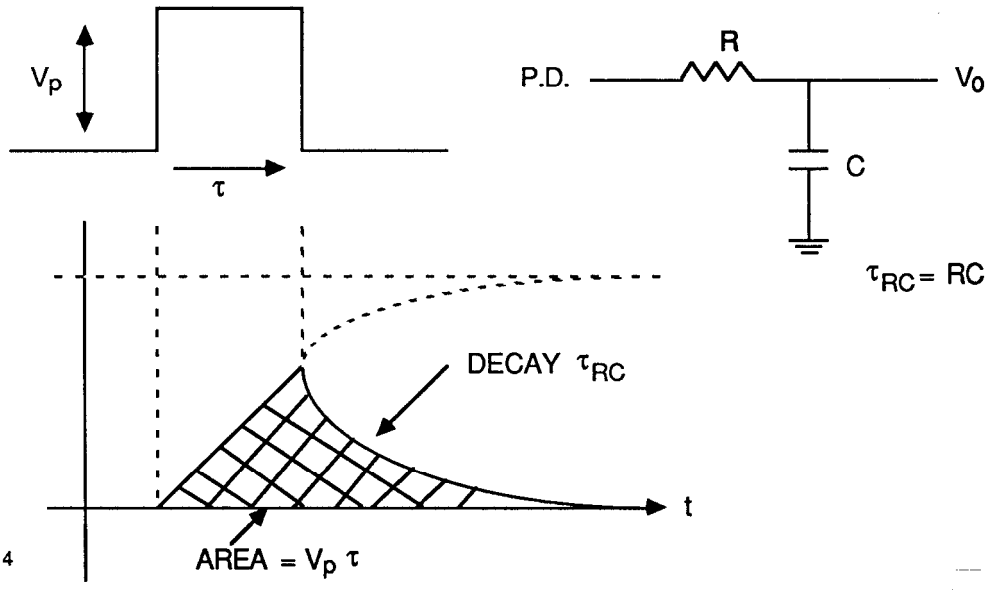
Pulse area = $V_p \tau$

As a phase detector, the DC component is

$$V_p \frac{\tau}{T} = \frac{V_p}{2\pi} 2\pi \frac{\tau}{T} = K_d \ \theta_e \qquad (25)$$

where $K_d = \frac{V_p}{2\pi}$

One property of simple RC networks is that they preserve area.



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Due to this pulse area preserving aspect, the frequency domain transfer function for the phase/frequency detector may be expressed as

$$V_o(S) = K_d \ \Theta_e(S) \ T \ D(S) \tag{26}$$

where D(S) is the normal Laplace transfer function of the output network. As developed earlier, due to the sampling action of the system, the true open-loop gain function is

$$G^*_{OL}(W) = \frac{1}{T} \sum_{n=-\infty}^{\infty} G_{OL}(w + nw_s) \tag{27}$$

The T factor due to the phase detector and the 1/T factor in $G^*_{OL}(W)$ cancel.

Analysis Example

An application requires a phase-locked loop for frequency synthesis with the following performance criteria

Frequency Range	220 MHz to 330 MHz
Channel Spacing	2 MHz
Switching Speed	< 50 μsec to 5.7°
Sampling Spurs	< -80 dBc
Phase Noise	< -140 dBc/Hz @ 10 MHz

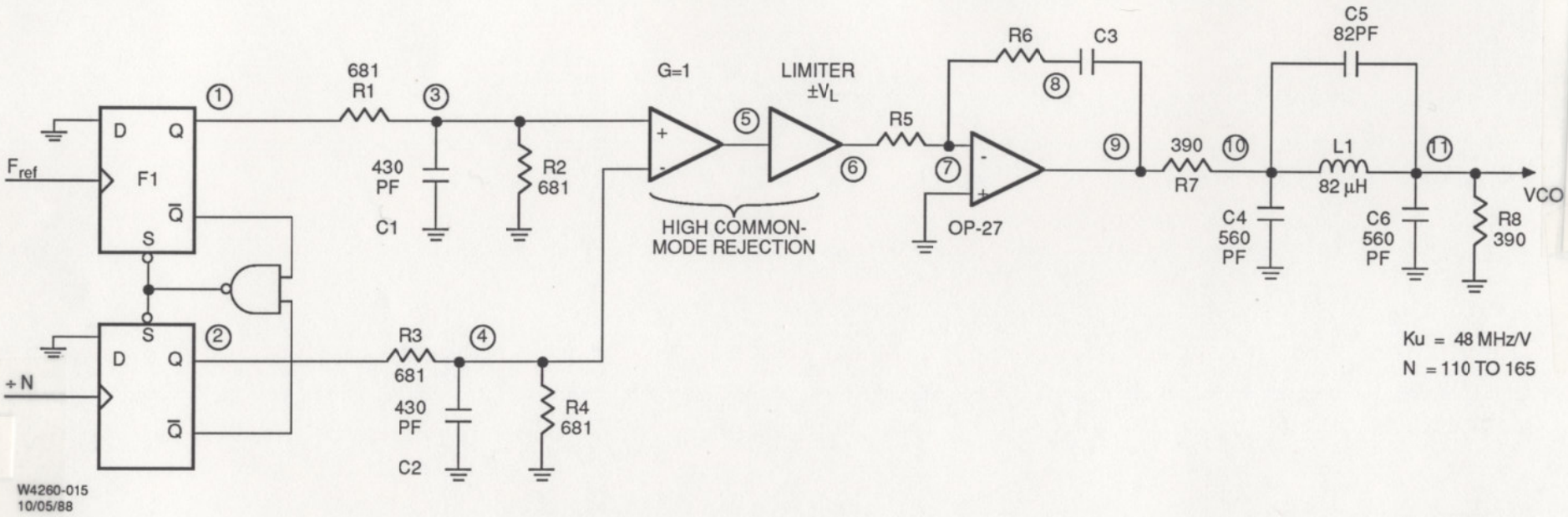
(In actuality, this example comes from a larger synthesizer design and these requirements were flowed down to this particular phase-locked loop).

Based upon some preliminary analysis, the model to be simulated was arrived at and is shown in Figure 15.

Several cases were easily simulated.

Case	w_n	ξ	(N=138)
1	56.5 KHz	0.688	
2	56.5 KHz	0.688	Post-det. τ = T/2
3	88.4 KHz	0.85	
4	88.4 KHz	0.567	
5	70.73 KHz	0.85	

The simulations clearly reveal dramatic impact upon the frequency switching speed. Relevant frequency domain analysis is shown finally for the adopted parameters, case 5.



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Model for Simulation Purposes

ASM Coarse Loop: ct1.pll

Circuit Details:

Component	Value/Index	+Node In	-Node In	+Node Out	-Node Out
r01	6.810000e+002	1	3		
r02	6.810000e+002	3	0		
c01	4.300000e-010	3	0		
r03	6.810000e+002	2	4		
r04	6.810000e+002	4	0		
c02	4.300000e-010	4	0		
o01	1.000000e+000	3	4	5	0
m01	2.000000e+000	5	6		
r05	6.800000e+002	6	7		
r06	7.600000e+002	7	8		
c03	5.100000e-009	8	9		
g01	0	0	7	9	0
r07	3.900000e+002	9	10		
c04	5.600000e-010	10	0		
l01	8.200000e-005	10	11		
c05	8.200000e-011	10	11		
c06	5.600000e-010	11	0		
r08	3.900000e+002	11	0		

Gain Block Information

Name	Ref.	Gol db	Pole 1 Hz	Pole 2 MHz	Rin M.	Rout	+Rail. V.	-Rail. V.	Slew, V/us
OP27	0	110.00	10.00	10.00	1000.00	10.00	9.00	-9.00	10.000

VCO Information:
Description: VCO
VCO is linear
VCO center frequency, MHz= 300.000000
Tuning sens., MHz/V = 48.000000
VCO Control: Node 11

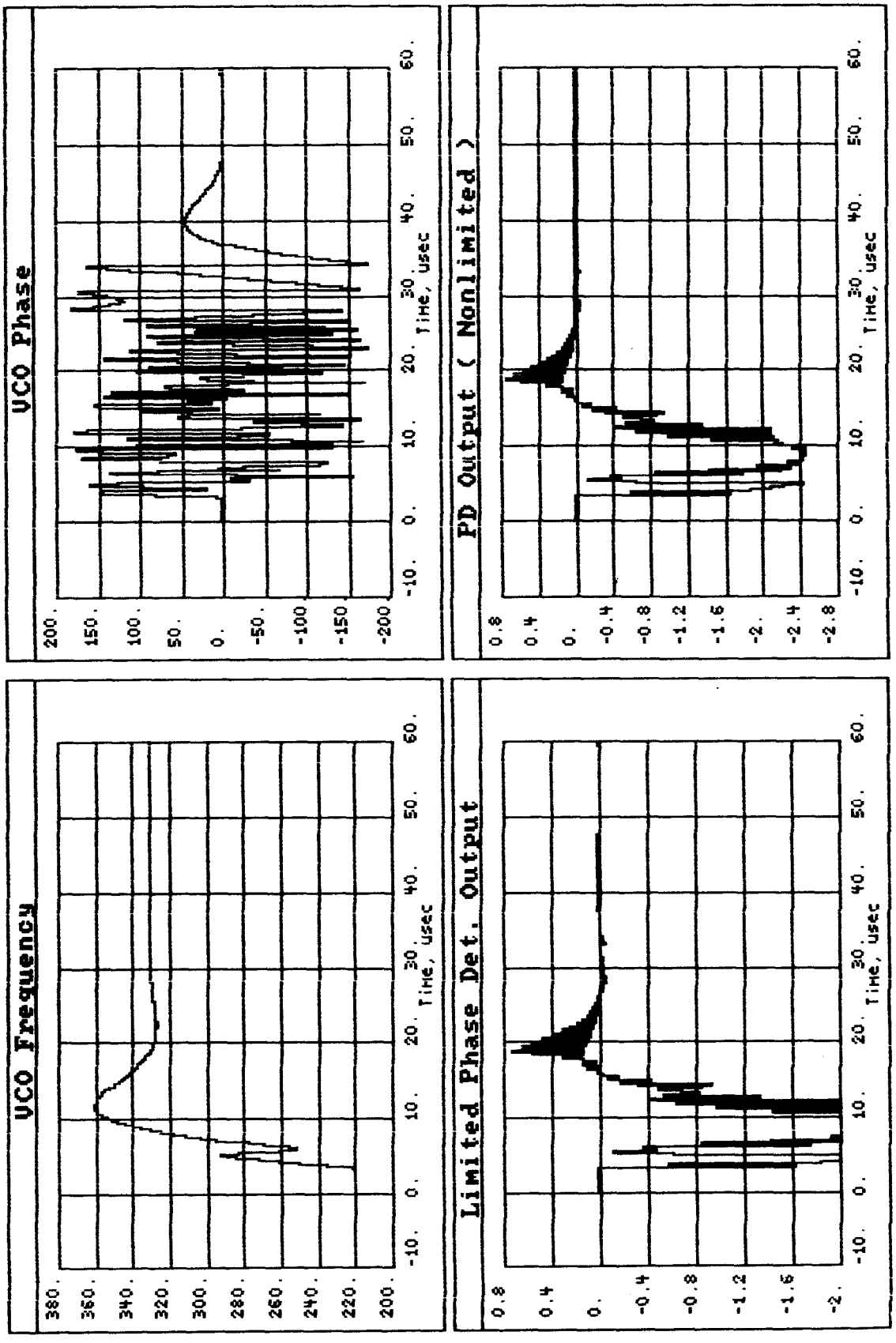
Phase Detector Information:
Description: PD
Phase/Frequency Detector; non-tri-state
Max. output voltage= 5.000000
Min. output voltage= 0.000000
Output Node (Ref.) 1
Output Node (VCO.) 2

Analysis Details:
Feedback divider ratio 165.000000
Iteration time step, usec 0.019000
PLL Reference Frequency,Hz 2.000000e+006

Case I: Hop N = 110 to 165

W_n = 56.5 KHz

ξ = 0.688



ASM Coarse Loop: ct2.pll

Circuit Details:

Component	Value/Index	+Node In	-Node In	+Node Out	-Node Out
r01	6.810000e+002	1	3		
r02	6.810000e+002	3	0		
c01	7.400000e-010	3	0		
r03	6.810000e+002	2	4		
r04	6.810000e+002	4	0		
c02	7.400000e-010	4	0		
o01	1.000000e+000	3	4	5	0
m01	2.000000e+000	5	6		
r05	6.800000e+002	6	7		
r06	7.600000e+002	7	8		
c03	5.100000e-009	8	9		
g01	0	0	7	9	0
r07	3.900000e+002	9	10		
c04	5.600000e-010	10	0		
l01	8.200000e-005	10	11		
c05	8.200000e-011	10	11		
c06	5.600000e-010	11	0		
r08	3.900000e+002	11	0		

Gain Block Information

Name	Ref.	Gol db	Pole 1 Hz	Pole 2 MHz	Rin M.	Rout	+Rail. V.	-Rail. V.	Slew, V/us
OP27	0	110.00	10.00	10.00	1000.00	10.00	9.00	-9.00	10.000

VCO Information:
Description: VCO
VCO is linear
VCO center frequency, MHz= 300.000000
Tuning sens., MHz/V = 48.000000
VCO Control: Node 11

Phase Detector Information:
Description: PD
Phase/Frequency Detector; non-tri-state
Max. output voltage= 5.000000
Min. output voltage= 0.000000
Output Node (Ref.) 1
Output Node (VCO.) 2

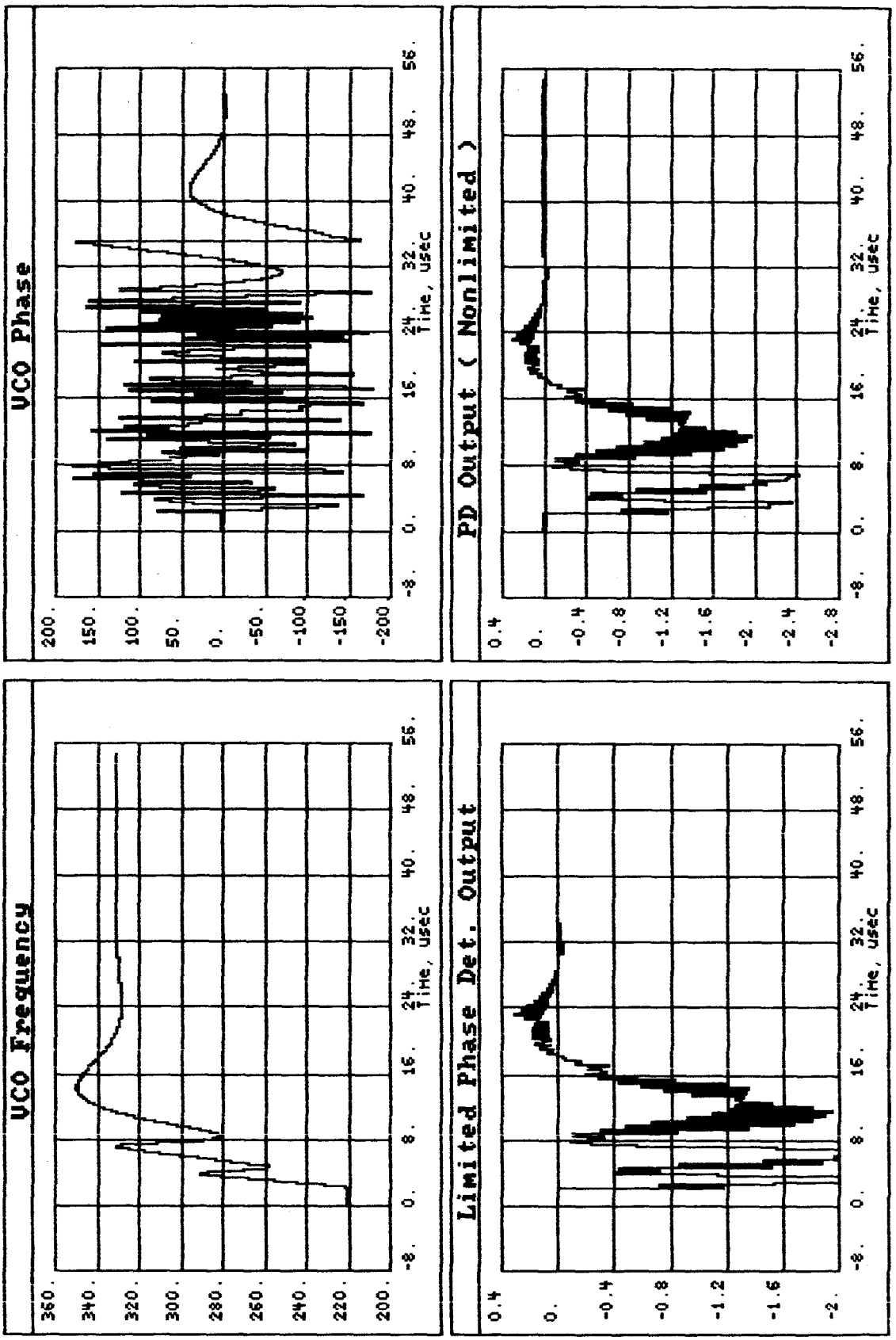
Analysis Details:
Feedback divider ratio 165.000000
Iteration time step, usec 0.019000
PLL Reference Frequency,Hz 2.000000e+006

Case II: N = 110 to 165

W_n = 56.5 KHz

ξ = 0.688

Post-Det. Filter $\tau = T_{ref}/2$



ASM Coarse Loop: ct3.pll

Circuit Details:

Component	Value/Index	+Node In	-Node In	+Node Out	-Node Out
r01	6.810000e+002	1	3		
r02	6.810000e+002	3	0		
c01	4.300000e-010	3	0		
r03	6.810000e+002	2	4		
r04	6.810000e+002	4	0		
c02	4.300000e-010	4	0		
o01	1.000000e+000	3	4	5	0
m01	2.000000e+000	5	6		
r05	2.780000e+002	6	7		
r06	6.000000e+002	7	8		
c03	5.100000e-009	8	9		
g01	0	0	7	9	0
r07	3.900000e+002	9	10		
c04	5.600000e-010	10	0		
l01	8.200000e-005	10	11		
c05	8.200000e-011	10	11		
c06	5.600000e-010	11	0		
r08	3.900000e+002	11	0		

Gain Block Information

Name	Ref.	Gol db	Pole 1 Hz	Pole 2 MHz	Rin M.	Rout	+Rail. V.	-Rail. V.	Slew, V/us
OP27	0	110.00	10.00	10.00	1000.00	10.00	9.00	-9.00	10.000

VCO Information:
Description: VCO
VCO is linear
VCO center frequency, MHz= 300.000000
Tuning sens., MHz/V = 48.000000
VCO Control: Node 11

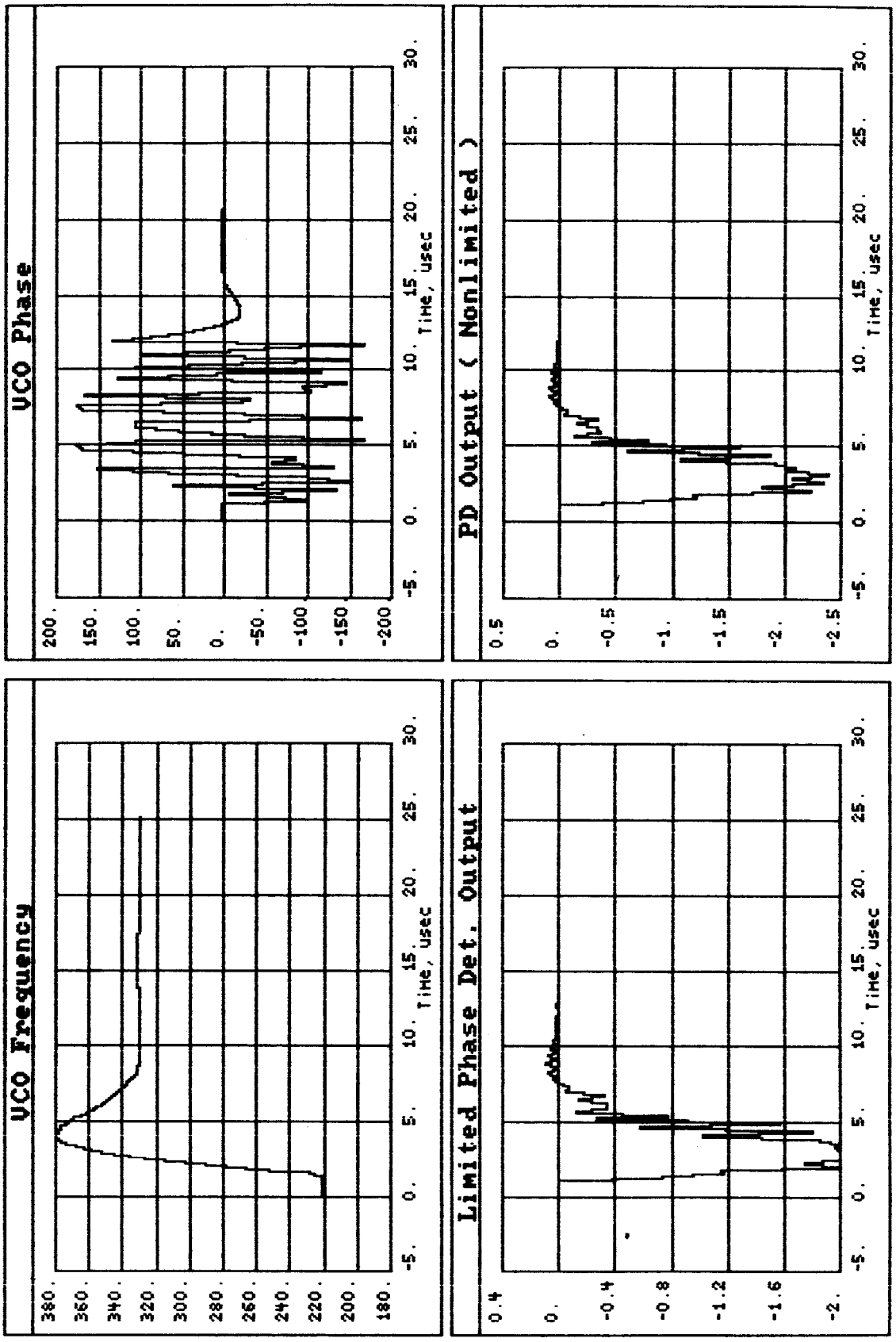
Phase Detector Information:
Description: PD
Phase/Frequency Detector; non-tri-state
Max. output voltage= 5.000000
Min. output voltage= 0.000000
Output Node (Ref.) 1
Output Node (VCO.) 2

Analysis Details:
Feedback divider ratio 110.000000
Iteration time step, usec 0.019000
PLL Reference Frequency,Hz 2.000000e+006

Case III: N = 110 to 165

W_n = 88.4 KHz

ξ = 0.85



ASM Coarse Loop; ct4.pll

Circuit Details:

Component	Value/Index	+Node In	-Node In	+Node Out	-Node Out
r01	6.810000e+002	1	3		
r02	6.810000e+002	3	0		
c01	4.300000e-010	3	0		
r03	6.810000e+002	2	4		
r04	6.810000e+002	4	0		
c02	4.300000e-010	4	0		
o01	1.000000e+000	3	4	5	0
m01	2.000000e+000	5	6		
r05	2.780000e+002	6	7		
r06	4.000000e+002	7	8		
c03	5.100000e-009	8	9		
g01	0	0	7	9	0
r07	3.900000e+002	9	10		
c04	5.600000e-010	10	0		
l01	8.200000e-005	10	11		
c05	8.200000e-011	10	11		
c06	5.600000e-010	11	0		
r08	3.900000e+002	11	0		

Gain Block Information

Name	Ref.	Gol db	Pole 1 Hz	Pole 2 MHz	Rin M.	Rout	+Rail. V.	-Rail. V.	Slew, V/us
OP27	0	110.00	10.00	10.00	1000.00	10.00	9.00	-9.00	10.000

VCO Information:
Description: VCO
VCO is linear
VCO center frequency, MHz= 300.000000
Tuning sens., MHz/V = 48.000000
VCO Control: Node 11

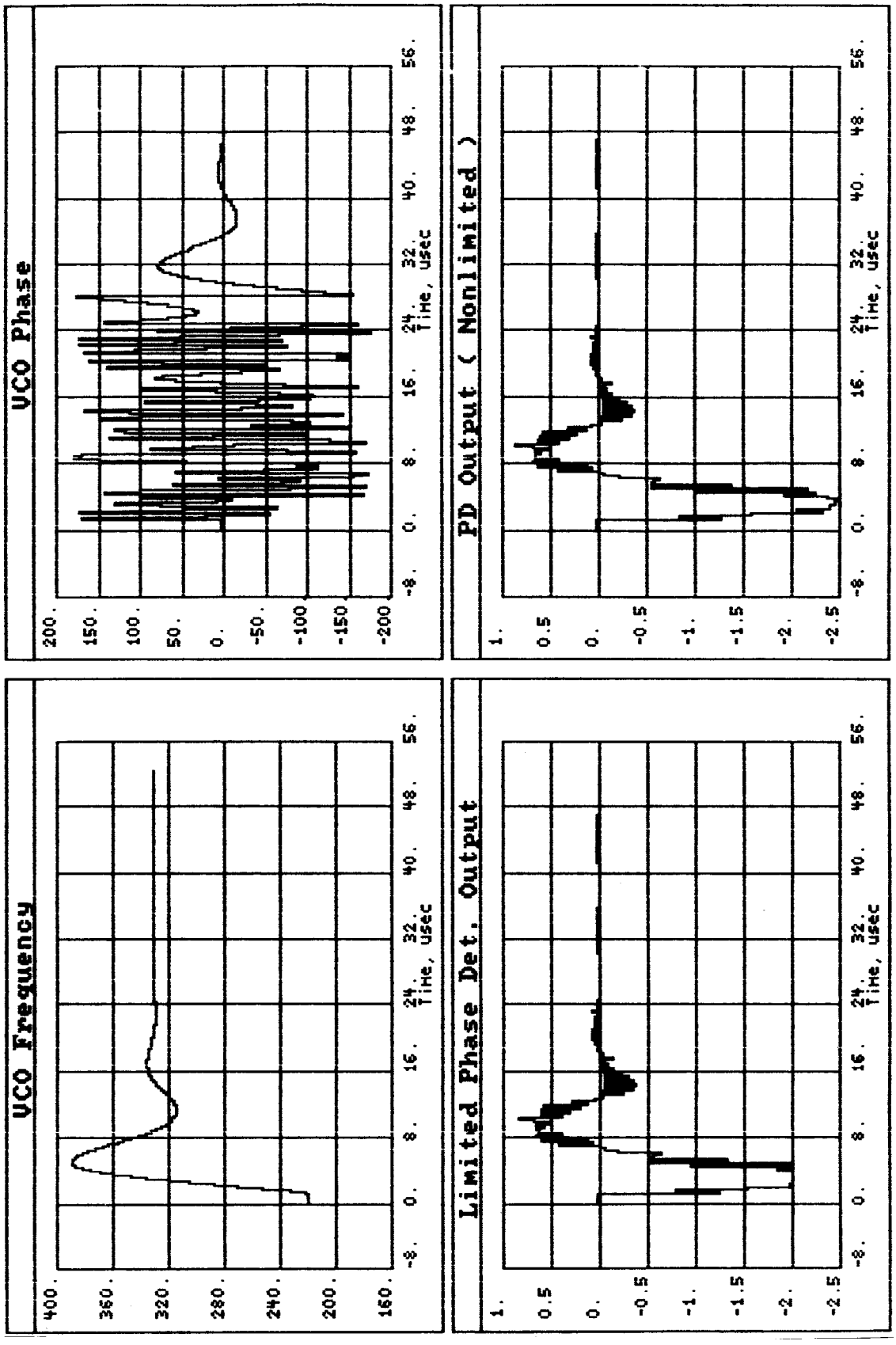
Phase Detector Information:
Description: PD
Phase/Frequency Detector; non-tri-state
Max. output voltage= 5.000000
Min. output voltage= 0.000000
Output Node (Ref.) 1
Output Node (VCO.) 2

Analysis Details:
Feedback divider ratio 110.000000
Iteration time step, usec 0.019000
PLL Reference Frequency,Hz 2.000000e+006

Case IV: ^N = 110 to 165

W_n = 88.4 KHz

ξ = 0.567



ASM Coarse Loop; ct5.pll

Circuit Details:

Component	Value/Index	+Node In	-Node In	+Node Out	-Node Out
r01	6.810000e+002	1	3		
r02	6.810000e+002	3	0		
c01	4.300000e-010	3	0		
r03	6.810000e+002	2	4		
r04	6.810000e+002	4	0		
c02	4.300000e-010	4	0		
o01	1.000000e+000	3	4	5	0
m01	2.000000e+000	5	6		
r05	4.340000e+002	6	7		
r06	7.500000e+002	7	8		
c03	5.100000e-009	8	9		
g01	0	0	7	9	0
r07	3.900000e+002	9	10		
c04	5.600000e-010	10	0		
l01	8.200000e-005	10	11		
c05	8.200000e-011	10	11		
c06	5.600000e-010	11	0		
r08	3.900000e+002	11	0		

Gain Block Information

Name	Ref.	Gol db	Pole 1 Hz	Pole 2 MHz	Rin M.	Rout	+Rail. V.	-Rail. V.	Slew, V/us
OP27	0	110.00	10.00	10.00	1000.00	10.00	9.00	-9.00	10.000

VCO Information:
Description: VCO
VCO is linear
VCO center frequency, MHz= 300.000000
Tuning sens., MHz/V = 48.000000
VCO Control: Node 11

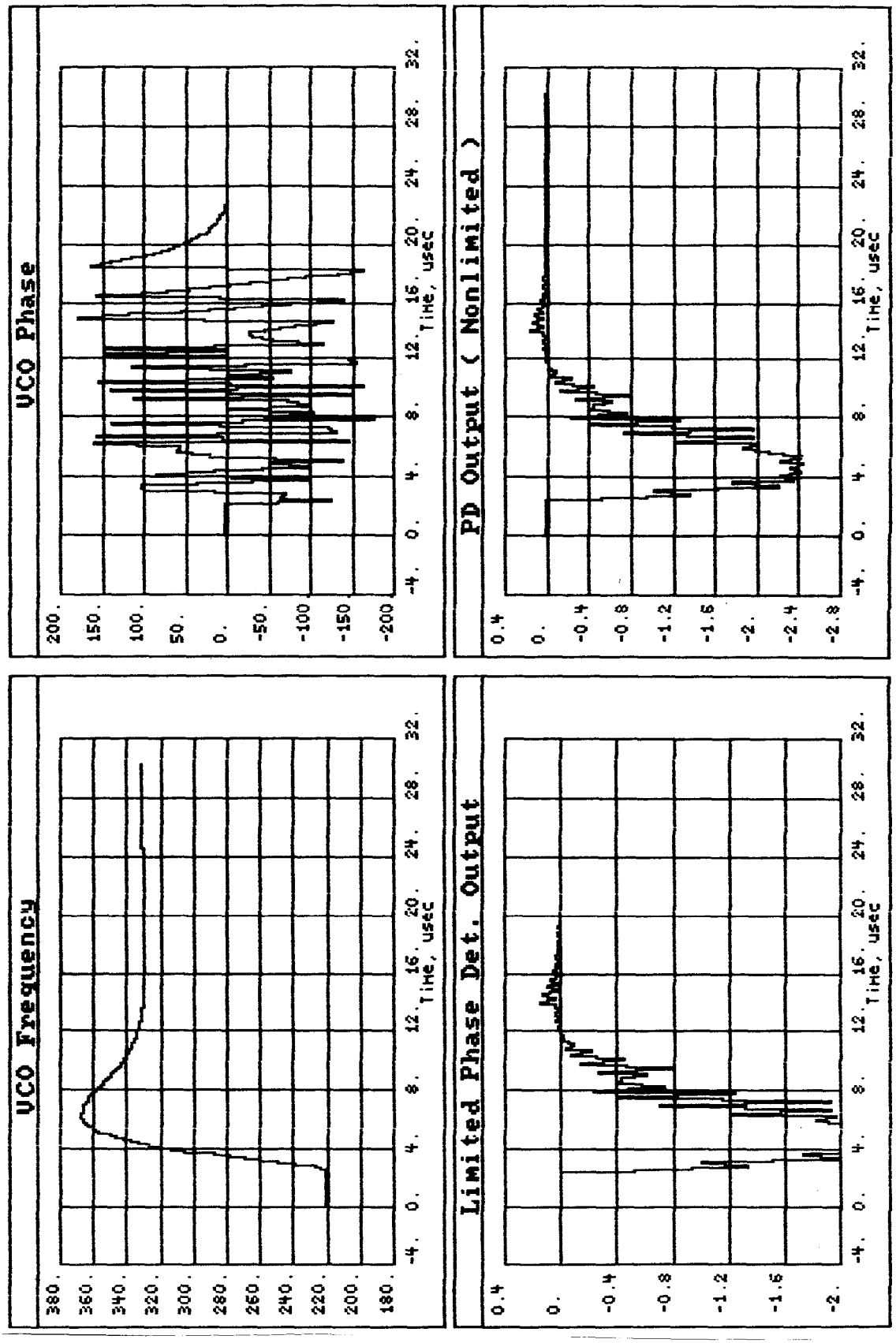
Phase Detector Information:
Description: PD
Phase/Frequency Detector; non-tri-state
Max. output voltage= 5.000000
Min. output voltage= 0.000000
Output Node (Ref.) 1
Output Node (VCO.) 2

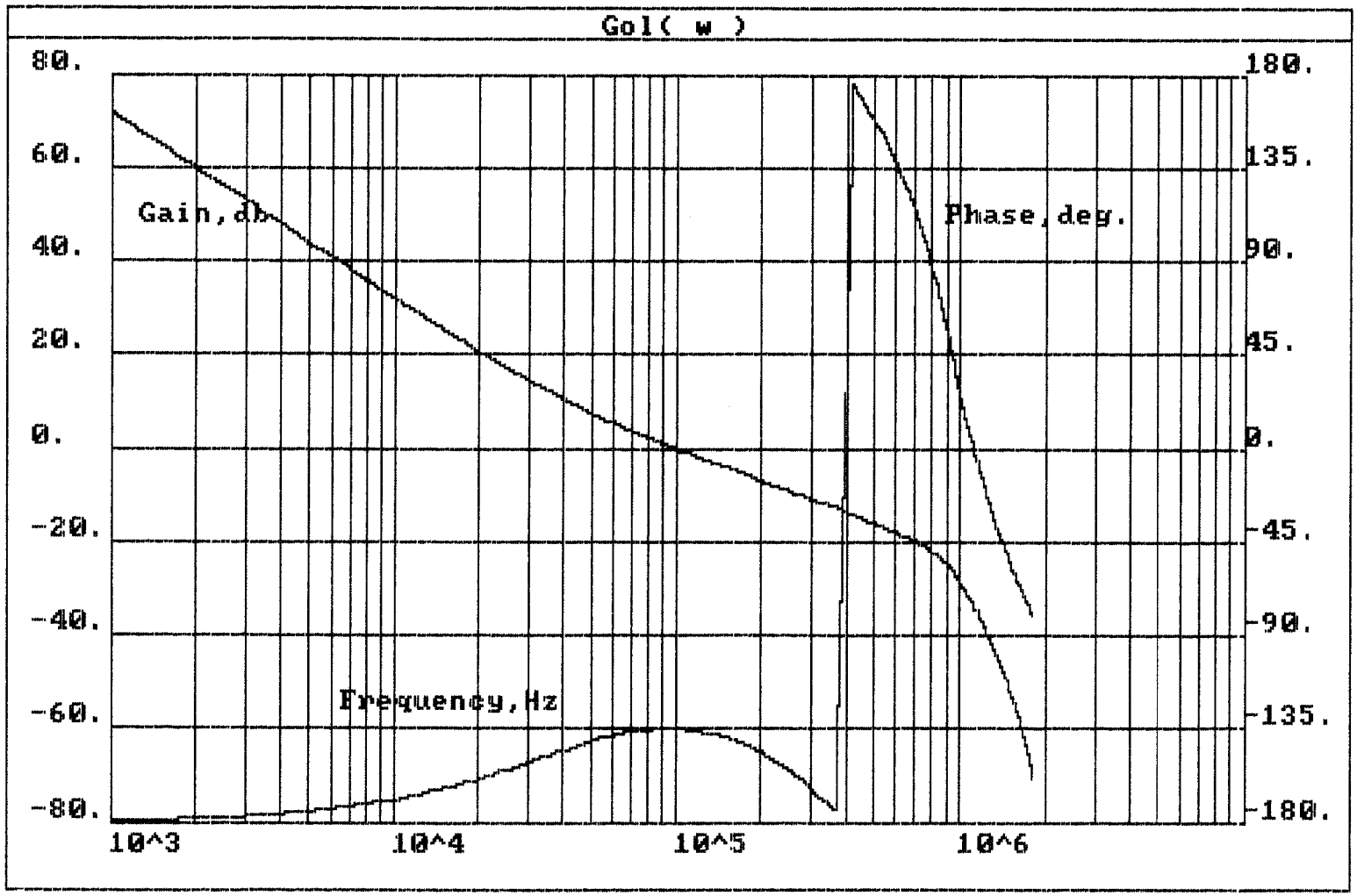
Analysis Details:
Feedback divider ratio 165.000000
Iteration time step, usec 0.019000
PLL Reference Frequency,Hz 2.000000e+006

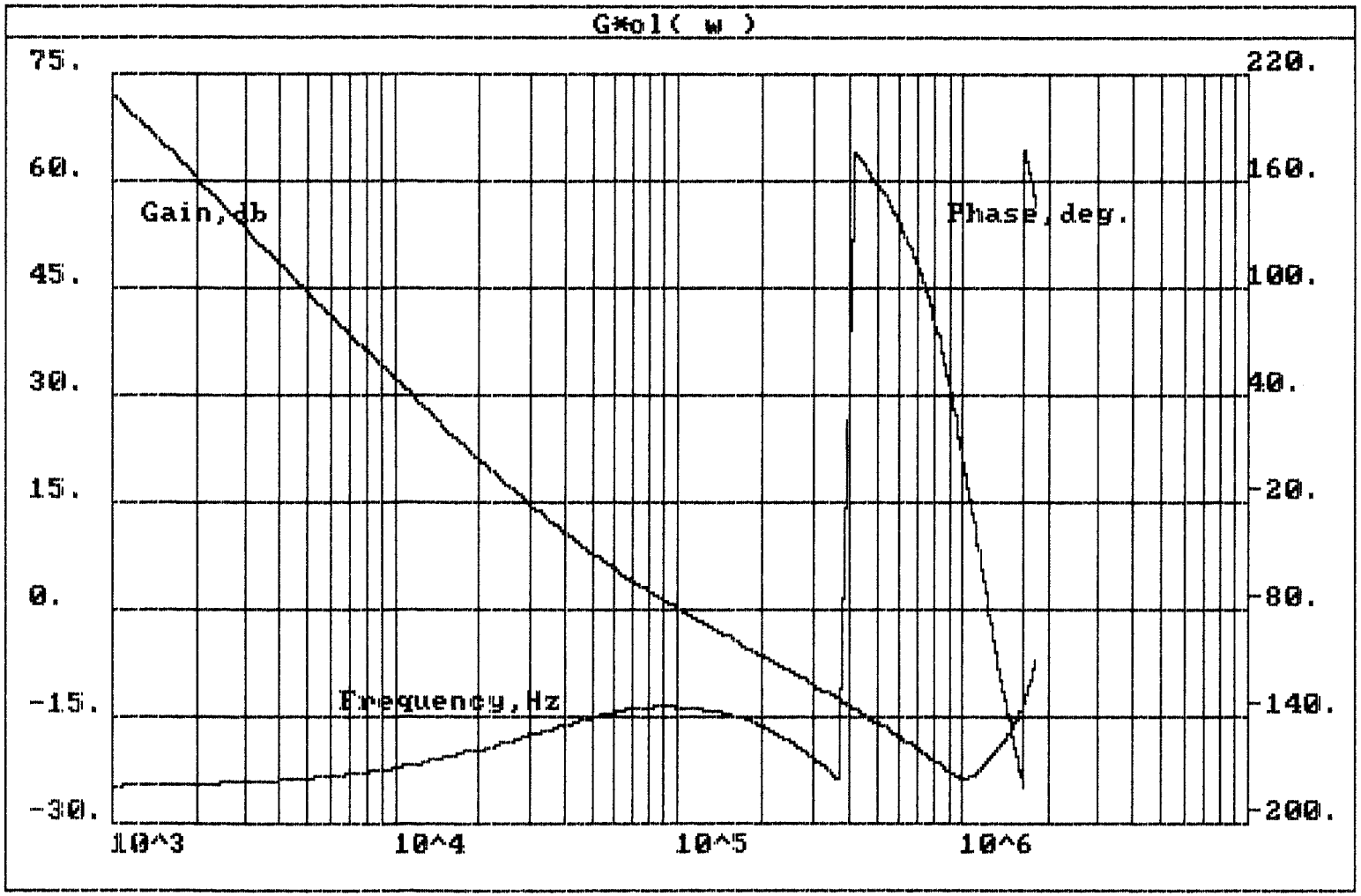
Case V: N = 110 to 165

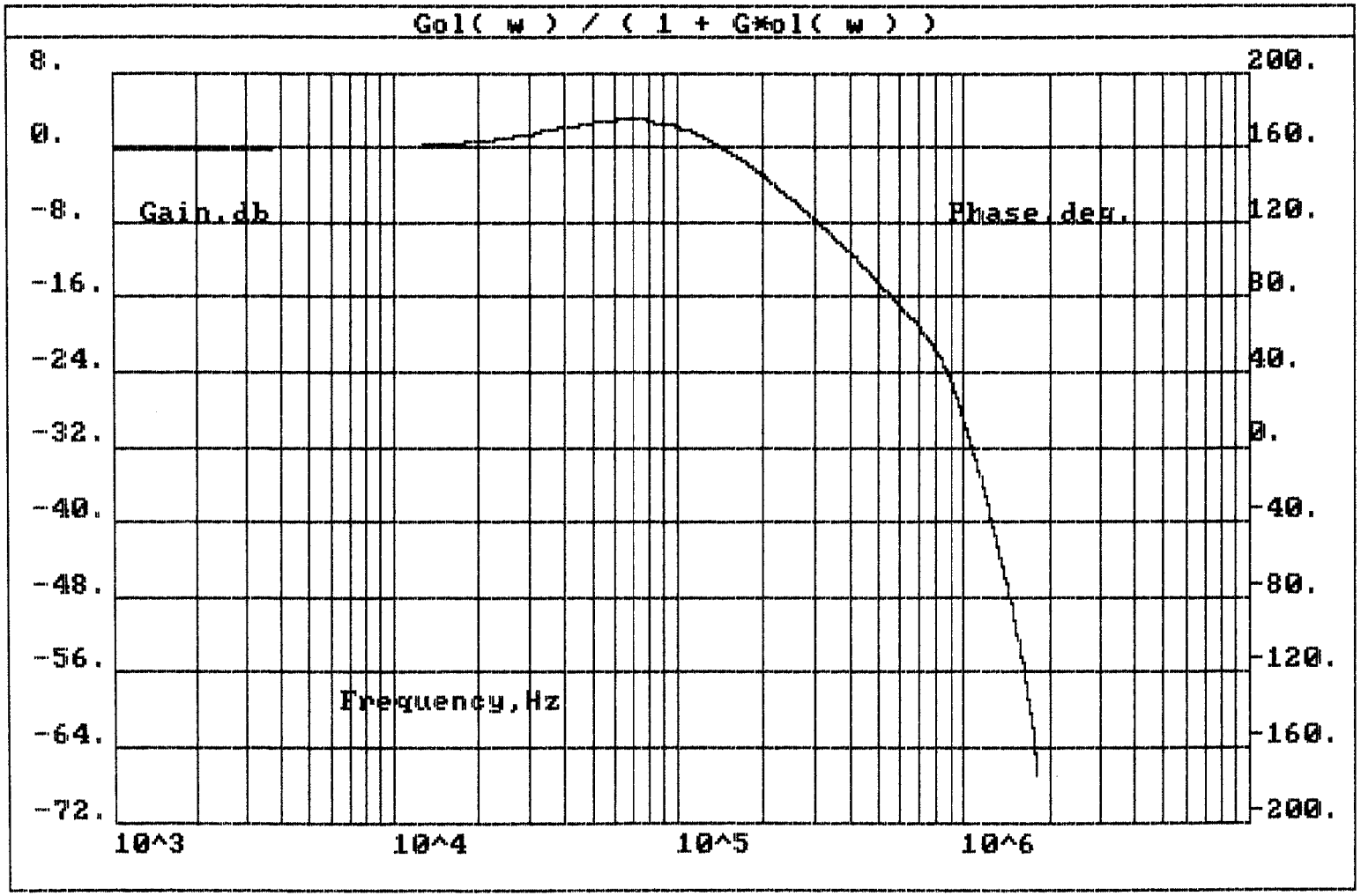
W_n = 70.7 KHz

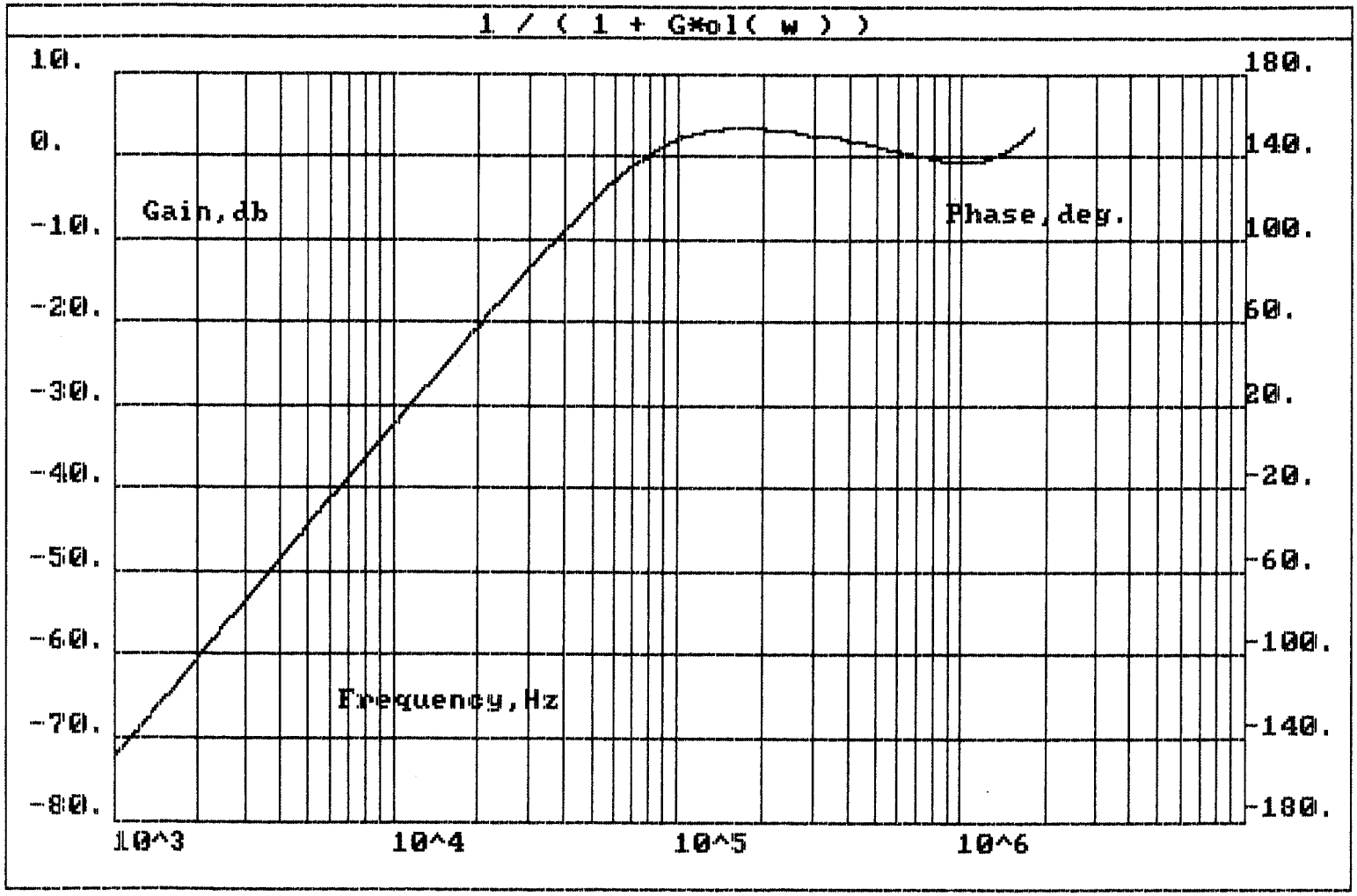
ξ = 0.85




Gol(w)
80.
60.
40.
20.
0.
-20.
-40.
-60.
-80.
180.
135.
90.
45.
0.
-45.
-90.
-135.
-180.
Gain,db
Phase,deg.
Frequency,Hz
10^3
10^4
10^5
10^6


G*ol(w)
75.
60.
45.
30.
15.
0.
-15.
-30.
220.
160.
100.
40.
-20.
-80.
-140.
-200.
Gain,db
Phase,deg.
Frequency,Hz
10^3
10^4
10^5
10^6


Gol(w) / (1 + G*ol(w))
8.
0.
-8.
-16.
-24.
-32.
-40.
-48.
-56.
-64.
-72.
200.
160.
120.
80.
40.
0.
-40.
-80.
-120.
-160.
-200.
Gain,db
Phase,deg.
Frequency,Hz
10^3
10^4
10^5
10^6


1 / (1 + G*ol(w))
10.
0.
-10.
-20.
-30.
-40.
-50.
-60.
-70.
-80.
180.
140.
100.
60.
20.
-20.
-60.
-100.
-140.
-180.
Gain,db
Phase,deg.
Frequency,Hz
10^3
10^4
10^5
10^6