GMSK Modulation

The GMSK waveform can be represented by the instantaneous frequency function

$$f(t) = f_o + \frac{1}{4T}\sum_n a_n\, g(t - nT) \qquad a_n = \pm 1 \text{ data} \qquad [1]$$

$$g(t) = Q\left[k_o BT\left(-\frac{1}{2} - \frac{t}{T}\right)\right] - Q\left[k_o BT\left(\frac{1}{2} - \frac{t}{T}\right)\right] \qquad [2]$$

where the symbol rate $F_{sym} = (270 + 5/6)$ k, and $T = F^{-1}_{sym}$. Also,

where $k_o = 7.546$ and $$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^\infty e^{-y^2/2}\, dy \qquad [3]$$

This representation was used in the May design review materials. For GSM, BT = 0.30, and the modulation index h = 0.50 which results in the apparent peak frequency shift of $\Delta F = (4T)^{-1}$ preceding the above summation over n. (Note, $h = 2\,\Delta FT$).

Since a type-2 PLL cannot track phase functions with parabolic and higher-order time dependencies without error, it is worthwhile computing the maximum rate of frequency change that can be seen by the PLL. It suffices to consider a single "frequency pulse" and compute

$$\begin{aligned} d(t) &= \frac{d}{dt}\left[\frac{1}{4T}g(t)\right] \\ &= \frac{1}{4T}\left[\frac{k_o B}{\sqrt{2\pi}} e^{-\frac{1}{2}\left[k_o BT\left(-\frac{1}{2}-\frac{t}{T}\right)\right]^2} - \frac{k_o B}{\sqrt{2\pi}} e^{-\frac{1}{2}\left[k_o BT\left(\frac{1}{2}-\frac{t}{T}\right)\right]^2}\right] \\ &= \frac{k_o B}{4T\sqrt{2\pi}}\left[\chi\left(-\frac{1}{2}-\frac{t}{T}\right) - \chi\left(\frac{1}{2}-\frac{t}{T}\right)\right] \end{aligned} \qquad [4]$$

where for convenience

$$\chi(u) = e^{-\frac{1}{2}(k_o BTu)^2} \qquad [5]$$

In order to maximize d(t), we need to take the derivative and compute the time at which its value is equal to zero. In doing so, this leads to the required equality

$$\left(-\frac{1}{2}-\frac{t}{T}\right)\ e^{-\frac{1}{2}\left[k_o BT\left(-\frac{1}{2}-\frac{t}{T}\right)\right]^2} = \left(\frac{1}{2}-\frac{t}{T}\right)\ e^{-\frac{1}{2}\left[k_o BT\left(\frac{1}{2}-\frac{t}{T}\right)\right]^2} \qquad [6]$$

which can be easily reduced to simply

$$\frac{\frac{t}{T}+\frac{1}{2}}{\frac{t}{T}-\frac{1}{2}} = e^{(k_o BT)^2\,\frac{t}{T}} \qquad [7]$$

This result cannot be reduced further since it is transcendental in nature. For the case where k_o= 7.546 and BT= 0.30, the solution for the maximum of d(t) occurs for t / T = ± 0.56009. Substituting this back into the original equation, the maximum frequency rate of change is then simply given by d(0.56009T) or

$$\frac{k_o B}{4T\sqrt{2\pi}}\left[\chi\left(-\frac{1}{2}-0.56009\right)-\chi\left(\frac{1}{2}-0.56009\right)\right] \qquad [8]$$

where equates to approximately 2.785 10^{11} Hz / sec^2. At first glance, this appears to be a very large number indeed, but if we think in terms of changing (F_{symbol} / 4) Hz in one-half symbol interval, this equates to 3.67 10^{10} Hz / sec^2 so we have reasonably parity.

If a Type-2 PLL is subjected to a linear frequency range that is changing at a constant rate of Δω radians / sec^2, the steady-state stress imposed on the PLL is given by

$$\theta_{ss} = \frac{\Delta\omega}{\omega_n^2} \qquad [9]$$

Simple substitution for different loop natural frequencies leads to the results shown here in tabular form.

Table 1 Loop Stress for Type-2 PLL Subjected to Linear Frequency Sweep

Loop Natural Frequency, Hz	Loop Stress, deg.
100 k	254
120 k	176
140 k	130

Obviously, the translation loop is not subjected to this frequency sweep rate except on symbol transitions, but this does provide some insight into the degree to which the PLL is being pushed when fairly small loop natural frequencies are employed.

A Closer Look at the Type-2 Case

It is worthwhile looking at the behavior of an ideal Type-2 PLL when it is asked to pass the GMSK modulation. We will focus on the PLL's response to a single "frequency pulse" as before. For the Type-2 case,

$$G_{OL}(s) = \left(\frac{\omega_n^2}{s}\right)\left(1 + \frac{2\ \zeta s}{\omega_n}\right)$$

$$\frac{\theta_o(s)}{\theta_{in}(s)} = \frac{G_{OL}(s)}{1+G_{OL}(s)} = \frac{\omega_n^2\left(1+\frac{2\zeta s}{\omega_n}\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad [10]$$

$$\frac{\theta_e(s)}{\theta_{in}(s)} = \frac{1}{1+G_{OL}(s)} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Here, θ_e is the phase tracking error as seen at the phase detector of the PLL. Focusing first on θ_e:

$$\left(s^2 + 2\zeta\omega_n s + \omega_n^2\right)\theta_e = s^2\theta_{in}$$

$$s\theta_e + 2\zeta\omega_n\theta_e + \omega_n^2\frac{\theta_e}{s} = s\theta_{in} \qquad [11]$$

We now let $d\theta_{in}/dt = 2\pi f_{in}(t)$ which leads to the following assignment of state variables:

$$u_0 = s\theta_{in} \Rightarrow \frac{d}{dt}\theta_{in}(t)$$

$$u_1 = \frac{\theta_e}{s} \Rightarrow \int \theta_e(t)\ dt \qquad [12]$$

$$u_2 = \theta_e(t)$$

This set of integro-differential equations can be numerically integrated in order to examine the behavior of $\theta_e(t)$ for different PLL loop parameters. A plot of the phase error behavior at the phase detector for a single frequency pulse is shown here in Figure 1 for several closed-loop bandwidth cases.

For the behavior of the output phase with time, we have

$$s^2\theta_o + 2\zeta\omega_n s\theta_o + \omega_n^2\theta_o = \theta_{in}\omega_n^2 + \theta_{in}\frac{2\zeta s}{\omega_n} \qquad [13]$$

which for computational purposes is better expressed as

$$\left(1+\frac{2\zeta\omega_n}{s}+\frac{\omega_n^2}{s^2}\right)\theta_o=\theta_{in}\omega_n^2\left(\frac{1}{s^2}+\frac{2\zeta}{\omega_n s}\right) \quad [14]$$

In state-variable form, it is convenient to choose the following:

$$\begin{aligned}
u_0 &= \theta_{in} \\
u_1 &= \int \theta_{in} dt \\
u_2 &= \int u_1 dt \\
\theta_o &= \omega_n^2\left(u_2+\frac{2\zeta}{\omega_n}u_1\right)-2\zeta\omega_n u_3-\omega_n^2 u_4 \\
u_3 &= \int \theta_o dt \\
u_4 &= \int u_3 dt
\end{aligned} \quad [15]$$

This set of equations can be numerically integrated for the same frequency pulse input to show the output phase response of the Type-2 PLL as shown in Figure 2.

Figure 1 Type-2 Transient Phase Error Response to GMSK Frequency Pulse for the Type-2 PLL

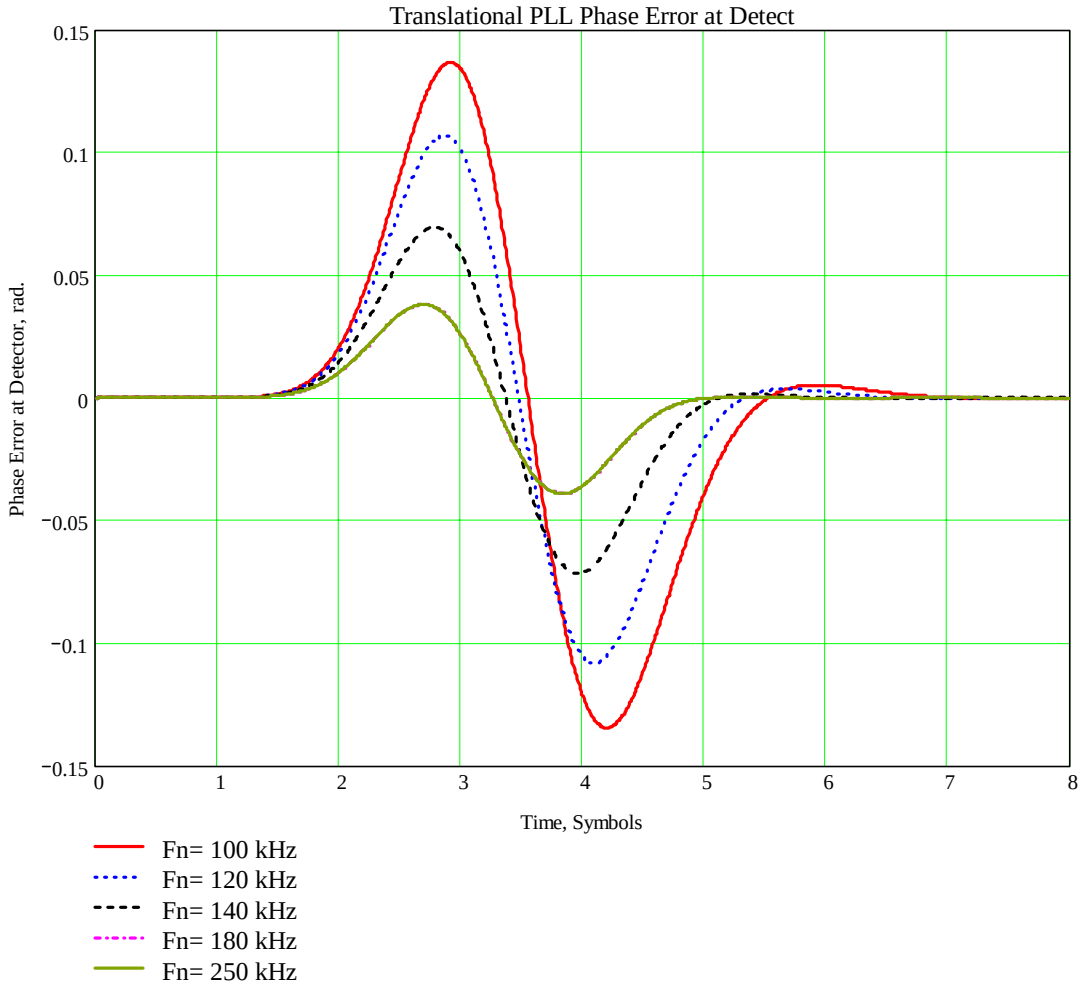
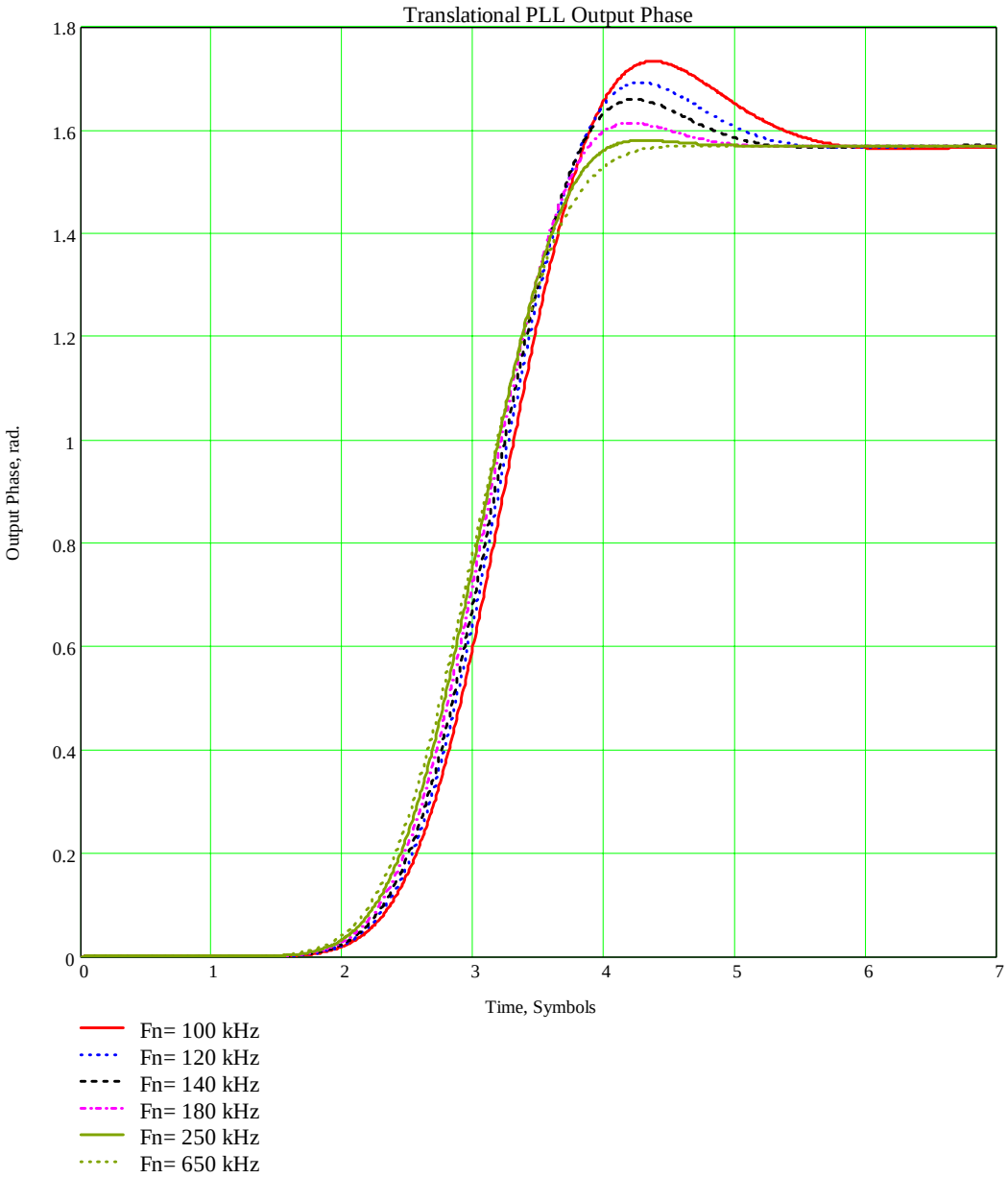


Figure 2 Output Phase Response to the Frequency Pulse for the Type-2 PLL



General Comments

The phase trajectories shown in Figures 1 and 2 reveal loop strain for the lower bandwidth cases. From Figure 1, the worst-case peak phase error is about 0.15 radians, or approximately 8.6 degrees. For a 4 MHz phase-locked loop comparison frequency, this phase error is equivalent to a pulse width change at the phase detector of only about (8.6/360) 250 nsec ≈ 6 nsec which is negligible as far as the reference-related spur levels are concerned.

Type-3 PLL Behavior with GMSK Frequency Pulse Input

The primary motivation for looking at the translational loop right now were based upon earlier comments made pertaining to trading-off PLL bandwidth for performance. At the time, it appeared that the PLL was being over stressed by the modulation, but the results shown in Figures 1 and 2 tend to suggest otherwise. The root issue (as far as phase accuracy is concerned) may well be the length of the (presumably FIR) equalizer or another matter entirely that is interfering with obtaining the desired results, but determination of the underlying problem will require additional time.

Before leaving this first glance at the translational PLL for GMSK, it is worthwhile to consider whether a Type-3 architecture can provide some benefit over the classical Type-2. Admittedly, the type-3 route poses some new issues over the Type-2 approach, so the examination here will be strictly mathematical rather than circuit-oriented. It is hoped that the Type-3 architecture will produce an additional degree of freedom whereby the PLL's natural loop frequency can be traded-off for a smaller value without sacrificing phase accuracy.

There is not much immediately available literature on Type-3 PLLs, so some review of the basic tenants is appropriate. The general open-loop gain transfer function for a Type-3 PLL is given by

$$G_{OL}(s) = K\frac{(1+s\tau_2)(1+s\tau_3)}{s(\tau_1 s)^2} \qquad [16]$$

Generally, the time constants τ_2 and τ_3 are chosen to be equal, so this simplifies the open-loop gain function as

$$G_{OL}(s) = \frac{K}{s}\left(\frac{1+s\tau_2}{s\tau_1}\right)^2 \qquad [17]$$

The phase of the open-loop gain function is clearly given by

$$\angle G_{OL}(s) = -\frac{3\pi}{2} + 2\tan^{-1}(\omega\tau_2) \qquad [18]$$

Obviously, $\angle G_{OL}(s) = -\pi$ for $\omega\tau_2 = 1$ which means that this situations occurs for $\omega = \tau_2^{-1}$. The gain at this critical frequency is given by

$$G_M = 2K\tau_2\left(\frac{\tau_2}{\tau_1}\right)^2 \qquad [19]$$

A positive gain margin results if and only if $G_M > 1$.

For frequencies $\omega > \tau_2^{-1}$, the control loop looks very similar to a classical Type-2 loop. (This same equivalence may translate into a negligible advantage for the GSM translational loop application.)

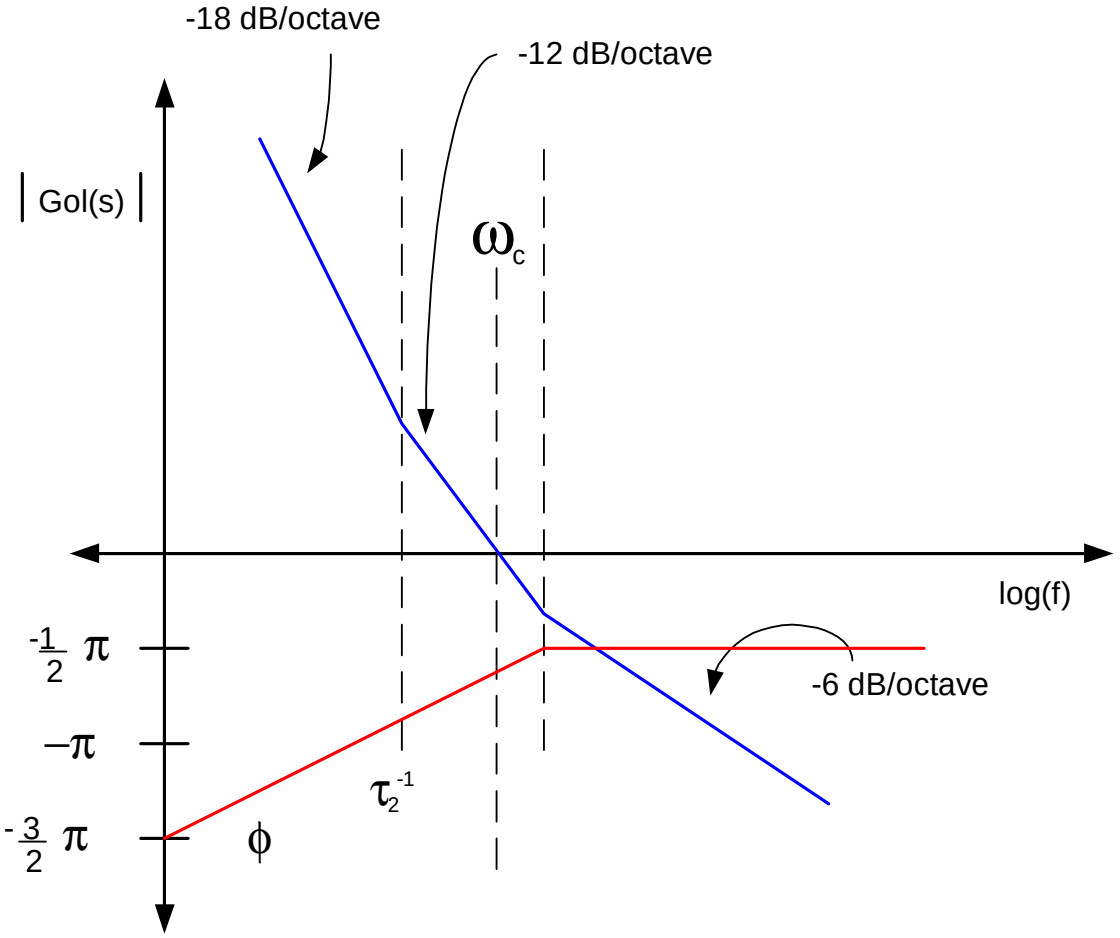
To first-order, for $\omega > \tau_2^{-1}$,

$$\left|G_{OL}(s)\right| \approx \left|\frac{K}{s}\left(\frac{\tau_2}{\tau_1}\right)^2\right| \qquad [20]$$

so the unity-gain cross-over frequency (ω_c) is approximately given by

$$\omega_c \approx K\left(\frac{\tau_2}{\tau_1}\right)^2 \qquad [21]$$

Figure 3 Open-Loop Gain Characteristic for Type-3 PLL



From earlier, the gain margin was given by [19] and therefore,

$$\omega_c \approx \frac{G_M}{2\tau_2} \qquad [22]$$

The exact result for ω_c can be found by solving

$$\left| \frac{K}{j\omega} \left(\frac{1+ j\omega\tau_2}{j\omega\tau_1} \right)^2 \right| = 1$$

or

$$\omega^3 - K\left(\frac{\tau_2}{\tau_1}\right)^2 \omega^2 - \frac{K}{\tau_1^2} \equiv 0 \qquad [23]$$

Given an initial estimate for the true solution (denoted by ω_x), a root-polishing recursion can be easily found as

$$\omega_x' = \omega_x + d\omega$$

where

$$d\omega = \frac{-\omega_x^3 + K\left(\frac{\tau_2}{\tau_1}\right)^2 \omega_x^2 + \frac{K}{\tau_1^2}}{3\omega_x^2 - K\left(\frac{\tau_2}{\tau_1}\right)^2 2\omega_x} \qquad [24]$$

Comment: Use of K and τ_1 is redundant. If we simply assign $K_x = K/\tau_1^2$, then the equation to be solved simplifies to

$$\omega^3 - K_x(\tau_2\omega)^2 - K_x \equiv 0$$

Near Equivalence for the Type-3 PLL with the Classical Type-2 PLL

For a given value of ω_c, a Type-3 PLL behaves very similarly to a Type-2 PLL having a damping factor of ζ given by

$$\zeta \approx \frac{1}{2}\left(\frac{1-\alpha^2}{2\alpha}\right)^{\frac{1}{2}} \quad where \quad \alpha = \left(\omega_c \tau_2\right)^{-1} \qquad [25]$$

Assuming that we have a pre-specified value of ω_c, we need to know how to select τ_2. From [25], we obtain that

$$\alpha = \frac{-8\zeta^2 \pm \sqrt{64\zeta^4 + 4}}{2} \qquad [26]$$

In order to have $\alpha > 0$, it is simple to show that the only acceptable solution from [26] is

$$\tau_2^{-1} = \omega_c \left[\sqrt{16\zeta^4 + 1} - 4\zeta^2\right] \qquad [27]$$

Frequency Pulse Response of the Type-3 PLL

For the Type-3 PLL, the transfer function between the phase error and the applied input phase function is given by

$$\frac{\theta_e(s)}{\theta_{in}(s)} = \frac{s^3}{s^3 + K_x(\tau_2 s)^2 + 2K_x\tau_2 s + K_x} \quad [28]$$

and similarly for the output phase,

$$\frac{\theta_o(s)}{\theta_{in}(s)} = \frac{K_x(1+s\tau_2)^2}{s^3 + K_x(\tau_2 s)^2 + 2K_x\tau_2 s + K_x} \quad [29]$$

We are interested in comparing θ_o and θ_e with the results obtained earlier for the Type-2 PLL case. For the phase error process, we let

$$\begin{aligned} u_0 &= \frac{d}{dt}\theta_{in} \\ u_1 &= \frac{d}{dt}\theta_e \\ u_2 &= \theta_e = \int u_1 dt \\ u_3 &= \int u_2 dt = \int \theta_e \\ u_4 &= \int u_3 dt = \iint \theta_e dt \end{aligned} \quad [30]$$

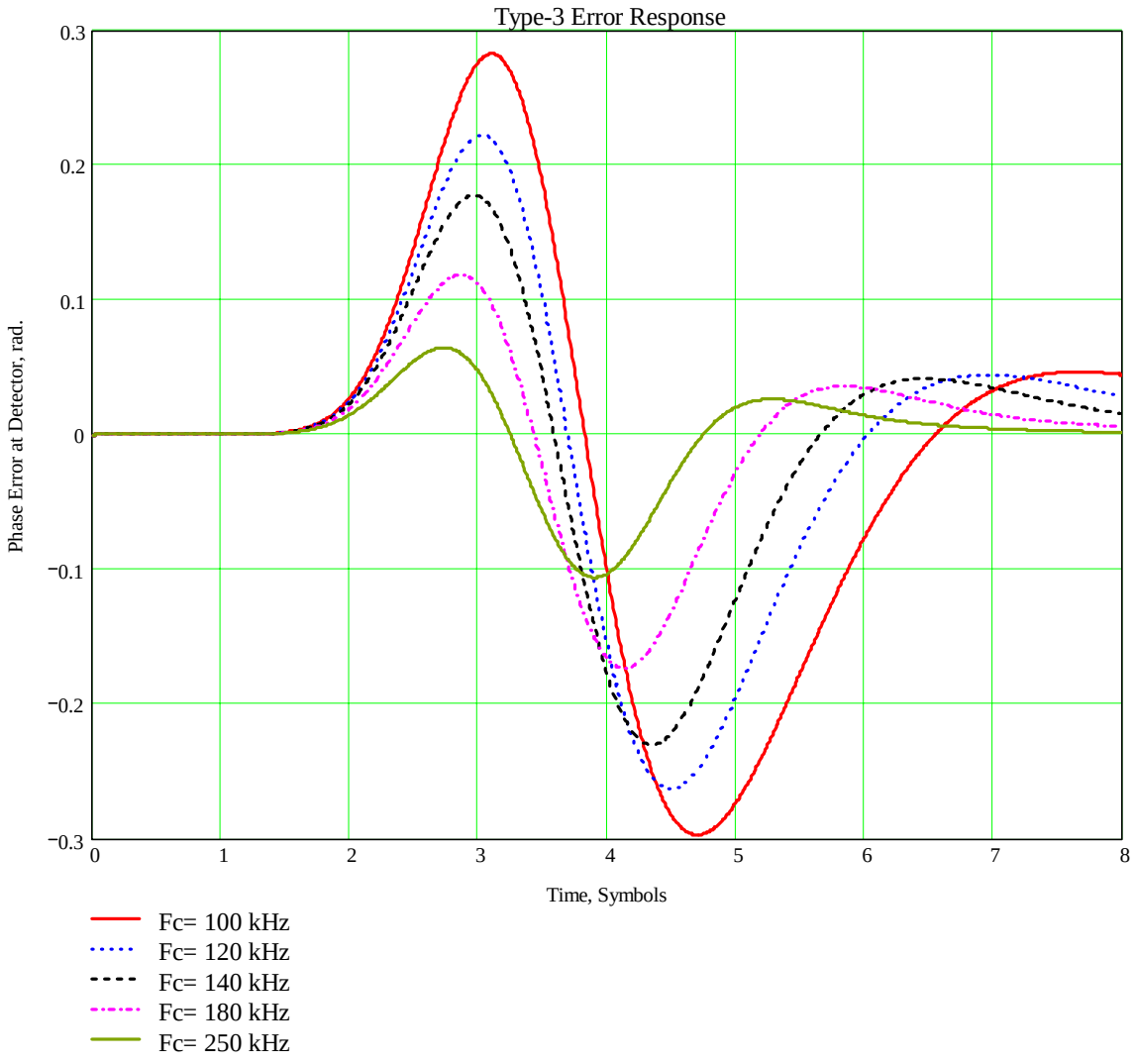
which leads to the state-equations given by

$$\begin{aligned} u_0 &= 2\pi f_{in}(t) \\ u_1 &= u_0 - K_x\left[\tau_2^2 u_2 + 2\tau_2 u_3 + u_4\right] \\ u_2 &= \int u_1 dt \\ u_3 &= \int u_2 dt \\ u_4 &= \int u_3 dt \end{aligned} \quad [31]$$

The phase error response at the phase detector for the Type-3 case is shown in Figure 4. The time duration of the error is particularly concerning because it stretches over several symbol intervals thereby causing intersymbol interference which could only be corrected using a fairly long equalizer.

In making comparisons between the Type-2 and Type-3 systems, we should not equivalence ω_c with ω_n because the ω_c corresponds to approximately the unity open-loop gain for the Type-3 system which is quite different.

Figure 4 Phase Error Response of the Type-3 PLL to a Single Frequency Pulse



For the Type-2 system, the unity open-loop gain frequency occurs at

$$\omega_{2unity} = \omega_n \sqrt{2\zeta^2 + \sqrt{4\zeta^4 + 1}} \qquad [32]$$

which equals approximately 1.554 ω_n for a Type-2 system having ζ= 0.707.

For the output phase of the loop when subjected to the frequency pulse, we have the transform relationship

$$\theta_o\left[s + K_x\tau_2^2 + \frac{2K_x\tau_2}{s} + \frac{K_x}{s^2}\right] = K_x\theta_{in}\left[\frac{1}{s^2} + \frac{2\tau_2}{s} + \tau_2^2\right] \quad [33]$$

If we now make the following state-variable assignments of

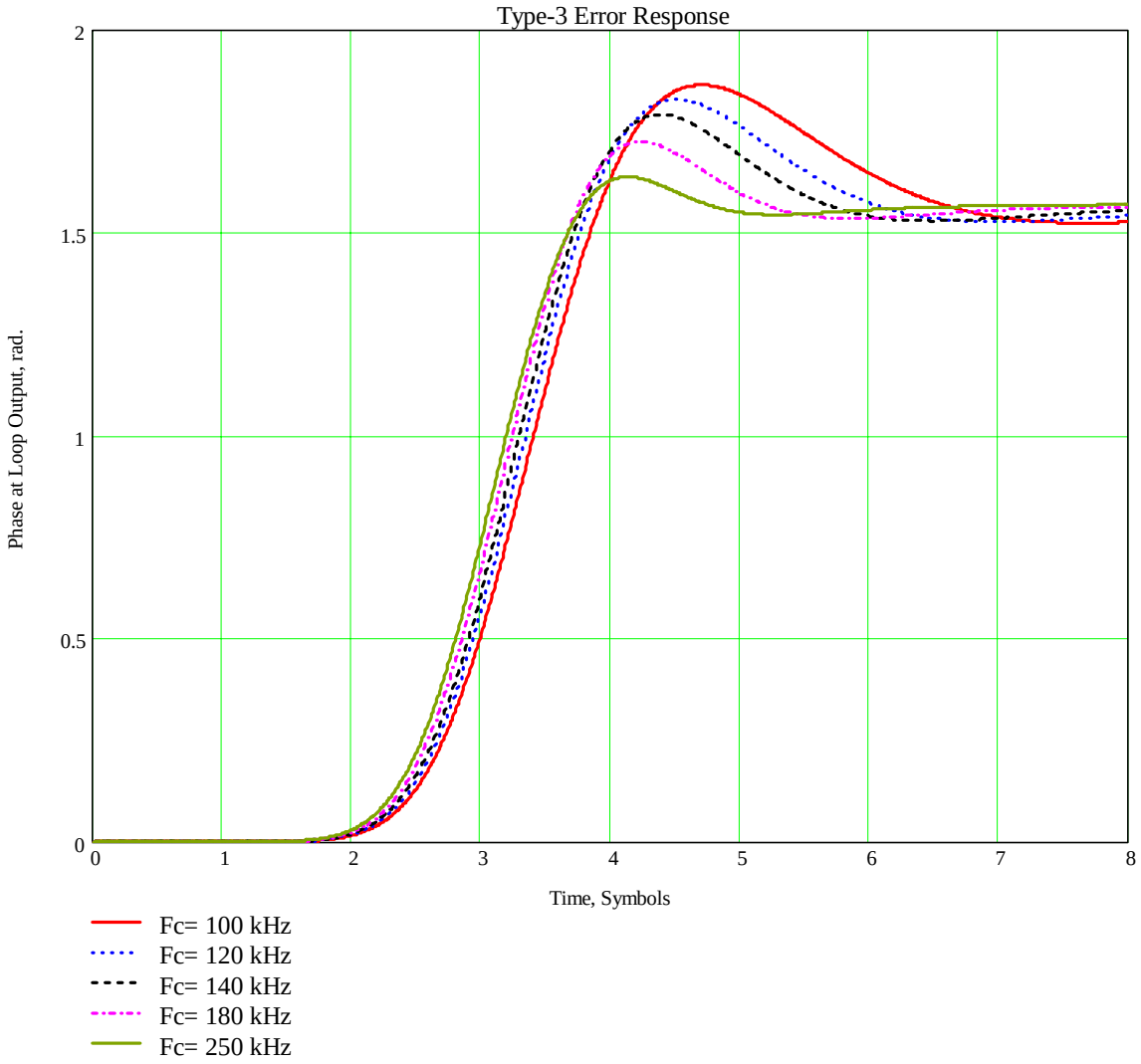
$$\begin{aligned} u_0 &= \theta_{in}(t) \\ u_1 &= \int u_0 dt = \int \theta_{in} dt \\ u_2 &= \int u_1 dt \\ u_3 &= \theta_o \\ u_4 &= \int u_3 dt \\ u_5 &= \int u_4 dt \end{aligned} \quad [34]$$

then the state-variable equations that must be integrated are

$$\begin{aligned} u_0 &= \theta_{in}(t) \\ u_1 &= \int u_0 dt \\ u_2 &= \int u_1 dt \\ u_3 &= \theta_o(t) \\ u_4 &= \int u_3 dt \\ u_5 &= \int u_4 dt \\ \frac{d\theta_o}{dt} &= K_x\left[u_2 + 2\tau_2 u_1 + \tau_2^2 u_0\right] - K_x\left[\tau_2^2 u_3 + 2\tau_2 u_4 + u_5\right] \end{aligned} \quad [35]$$

The output phase response for the frequency pulse input to the Type-3 PLL is shown in Figure 5 for the same PLL bandwidth cases as used in Figure 4. The step responses are disappointingly poor, particularly the very long tail response that would all but invalidate an FIR-type equalizer like that which can be used with the Type-2 PLL.

Figure 5 Output Phase Response to an Input Frequency Pulse for the Type-3 PLL Case



Summary

As far as the ideal Type-2 and Type-3 cases are concerned, the Type-2 (presently anticipated for the design) is far superior to the Type-3 PLL. There is no benefit in considering the Type-3 PLL case any further in regard to a translational role with GSM.

There is no doubt but that an 'optimal' choice of damping factor and natural frequency for the Type-2 PLL can be identified, but no attempt has been made here to arrive at that recommended solution.

The stress imposed at the Type-2 phase detector when modulation is applied does not appear to be excessive so long as a reasonable loop bandwidth is used.

The primary purpose of this short investigation was to explore whether a Type-3 architecture could ease bandwidth choices for the translational PLL; clearly it cannot.