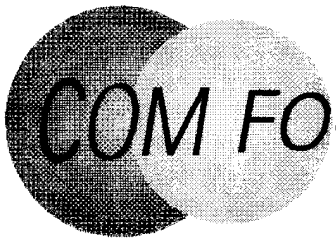

Canadair Bit Synchronizer
Theory of Operation

28 January 1991

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by

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December, 1990

1.0 Introduction

The document which follows is intended to provide detailed information about the Canadair bit synchronizer design approach, the theory behind the design, and where possible, information relevant to design modifications which would make the same generic design suitable for other as yet undefined systems. Although the Canadair system utilizes bi-phase (Manchester) modulation, the bit synchronizer is designed as an NRZ bit synchronizer per Loral direction. The Manchester signal is then viewed as an NRZ data stream at a bit rate twice that of the true Manchester symbol rate. Aside from a later section which addresses the incurred system mismatches which result when using an NRZ synchronizer to synchronize Manchester signals, this document will discuss the subject in terms of NRZ symbols rather than Manchester symbols.

Actual performance of the synchronizer in the Canadair system is further complicated compared to the theory presented here because the baseband data stream is impressed upon a subcarrier using frequency modulation, then combined with a wideband baseband video signal, and the result used to frequency modulate an RF carrier signal. Any nonlinearities, be they due to modulators or demodulators, or insufficient RF bandwidths resulting in degradation of the RF waveform, will cause video energy to be folded into the baseband spectrum region occupied by the data-bearing FM subcarrier thereby deteriorating the effective signal-to-noise (SNR) ratio of the data channel. These added dimensions of the overall Canadair system will not be considered here. Rather, the bit synchronizer will be discussed strictly in the context of a linear, additive white Gaussian noise (AWGN) baseband channel.

1.1 Data Synchronization: An Overview

The bit synchronizer is responsible for i) extracting high quality data bit estimates and ii) data clock estimates from the incoming analog signal which is generally buried in noise. Since both of these functions are extremely important in order for the overall system to perform well, design of the bit synchronizer portion of the system carries substantial importance.

Bit synchronizer design must be viewed as a marriage between

a good understanding of communication theory and hardware design if near optimal performance is to be obtained. Many different methods are available for performing the bit synchronization function. Reliable determination of whether synchronization has in fact been obtained is an equally difficult problem, particularly if the synchronization process must be performed quickly. It is straight forward to show that the design of the synchronization (or lock) detector is intimately tied to the false-lock indication probability which the system can accomodate. Due to the large amount of material available on the subject of bit synchronization, we will be brief and only address several of the many approaches which are available and which are suitable for the range of data rates which are of interest (10 kbps to 2 Mbps).

A nice introduction to optimal bit synchronization can be found in [23-28]. Gardner [2] divides the subject into estimation theoretic (e.g. maximum likelihood), early-late gate, transition tracking, and other categories. The early-late gate approach is primarily intended for use with square pulses where the SNR is very high. We will not consider it further since it is also not suitable where rapid synchronization is required. Holmes [24] itemizes a number of suboptimal bit synchronizers which are based upon either delay-and-multiply or upon the use of a nonlinearity to obtain a clock component.

Estimation Theoretic

Methods grouped into this category are generally capable of near optimal performance and are primarily based upon maximum-likelihood (ML) or maximum a posteriori (MAP) criteria. The MAP-based synchronizer (no intersymbol interference, ISI) is considered in great detail in [25] and an actual detailed implementation is discussed in [36]. A fairly broad range of theoretic-based synchronizers are derived in [29-35].

The MAP-based synchronizer discussed in [36] is shown in Figure 1. It is quite straight forward to show [25] that the log-likelihood function in this case is given by

$$\Lambda(\tau) = C_1 \sum_n Log\ \cosh\left[\frac{2A}{N_o}\, y(\tau) \right] \qquad (1)$$

where

C_1	a constant
A	peak signal amplitude, volts
N_o	one-sided noise power spectral density, W/Hz
$y(\tau)$	sampled output of matched-filter output
τ	symbol timing estimation error
z(t)	input signal

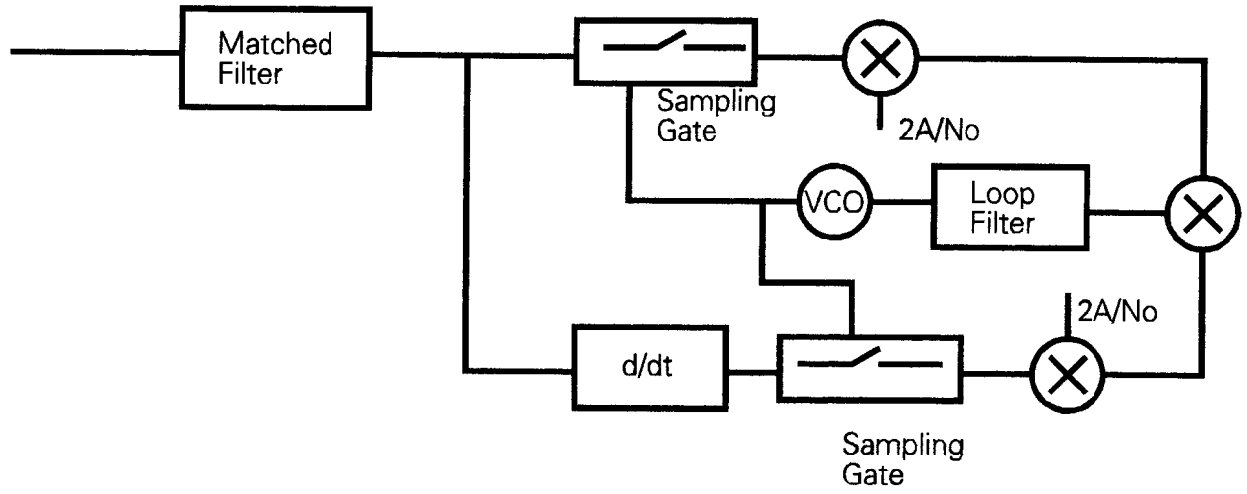


Figure 1. MAP-Based Symbol Synchronizer

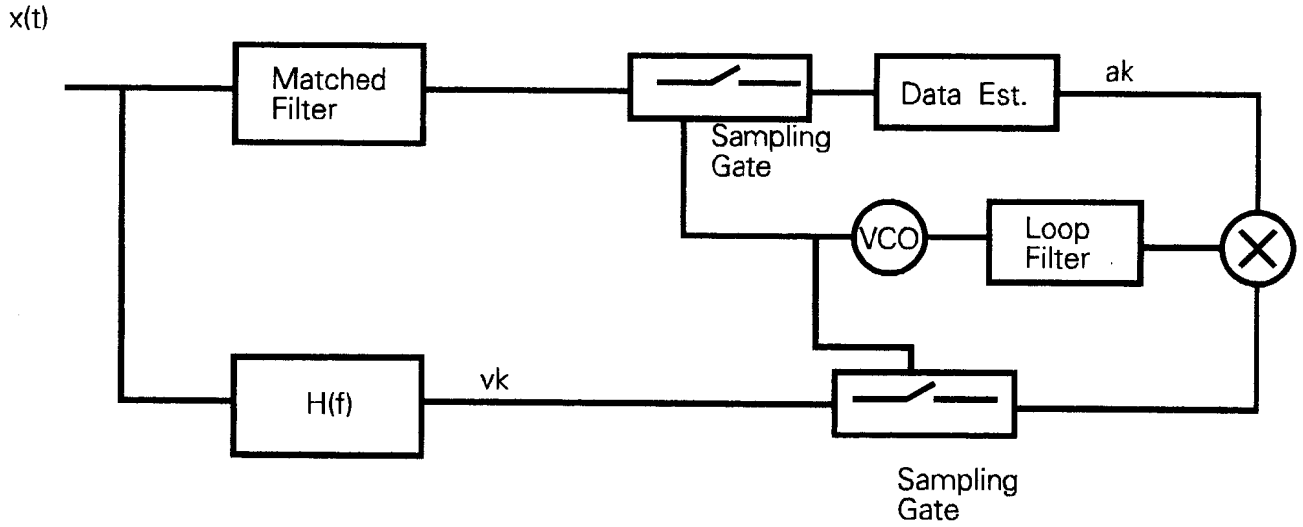


Figure 2. Modified Maximum Likelihood Synchronizer

h(t) matched-filter impulse response

T_s symbol period
T_o observation period

and

$$y(\tau) = \int_0^{T_o} z(t)\ h(t-nT_s-\tau)\ dt \qquad (2)$$

It is simple to maximize the likelihood ratio (since log() is a monotonic function) simply by differentiating (1) to give

$$\frac{\partial \Lambda(\tau)}{\partial \tau} = C_1 \sum_n \left[\frac{2A}{N_o}\ \dot{y}(\tau)\ \tanh\left(\frac{2A}{N_o}\ y(\tau) \right) \right] \qquad (3)$$

The loop configuration shown in Figure 1 clearly drives the quantity given by (3) to zero in steady-state.

The modified maximum likelihood (MML) synchronizer discussed in [33] is shown in Figure 2. H_{MF} represents the matched filter whereas H(f) is a filter designed to extract the data sampling clock. In cases where the matched filter output pulse shape is Nyquist (i.e. no ISI), H(f) simplifies to

$$H(f) = H_{MF}(f) \left[j2\pi f - \sum_m \frac{\dot{r}(mTs)}{r(0)}\ e^{-j2\pi fmT_s} \right] \qquad (4)$$

which is nothing more than the derivative of the matched filter output followed by a transversal filter. In the case where all the derivatives of r(t) are zero at $t = m\ T_s$, this reduces to the ML synchronizer.

The minimum mean-squared error (MMSE) synchronizer is shown in Figure 3. In this case, $H_p(f)$ eliminates the ISI as well as maximizes the SNR at its output. Since the ISI has been eliminated, the data reconstruction is very simple. If the output pulse is again Nyquist, $H_p(f)$ reduces to the matched filter $H_{MF}(f)$. In situations where the bandwidths involved are considerably less than Nyquist, the MMSE method is preferred compared to the MML method [33].

The data-aided ML and non-data-aided ML synchronizers are analyzed in [35] and are shown in Figures 4 and 5. If no ISI is present at the output of the matched filter g(-t), then the ML data reconstructor reduces to a simple comparator in which case it looks

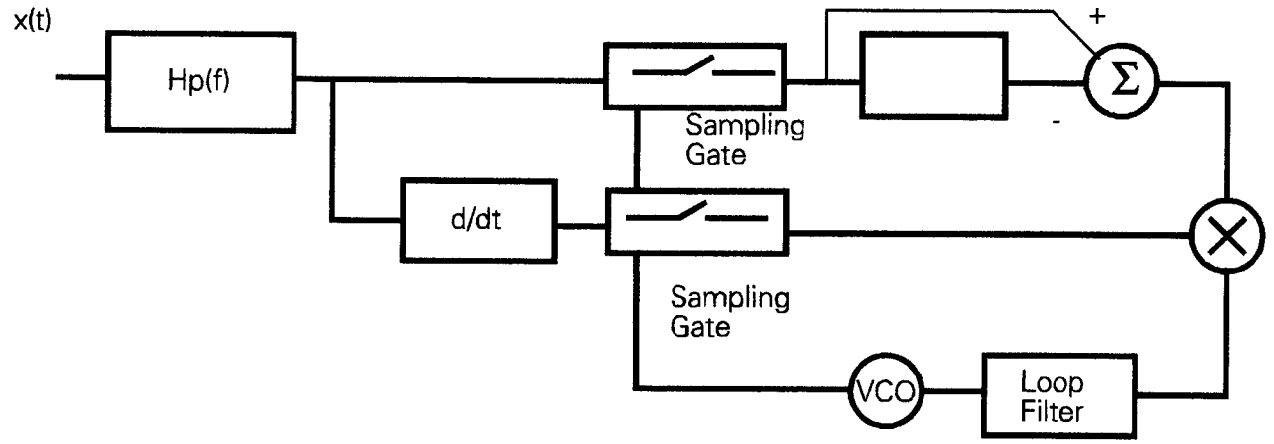


Figure 3. MMSE Synchronizer

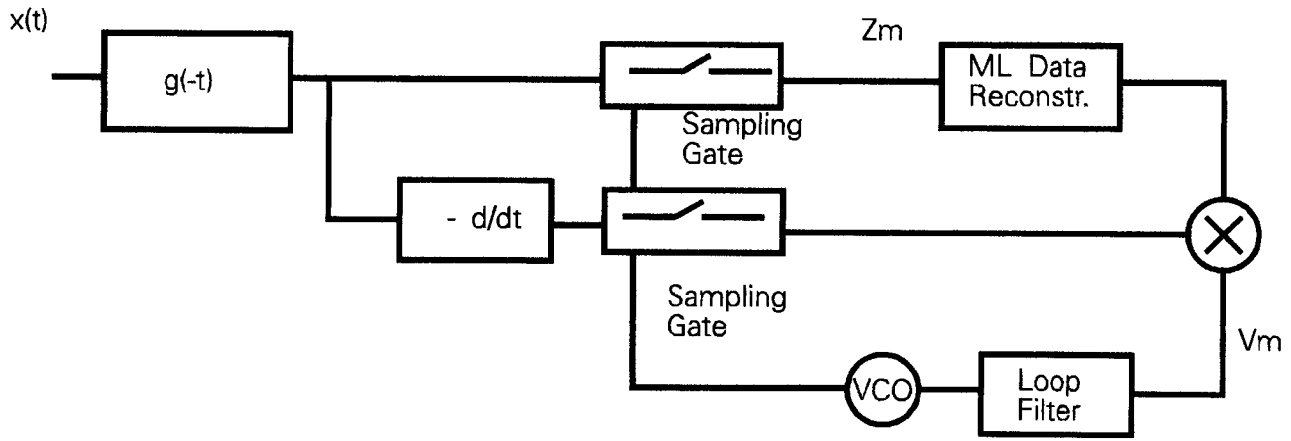


Figure 4. Data-Aided ML Synchronizer

very similar to Figure 3. If ISI is present, the optimal data reconstructor for the AWGN channel is a Viterbi receiver.

These previous four synchronizer types are compared in [34] for the case of raised-cosine symbols. Unlike in the sited references, [34] considered using each synchronizer to perform the timing recovery (only) and the data estimates were made using a matched filter followed by a maximum-likelihood sequence estimator [22]. As far as data estimation goes, this is optimal.

For the small excess bandwidth situation which is generally applicable in our situation, the smallest mean-square synchronization error for low SNR occurs for the DA-ML synchronizer [34]. Although this may be true, further examination of other plots in [34] shows that much larger synchronization loop bandwidths may be used for the MML and MMSE synchronizers in contrast hence making these approaches more suitable where fast acquisition is a necessity.

The methods addressed here are clearly numerically intensive, particularly at high data rates. As a result, they were not considered further in the context of the present design.

Transition Tracking

Transition tracking symbol synchronization is discussed in nearly every basic text convering bit synchronization including [21,23,24,26,28,29] to name but a few. A particularly good reference on the subject is [37]. A block diagram for a transition tracking (TT) symchronizer is shown in Figure 6. Note that the matched filter which was common to all of the previous synchronizers is missing. It is in fact present in the form of the in-phase and mid-phase integrators in the case of square NRZ data symbols.

Of the synchronizers considered thus far, the transition tracking synchronizer is the best suited for the Canadair system because it is very robust [37] and the most simple to implement. The approach may be used at virtually any data rate as well, making it an excellent choice for a generic bit synchronizer topology.

2.0 Design Goals

On August 7, 1990, a kick-off meeting was held to identify the design goals for the synchronizer. Tenative design goals were identified as shown in Table I.

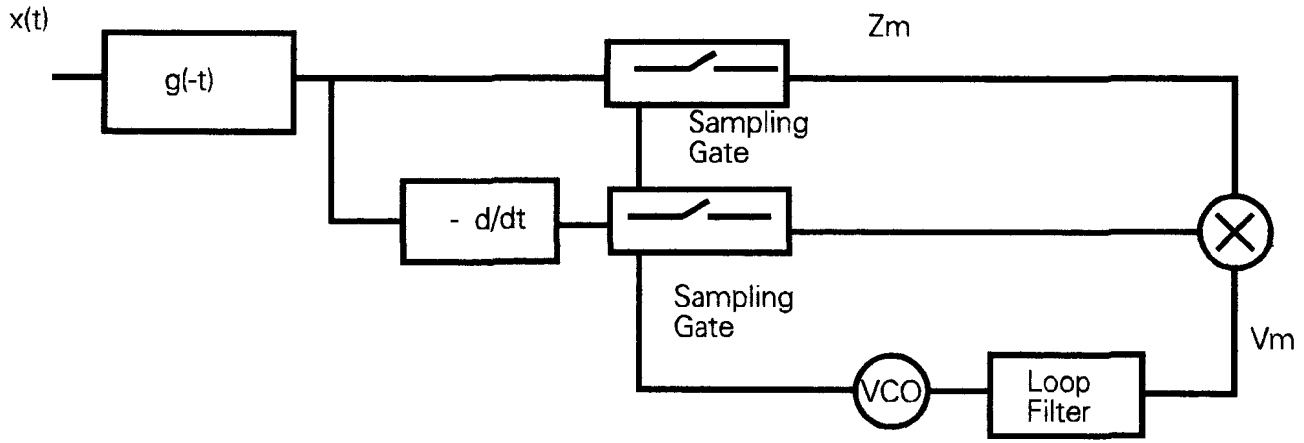


Figure 5. Nondata-Aided ML Synchronizer

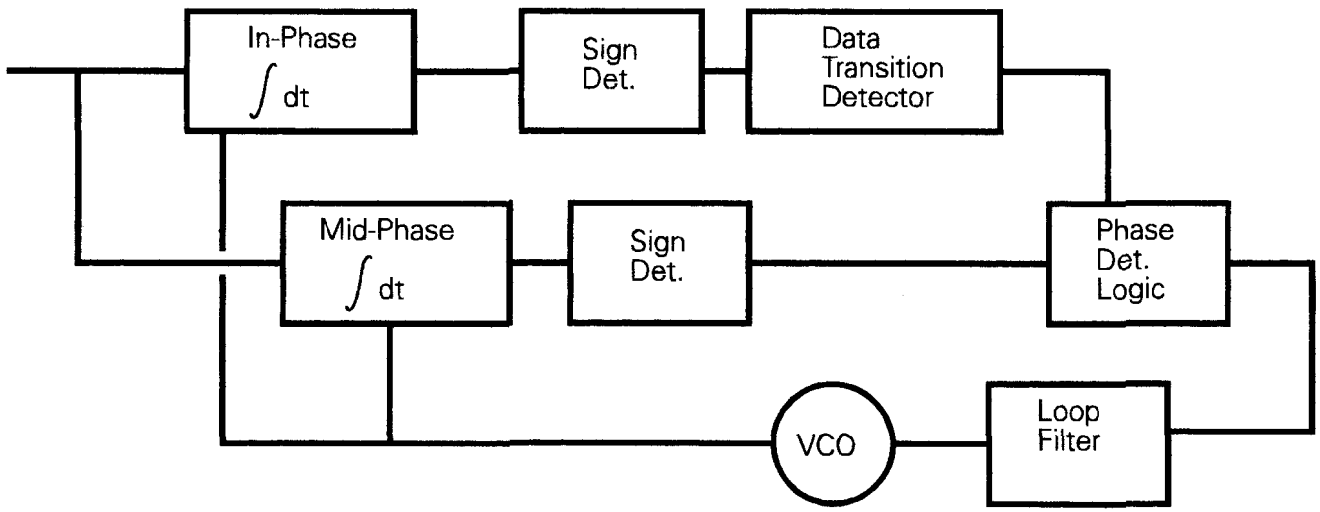


Figure 6. TT Synchronizer

Table I. Canadair Bit Synch: Initial Design Goals

Power Supplies	±15, 5 volts
Temperature Range	-55 to +85 C
NRZ Data Rate	40 kbps (capable of 1 kbps to 2 Mbps with component value changes)
Waveforms	Bi-phase-L, NRZ-L
Lock Time	< 100 symbols at TBD E_b/N_o
Run Length	> 30 symbols
Capture & Track Range	±1 % desired, actual TBD at TBD E_b/N_o
Min Capture SNR	12 dB desired, actual TBD
Bit Error Rate	≤ 3 dB from theory at TBD bit error rate
Clock Jitter	< 0.1% rms at TBD E_b/N_o

The original Canadair synchronizer was to be 40 kbps NRZ. Early into the project however, difficulties were identified involving DC offset out of the subcarrier demodulator and the waveform was changed to Manchester. Ranging precision considerations were also a factor in this decision. The minimum data rate was later raised to 10 kbps from 1 kbps. The design goals which have been adopted for the bit synchronizer are provided in Table II.

Table II. Canadair Bit Synch: Adopted Design Goals

Power Supplies	±15, 5 volts
Temperature Range	-55 to +85 C
NRZ Data Rate	80 kbps (capable of 10 kbps to 2 Mbps with component value changes)
Transition Density	NRZ 30% to 100%
Waveforms	Bi-phase-L, NRZ-L, ± 1 volt peak-peak input
Lock Time	NRZ: < 200 symbols at 12 dB E_b/N_o, ΔR= 0 < 600 symbols at 12 dB E_b/N_o, ΔR=±0.5% Bi-phase: < 150 symbols at 12 dB E_b/N_o, ΔR= 0 < 450 symbols at 12 dB E_b/N_o, ΔR=±0.5%
Run Length	> 30 symbols
Capture & Track Range	±1 % at 6 dB E_b/N_o
Min Capture SNR	12 dB
Bit Error Rate	≤ 3 dB from theory at 10^{-5} BER
Clock Jitter	< 0.5% at 12 dB E_b/N_o

ΔR denotes data rate error, bps

The design is primarily driven by the bottom six items shown in Table II. Lock time as we'll discuss shortly, is strongly driven by the prevaling data rate error and signal to noise ratio. It is fairly meaningless to discuss lock times on the order of Table I (100 symbols) unless the data rate error is very small and the SNR is very high. Since Mike Landry believed that the acquisition process could take as long as 500 to 600 symbols before there would be any system impact, the 100 symbol figure was changed to the values shown in Table II. Definition of what is meant by "lock time" is also at issue here. As alluded to in the introduction, reliable determination of lock is in itself a difficult question. In the Canadair bit synchronizer, indication of synchronization is substantially later than when synchronization is actually obtained. The run length parameter primarily sets a limit on the maximum number of consecutive data-ones or data-zeros which may occur and thereby affects the choice of synchronizer loop bandwidth. (This is not the case with Manchester symbols where we are guaranteed a transition every symbol period.) Extremely long run length

capability and fast acquisition are generally mutually exclusive design requirements. Normally, capture and track range are specified separately; they are also a strong function of SNR. In lieu of firm requirements, the ±1 % requirement was taken as a noise free design goal.

It cannot be understated how much the data rate uncertainty parameter amplified the complexity of the bit synchronizer design. Since VCXOs cannot cover this wide frequency range, and LC oscillators are prone to temperature drift, the bit synchronizer oscillator design case was quite involved. Had the data rate uncertainty been roughly ±0.07 % or less, the size of the present design would have shrunk dramatically (at least 50%). The worst-case locking speed would also be substantially faster as well.

The minimum capture SNR of 12 dB presents no serious design challenges unless very fast locking is desired over the full ±1 % data rate uncertainty range. The data rate anomoly for Canadair should be much smaller than ±1 % which should result in good locking speed nonetheless. Since the design is also required to accomodate NRZ data rate requirements up to 2 Mbps, this also dictated that the VCO phase noise performance be fairly good.

The degradation with respect to theory of 3 dB for the NRZ waveform is also very obtainable. The synchronizer design for Canadair is capable of performing within 1 dB of theory or better for NRZ data provided that the premodulation and matched filter are done properly and if no additional bandlimiting by other system elements is present.

Finally, the recovered clock jitter requirement is difficult enough that careful tracking loop parameters had to be selected. This is discussed at some length in section 3.3.

3.0 Design Methodology for the Canadair Bit Synchronizer

A block diagram for the bit synchronizer is shown in Figure 7. We will discuss each of the major functional areas shown in some detail within the balance of this section, identifying required design goals as they surface.

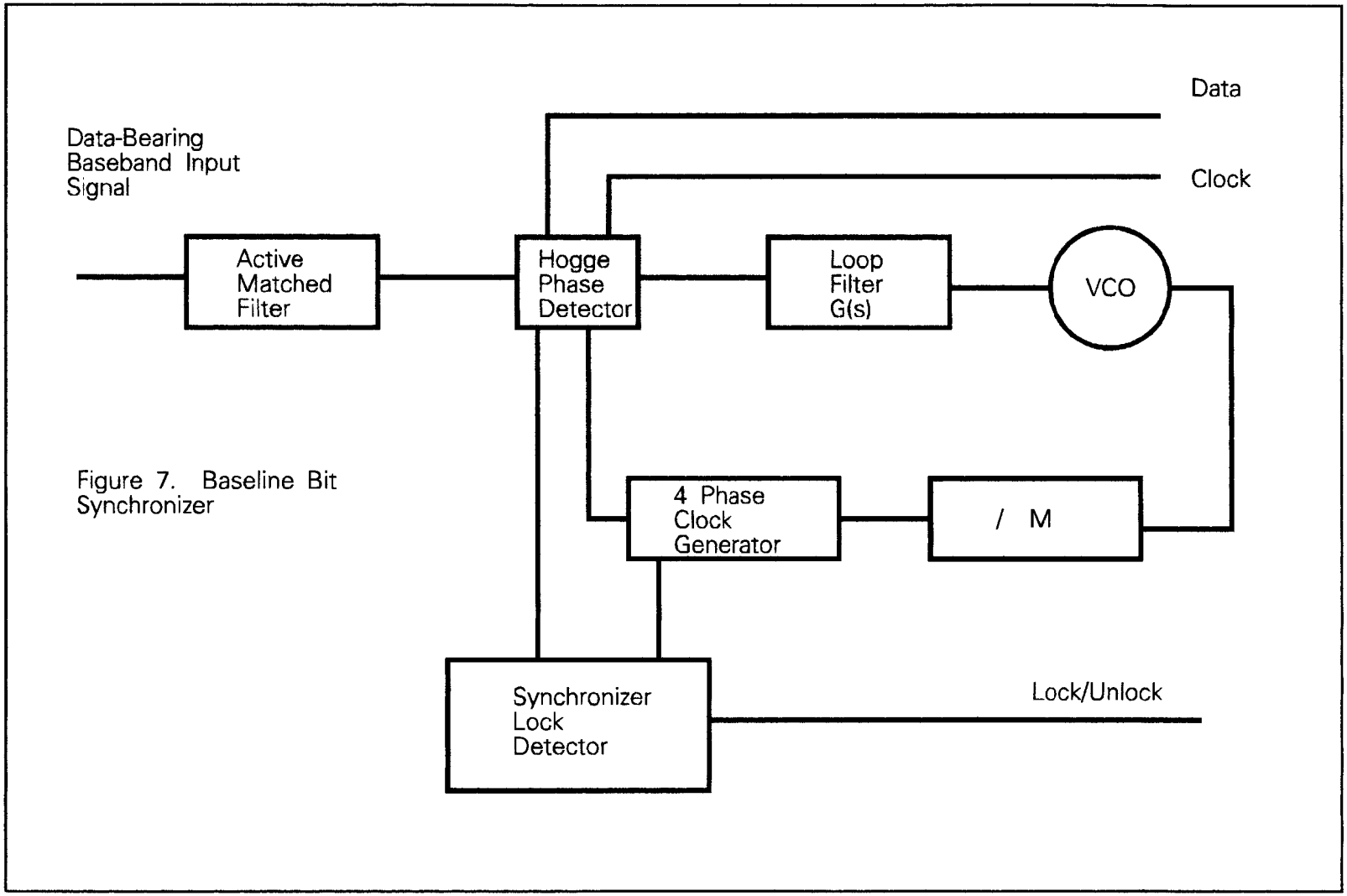


Figure 7. Baseline Bit Synchronizer

3.1 Voltage Controlled Oscillator

The VCO for the Canadair bit synchronizer occupies roughly half the total board area in the final configuration and simply based upon this proportion, is a pivotal design consideration for the synchronizer. As alluded to earlier, the primary parameter driving the complexity of this function is the desire to be able to accomodate data rate anomolies as large as ±1 % while having adequate phase noise performance to support NRZ data rates up to 2 Mbps.

The bit synchronizer effectively phase-locks the VCO to the data transitions of the incoming NRZ data stream. Two of the primary areas which must be addressed are i) center frequency accuracy and ii) phase noise performance. We can obtain some useful insight into the center frequency accuracy requirements using the simple arguments presented next.

3.1.1 Capture Range Implications Upon VCO Center Frequency Accuracy

A high degree of VCO center frequency accuracy is required in the bit synchronizer in order to avoid the need for a large closed-loop bandwidth during the acquisition process. A second alternative to the large acquisition bandwidth is of course to perform an acquisition sweep search using a smaller loop bandwidth, but this is not without its complications. In the next few paragraphs, we will examine the needed loop bandwidth requirements for acquisition as driven by VCO center frequency misalignment.

In the present context, the symbol shape which reaches the bit synchronizer input will be quite smooth due to the Bessel prefiltering which is performed at the transmitter. If we assume that a square-root raised cosine pulse with excess bandwidth factor 0.5 is representative for this situation, it can be shown that a N=3 Butterworth lowpass filter with BT= 0.5 is less than 0.5 dB from theory at a bit error rate (BER) of 10^{-5}. The (one-sided) noise bandwidth for this filter is given by

$$B_n = \frac{f_c}{\frac{2n}{\pi}\sin\left(\frac{\pi}{2n}\right)} \quad Hz \qquad (5)$$

where f_c is the filter 3 dB corner frequency (Hz) and n is the filter order. Therefore, for a N=3 Butterworth filter,

$$\begin{aligned} B_n &= 1.047\ f_c = 1.047\ x\ 0.5\ x\ R \\ &= 0.524\ R\ Hz \end{aligned} \qquad (6)$$

where R is the NRZ symbol rate in bits per second. The variance of the noise at the matched filter output is given by

$$\sigma_n^2 = N_o B_n = 0.524 N_o R \quad (7)$$

where N_o is the one-sided noise power spectral density (W/Hz). The effective variance seen by the tracking loop will be much less than this quantity since the (one-sided) loop bandwidth B_L is generally much less than B_n.

Assuming an alternating 1/0 data stream, the input signal has the appearance of a sine wave embedded in noise where the energy per bit is given by roughly

$$E_b = \frac{A^2}{2} T \quad (8)$$

where A is the baseband signal amplitude (V) and T is the symbol period (sec). The phase variance seen by the tracking loop due to the flat input noise spectrum N_o (one-sided) is then given by (see Appendix I)

$$\sigma_\theta^2 \approx \frac{2N_o B_L}{A^2} \; rad^2 = \left(\frac{B_L}{R}\right)\frac{1}{E_b/N_o} \; rad^2 \quad (9)$$

where the NRZ bit rate is given by $R = T^{-1}$. The loop signal to noise ratio, ρ, is given by

$$\rho = \frac{1}{2\sigma_\theta^2} \quad (10)$$

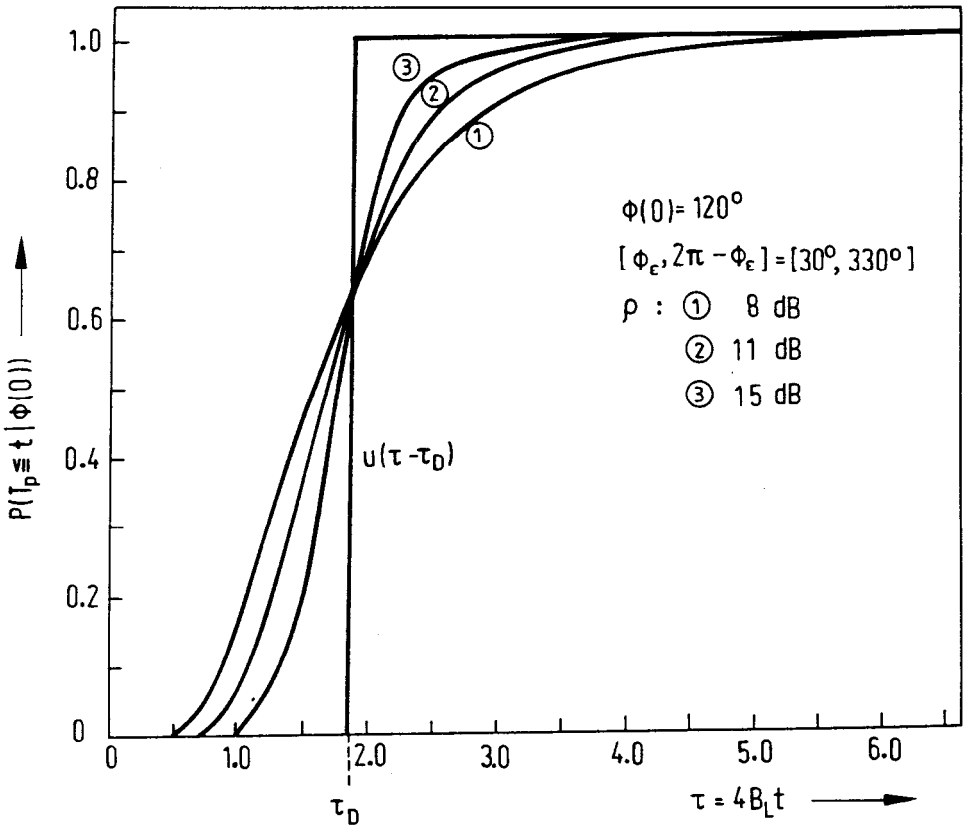
and for a classic second-order phase-locked loop,

$$B_L = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right) Hz \quad (11)$$

Putting these relationships together, we obtain

$$\rho = \frac{R}{\omega_n} \frac{1}{\left(\zeta + \frac{1}{4\zeta}\right)} \left(\frac{E_b}{N_o}\right) \qquad (12)$$

As supported by Figures 8 and 9 from [1], we should have a loop SNR of 15 dB or more for reliable acquisition. A number of researchers argue that capture is not possible for loop SNRs < 6 dB [2-3]. If we take ζ as 1.0, for a minimum E_b/N_o of 6 dB and a loop SNR ρ of 15 dB, we find from (12) that the loop natural frequency can be at most 1.6 percent of the NRZ data rate. This forces the VCO center frequency accuracy to be a primary design parameter for the entire synchronizer.



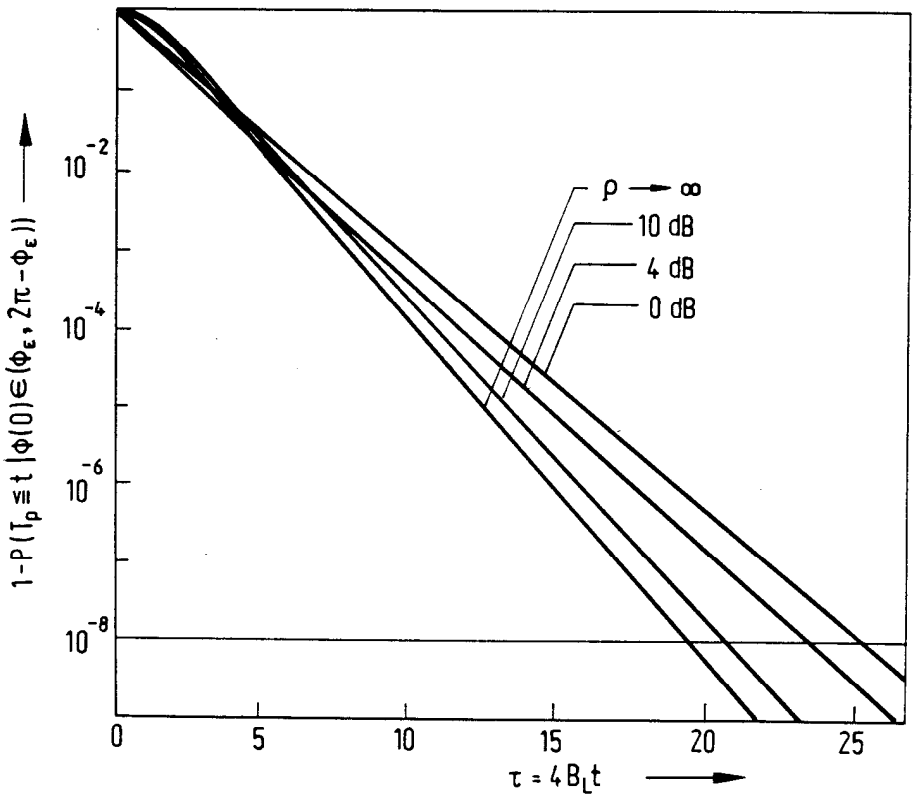
Conditional probability of acquiring lock $P[T_p \leq t \mid \phi(0) = 120°]$ (From Heinrich Meyr and Luitjens Popken, Phase Acquisition Statistics for Phase-Locked Loops, *IEEE Transactions on Communications*, Vol. 28, No. 8 © IEEE 1980).

Figure 8.

It is important to note that Figures 8 and 9 assume that the frequency error is zero. In general, the presence of a frequency error greatly detracts from the acquisition performance, lengthening the acquisition time and worst case, preventing acquisition from occuring at all.

From another perspective, the loop may capture the input signal only if the observed phase error during the pull-in process does not exhibit substantial cycle slipping. The criteria may be based upon the total peak phase error due to noise and the application of a step frequency change representing the VCO frequency error with respect to the incoming data rate. Mathematically, this may be expressed as

$$3\sigma_\theta + \theta_p \leq \frac{\pi}{2} \tag{13}$$



Probability of synchronization failure for a uniformly distributed initial phase error $\phi(0) \in [\phi_\varepsilon, 2\pi - \phi_\varepsilon]$ (From Heinrich Meyr and Luitjens Popken, Phase Acquisition Statistics for Phase-Locked Loops, *IEEE Transactions on Communications*, Vol. 28, No. 8 © IEEE 1980).

Figure 9.

where σ_θ is the standard deviation of the phase error due to noise and θ_p is the peak phase error due to the assumed step frequency error. A three-sigma condition was assumed for the peak value of the additive noise term. From [2] we have for $\zeta<1$ that

$$\theta_p = \frac{\Delta\omega}{\omega_n} \exp\left[-\frac{\zeta}{\sqrt{1-\zeta^2}} \tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta} \right) \right] rad \qquad (14)$$

and for $\zeta = 1$,

$$\theta_p = \frac{\Delta\omega}{\omega_n} \; rad \qquad (15)$$

Relating $\Delta\omega$ to the data bit rate R for the 1,0,1... data pattern case, we have that the data rate difference with respect to the nominal rate may be represented by

$$\frac{\Delta\omega}{2\pi} = \frac{\Delta R}{2} \qquad (16)$$

If we assume that $\zeta = 1$, combining (14), (15), and (16), we obtain the inequality

$$3\sqrt{\frac{5}{4}\pi\left(\frac{f_n}{R}\right)\frac{1}{(E_b/N_o)}} + \left(\frac{\Delta R}{2f_n}\right) \le \frac{\pi}{2} \qquad (17)$$

where f_n is the loop natural frequency in Hertz. Evaluating (17) for a loop natural frequency of 1.6 percent of R and an E_b/N_o of 6 dB, the data rate anomoly may be as large as 3.8 percent. Although this is an attractive result, the results indicates nothing about the locking speed which will result. More importantly, the self-noise of the phase detector due to the random nature of the incoming data has not been included in this discussion, and it is on the order of the incoming white noise term included here or stronger. This would force us to use a smaller loop bandwidth than the present theory would predict for tracking mode which leads to a decrease in the capture range unless the acquisition mode is handled separately.

A number of other factors seriously affect the design if the capture range requirement is excessive. It is quite straight forward to show that the tracking loop must have a bandwidth less

than B/4 Hz in order to be stable. Additionally, the desire to accomodate a transition density range (presently unspecified but probably 30% to 100% for NRZ) results in ω_n spanning a range of 1.0 : 1.83 further complicating the stability issue. Large bandwidth tracking loops are also imcompatible with long data run lengths for NRZ signals. (This is obviously not a problem with Manchester signals.) These facts combined with the phase detector self-noise problems alluded to above generally force us to use tracking loop bandwidths which are typically less than one percent of the data rate R.

One solution to the VCO center frequency accuracy problem is of course to use a VCXO for the bit synchronizer VCO. The primary problem here is that the pull range for such oscillators is only at best roughly 0.1 % which is substantially less than the 1 % design requirement presently imposed. A second alternative is to sweep an LC VCO over the frequency range of uncertainty, detect when phase acquisition has in fact occurred, and switch from acquisition mode to tracking mode. This is a popular method which has been used for many years. In the case of a carrier acquisition application, the permissible sweep rate for an acquisition probability of 0.90 is given by [3]

$$R_{90} = 0.5431 \left(1 - \sqrt{\frac{2}{\rho}} \right) B_L^2 \quad Hz/s \tag{18}$$

where a damping factor of 0.707 is assumed. The difficulty with this approach in the present context is primarily one of circuit complexity and available real estate. Not only does the additional sweep circuitry need to be included, but means to reliably detect lock and loss of lock must also be provided. If an external controller could assist in the decision making processes, this is an attractive approach to take unless the acquisition speed requirements are excessive. The decision not to use a sweep-type acquisition was based upon the need for i) fairly fast acquisition and ii) the desire that the bit synchronizer be a stand-alone functional module.

Another possible solution is to use a direct digital synthesizer. However, a completely integrated design would be required for the space presently available, and the temperature range would be a problem for presently available devices. Cost would also be fairly high for this approach.

The final oscillator approach which was adopted is shown in Figure 10. It consists of an LC VCO upconverted with a crystal oscillator followed by a divide operation which eases the LC VCO center frequency accuracy and phase noise requirements. As a side note, others have proposed phase-frequency locked methods to accomplish much the same final result [4]. Using this approach, the center frequency accuracy requirements for the LC oscillator are reduced by a factor of 4.8 : 1. This frequency plan is well suited

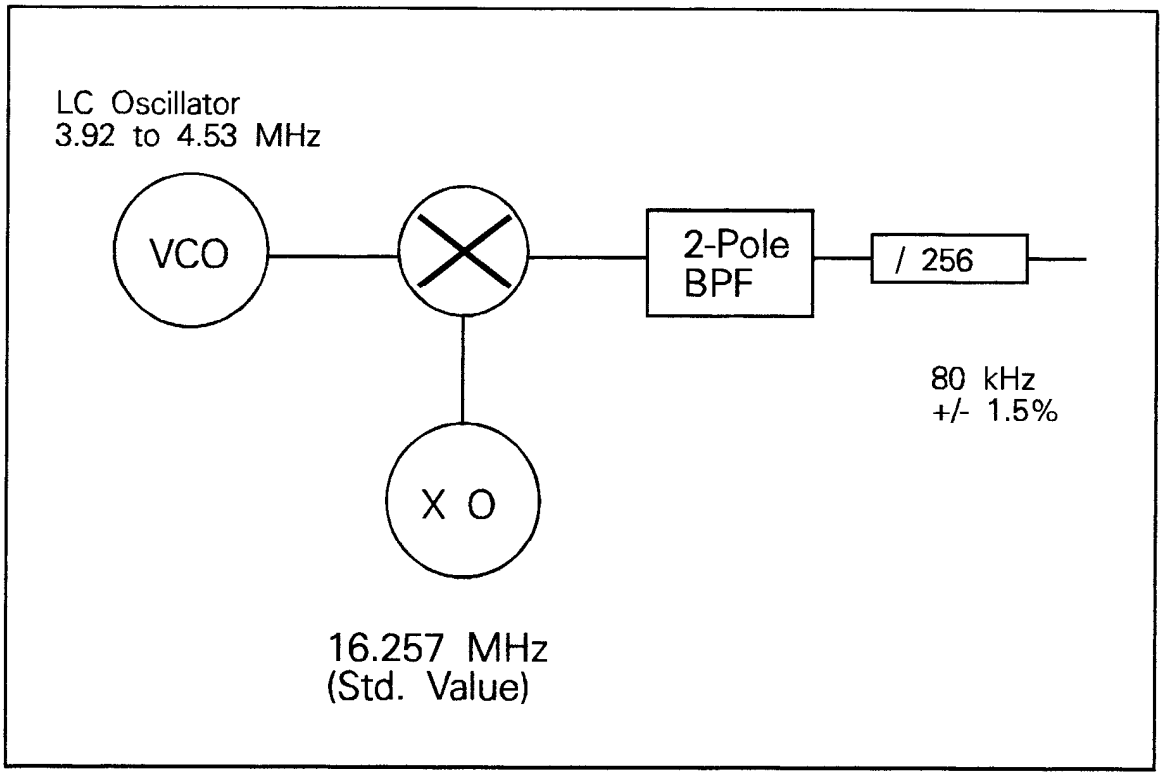


Figure 10 VCO Implementation for Canadair

for the Canadair project, the upconversion and divide operation reducing the LC oscillator phase noise contributions at the output by 62 dB. Although this degree of spectrum cleanup is certainly overkill, Loral dictated that the design be viable for NRZ data rates as high as 2 Mbps where the output divider ratios would of course be substantially smaller. Since this approach provides very good oscillator center frequency accuracy, initial acquisition may be performed by simply using a larger loop bandwidth than that used for the tracking mode. The actual bandwidths paramters chosen will be discussed later.

3.1.2 Phase Noise Requirements

The phase noise requirements of the LC oscillator for the Canadair project are not difficult to meet owing primarily to the large output divider ratio which improves the LC oscillator phase noise spectrum by 48 dB. The theory is developed here nonetheless for follow on applications where this may not be the case.

During steady-state operation, the oscillator phase noise spectrum leads to a random phase error which is equivalent to a random timing error in the clock recovery. The variance of this phase error is given by

$$\sigma_v^2 = \int_{-\infty}^{\infty} S_\theta(f) \, | 1 - H(f) |^2 \, df \qquad rad^2 \tag{19}$$

where $S_\theta(f)$ is the oscillator phase noise spectrum and H(f) is the closed-loop transfer function for the tracking loop. The square root of this variance term should be a small quantity, ideally less than 0.02 radians for negligible effect.

The run length issue poses another interesting perspective on the oscillator requirements. During a run of 1's or 0's (NRZ data), since no data transitions are present, the VCO is essentially running open-loop, free to follow its own phase trajectory as it pleases. Obviously, if the phase deviates too far from ideal during the run, the clock recovery may slip an appreciable portion of a symbol leading to poor error performance. This situation is generally dealt with by requiring the VCO excess phase accumulation over the run length to be less than a prescribed quantity which can then be related back to the VCO phase noise spectrum as follows. It can be shown that the variance of the excess phase accumulation over a period of time τ (for wide-sense stationary random phase processes) is given by

$$\sigma_\Delta^2(\tau) = 2[\, R_\theta(0) - R_\theta(\tau) \,] \tag{20}$$

where R_θ is the autocorrelation function of the underlying phase noise process. Using the Wiener-Khinchin theorem, this may be expressed in terms of the VCO phase noise spectrum as

$$\sigma_\Delta^2(\tau) = 8 \int_0^\infty S_\theta(f) \sin^2(\pi f \tau)\, df \tag{21}$$

where the phase noise spectrum $S_\theta(f)$ was assumed to be symmetric. This may be directly related to the phase noise as measured on a spectrum analyzer as

$$\mathcal{L}(f) = \frac{1}{2} S_\theta(f) \tag{22}$$

Proof of this latter point is given in Appendix II. Assume that the oscillator phase noise spectrum may be modeled by

$$\mathcal{L}(f) = \frac{K}{\omega^2} \quad rad^2/Hz \tag{23}$$

Substituting this result, we have

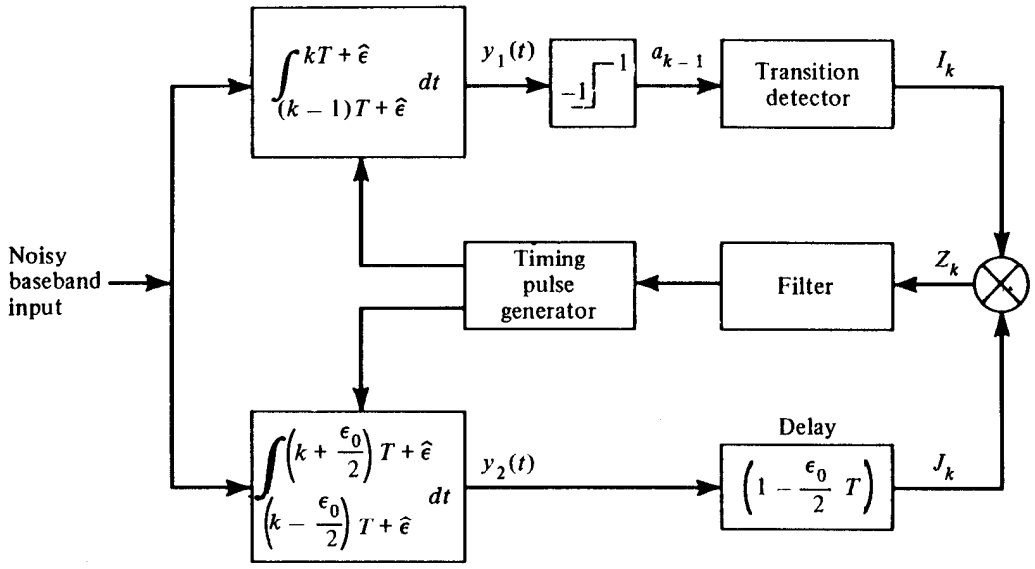
$$\begin{aligned} \sigma_\Delta^2(\tau) &= 16 \int_0^\infty \mathcal{L}(f) \sin^2(\pi f \tau)\, df \\ &= 4K\tau^2 \int_0^\infty \frac{\sin^2(\pi f \tau)}{(\pi f \tau)^2}\, df \\ &= 2K\tau \quad rad^2 \end{aligned} \tag{24}$$

For the 80 kbps NRZ case at hand, the maximum run length is required to be 30 Manchester symbol periods (60 NRZ symbols) making τ= 60/80 kHz or 750 microseconds. (Run length is not an issue for bi-phase.) If we require that the oscillator excess phase over this time period have a standard deviation of less than 10 degrees, then $K \leq 20.31$ implying that the oscillator spectrum at 1 kHz offset must be less than -63 dBc/Hz.

3.2 Transition-Tracking Phase Detectors

The phase detector portion of the bit synchronizer is responsible for estimating the timing error between the local clock and that of the incoming noise corrupted data stream. A rigorous study of this area can be quite involved, generally involving subjects such as cyclostationary processes. We will avoid such discussions here, but [6-17] are provided as reference.

Many factors lead me to take the digital transition tracking method [18] as the baseline concept for the Canadair project. In the present context, this detector results in an unbiased phase error estimate with no self-noise in the limiting case. One form of this type of bit synchronizer is shown here in Figure 11.



Block diagram of an in-phase/midphase symbol synchronizer.

Figure 11. Transition-tracking bit synchronizer from [21].

A close-up of the phase detector concept used in this configuration (with hard-limited output) is shown in Figure 12. The hard-limiting, although simplifing the hardware, results in substantial phase detector self-noise which cannot be neglected in the design analysis. The synchronizer discussed in [18] used a maximum loop bandwidth of only 0.2%.

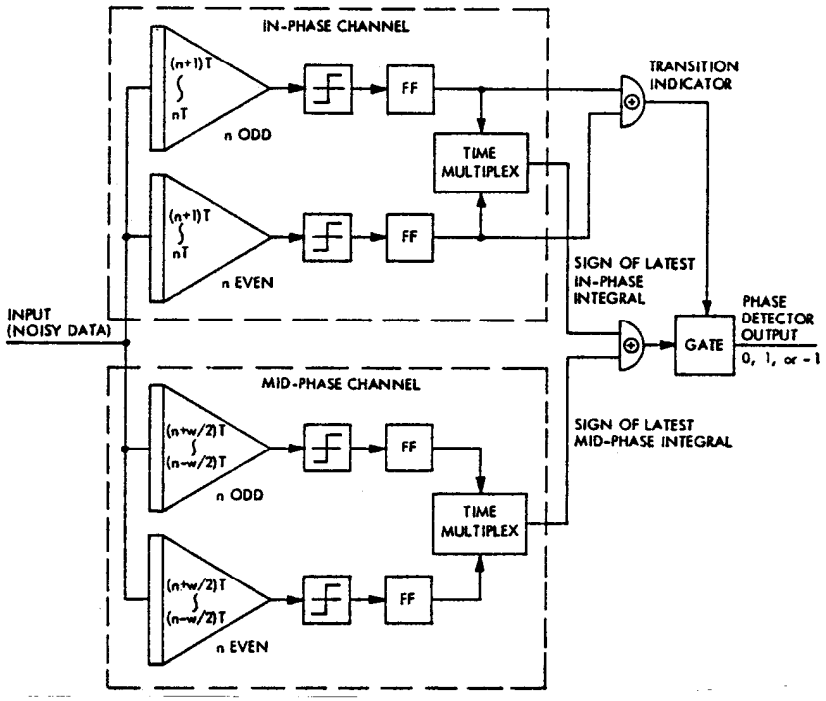


Figure 12. Phase detector details pertaining to Figure 11 [18].

One of the most simple phase detector types is the classic early-late gate type. The primary problem with this type of phase detector is that the phase detector self-noise is substantial, limiting us to loop bandwidths substantially less that one percent of the NRZ data rate. This limitation would primarily manifest itself as reduced acquisition speed in the Canadair project. Assuming random data, the spectral density of the self-noise may be derived as follows.

For a locked tracking loop in the absence of noise, the phase detector error output may be modeled as

$$\theta_e(t) = \sum_{n=-\infty}^{\infty} a_n \, rect(t-nT) \tag{25}$$

where the a_n are independent random variables taking values of $\pm 2\pi$ equally likely. The autocorrelation function is given by

$$R_{\theta_e}(\tau) = 4\,\pi^2 \bigwedge(\tau) \tag{26}$$

where

$$\Lambda(\tau) = 1 - \frac{|\tau|}{T} \quad for\ |\tau| \le T$$
$$else\ 0 \tag{27}$$

The one-sided power spectral density may be found to be

$$S_{\theta_e}(f) = \frac{8\pi^2}{R}\frac{\sin^2(\pi fT)}{(\pi fT)^2} \quad rad^2/Hz \tag{28}$$

Using this result, the tracking error variance due to the self-noise alone is (assuming a small loop bandwidth $B_L << 1/2T$)

$$\sigma_e^2 \approx \frac{8\pi^2}{R}B_L \quad rad^2 \tag{29}$$

or

$$\sigma_e \approx 2\pi\sqrt{\frac{2B_L}{R}} \quad rad. \tag{30}$$

Therefore, for a 1% tracking bandwidth, σ_e = 50 degrees rms which is equivalent to a loop SNR of only -1.8 dB. This is clearly nonsense. In order to obtain a loop SNR of 15 dB due to this self-noise term, the maximum loop bandwidth may be at most 0.02% which is clearly very small.

A much simpler phase detector design which has been proposed based upon the transition tracking concept is developed in [19]. Although a patent is pending (or by now awarded) on the method, it leads to substantial circuit simplification which is well worth any minor royalty charges which may be involved. This detector concept (without any matched filter) is shown in Figure 12.

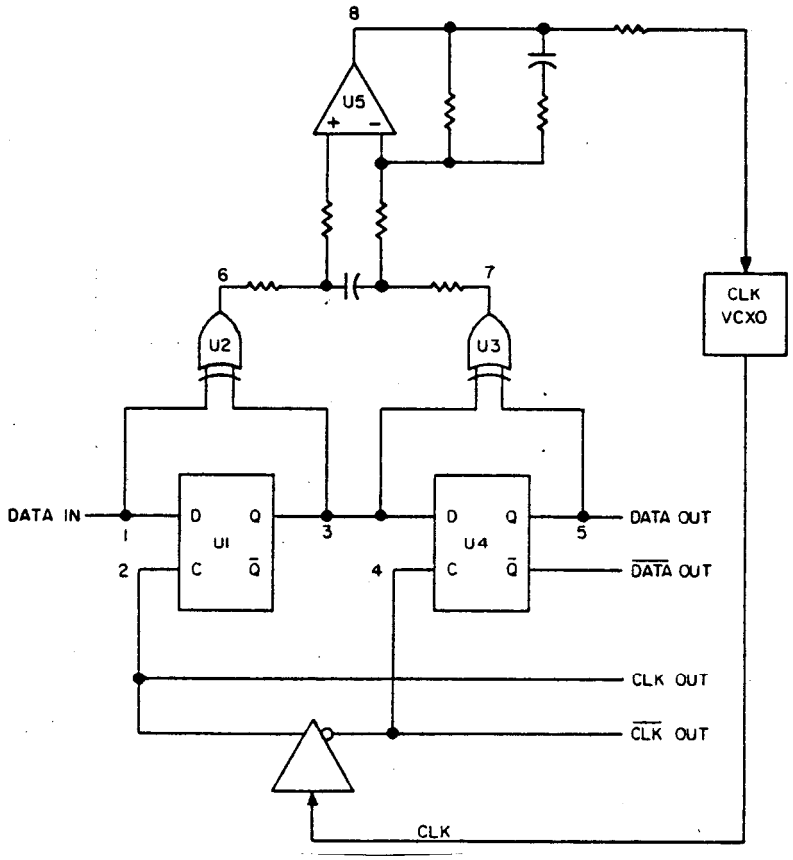


Figure 12. Hogge NRZ bit synchronizer concept [19].

As pointed out in [20], the Hogge method is not completely free of phase detector self-noise due to the π phase difference between the signals at nodes 6 and 7 in Figure 12. This situation may be improved as discussed in [20]. Nonetheless, we will take the Hogge method as our baseline since Hogge is with a domestic firm.

From [20], the power spectral density of the phase error signal in the Hogge method (no noise or ISI) is given by

$$S_e(\omega) = 4\pi^2 T \left| sinc\left(\frac{\omega T}{4\pi}\right) \right|^2 \left| \sin\left(\frac{\omega T}{4}\right) \right|^2 \qquad (31)$$

for random data. We will use this result in the detailed design portion of this memo in the next section.

3.3 Loop Filter and Loop Parameters

In this next section, we will identify the tracking loop parameters needed for the Canadair bit synchronizer. From there, it will be fairly straight-forward to back out what kind of acquisition performance we can obtain prior to entering tracking mode.

The primary requirements in the tracking mode are i) to achieve less than 0.5 % rms clock jitter at 12 dB E_b/N_o and ii) have a run length capability exceeding 30 symbols. Again, the run length is immaterial for the Manchester waveform.

The tracking loop parameters may be identified as follows. Assuming that the phase detector gain is given by K_{do} volts/radian for an alternating 1,0,1... NRZ data pattern (100% transition density), the effective phase detector gain with random data present is given by

$$K_d = K_{do}\,\eta \tag{32}$$

where η is the data stream average transition density. Assuming that the VCO tuning sensitivity is given by K_v rad/s/V and a classic type-2 control loop, the open-loop gain is given by

$$\begin{aligned} G_{OL}(s) &= \frac{K_d\,K_v}{s}\,\frac{1 + s\tau_2}{s\,\tau_1} \\ &= \omega_n^2\,\frac{1 + 2\zeta s/\omega_n}{s^2} \end{aligned} \tag{33}$$

where

$$\begin{aligned} \omega_n &= \sqrt{\frac{K_d\,K_v}{\tau_1}} \\ \zeta &= \frac{1}{2}\omega_n\tau_2 \end{aligned} \tag{34}$$

The closed-loop transfer function is the classic result

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{\omega_n^2\,(1 + 2\zeta s/\omega_n)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (35)$$

The primary noise contributors to the tracking jitter are

1) ISI noise which is assumed to be negligible,
2) additive Gaussian noise,
3) VCO self-noise
4) phase detector self-noise (data-dependent)

The planned VCO approach will have very low self-noise therefore leaving items (2) and (4) as the primary jitter contributors which must be addressed. As reasoned earlier, the tracking error variance due to the Gaussian noise is given by roughly

$$\sigma_n^2 = \frac{B_L}{R}\frac{1}{E_b/N_o} \quad rad^2 \qquad (36)$$

The (one-sided) noise power spectral density of the data-dependent self-noise was given earlier in (31) as

$$S_e(f) = \frac{4\pi^2}{R}\frac{\sin^2(\pi fT/2)}{(\pi fT/2)^2}\sin^2(\pi fT/2) \quad rad^2/Hz \qquad (37)$$

The tracking error variance due to this contribution is then given by

$$\sigma^2 = \frac{4\pi^2}{R}\int_0^{\infty}\frac{\sin^2(\pi fT/2)}{(\pi fT/2)^2}\sin^2(\pi fT/2)\,|H(f)|^2\,df \qquad (38)$$

For very small loop bandwidths compared to the data rate, this may be approximated as

$$\sigma^2 \approx \frac{4\pi^2}{R}\int_0^{\alpha B_L}\left(\frac{\pi fT}{2}\right)^2 df \quad rad^2 \qquad (39)$$

which may be further simplified to

$$\sigma^2 = \frac{\pi^4}{3}\left(\frac{\alpha\ B_L}{R}\right)^3 \ rad^2 \qquad (40)$$

where $\alpha\ B_L$ is the assumed extent of the pattern noise within the tracking loop. The parameter α depends upon additional filtering within the control loop beyond that normally found in an ideal type-2 system. Combining (36) and (40), we find the total track variance to be given by

$$\sigma_T^2 = \left(\frac{B_L}{R}\right)\frac{1}{E_b/N_o} + \frac{\pi^4}{3}\left(\frac{4B_L}{R}\right)^3 \ rad^2 \qquad (41)$$

where an α of 4 was adopted. This result may be used to examine some typical parameter choices as shown below in Table III.

Table III Track Variance Versus Loop SNR

B_L/R	E_b/N_o, dB	σ_T^2, rad²	RMS Jitter, %
0.01	12	0.00271	0.828
	14	0.00248	0.792
	16	0.00233	0.768

Note: These values are different than the original writeup because a slightly different E_b/N_o relationship was used, and upon my own derivation of (37) it was found that the original reference was for a one-sided spectrum rather than a two-sided spectrum as I initially assumed.

The phase detector self-noise term is appreciable in setting the loop SNR as evidenced in Table III. This term was evaluated separately for a number of parameter choices as shown in Table IV.

Table IV Tracking Jitter Due to Phase Detector Self-Noise

	RMS Jitter, %		
B_L/R	α= 2	α= 3	α= 4
0.001			0.023
0.005			0.26
0.01		0.47	0.73
0.015	0.47	0.86	1.33
0.02	0.73	1.33	2.05
0.03	1.33	2.45	3.77
0.04	2.05	3.77	5.81
0.05	2.87	5.27	8.11

Note: Values differ from original writeup. See note, Table III.

Similarly, the jitter due to the additive Gaussian noise term may be evaluated as shown in Table V.

Table V Tracking Jitter Due to Additive Noise

		Jitter, % RMS		
B_L/R	E_b/N_o=	6 dB	10 dB	12 dB
0.002		0.36	0.23	0.18
0.005		0.56	0.36	0.28
0.01		0.80	0.50	0.40
0.015		0.98	0.62	0.49
0.02		1.13	0.71	0.57

The Gaussian variance contribution to the tracking error is fairly small compared to the self-noise contribution shown in Table IV, largely because the Gaussian noise spectrum is white whereas the self-noise spectrum is not. The primary motivation for reducing the loop bandwidth between acquisition and tracking modes is then to reduce the phase detector self-noise contribution to the tracking error variance.

From (32) and (34), the damping factor is a function of the transition density as given by

$$\zeta = \frac{1}{2}\sqrt{\frac{K_{do}\eta K_V}{\tau_1}}\,\tau_2 \qquad (42)$$

$$= \zeta_o\sqrt{\eta}$$

where ζ_o is the damping factor for a transition density of 100%. Therefore, a change in η from 30% to 100% results in a damping factor change of 1 to 1.83. The loop bandwidth changes similarly as given by

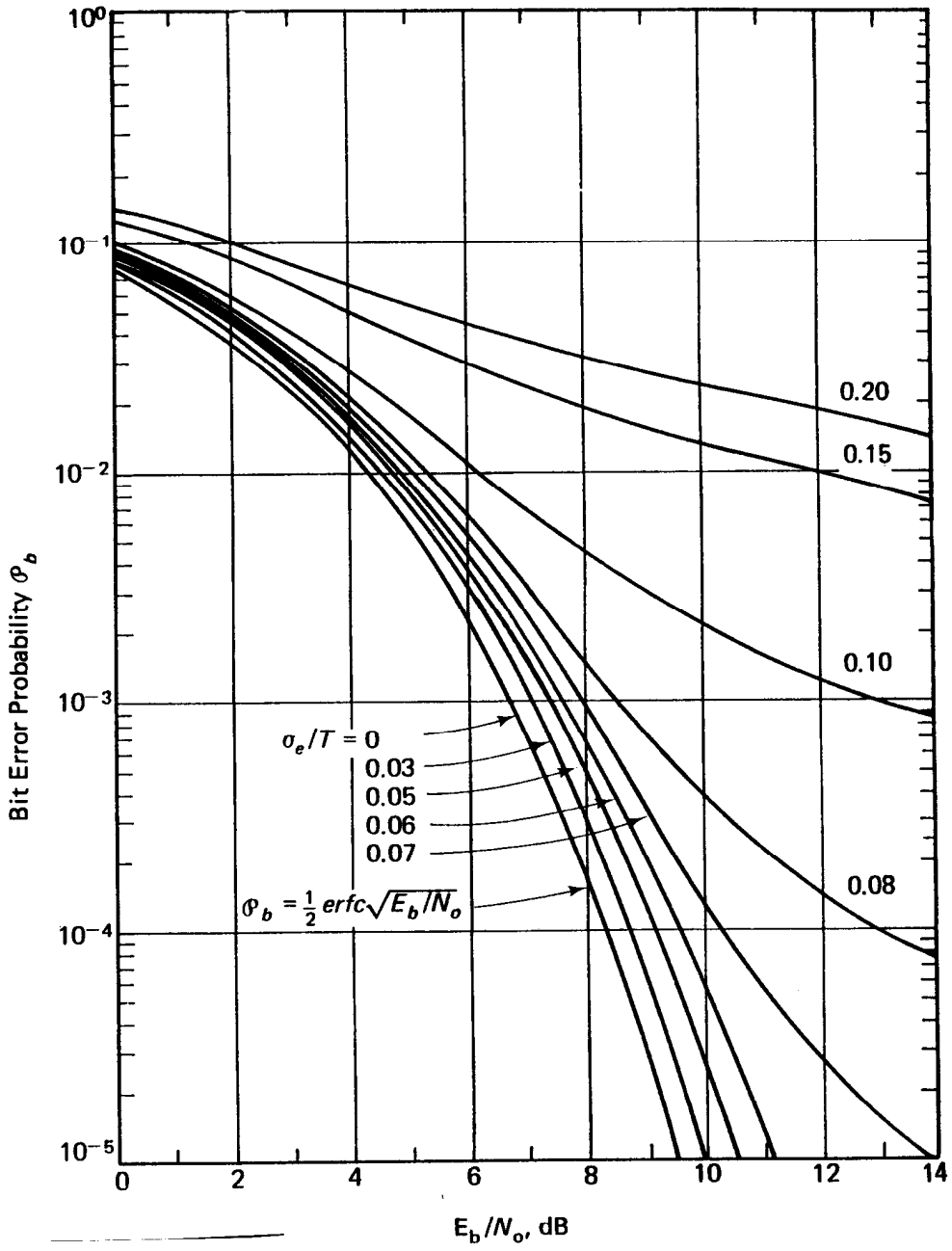
$$B_L = \frac{\omega_{no}}{2}\left(\zeta_o \eta + \frac{1}{4\zeta_o}\right) \qquad (43)$$

which results in a bandwidth range of 1.0 to 2.27. The parameter spread for Manchester signaling will of course be smaller since the minimum transition density in this case is 50%.

Based upon this information, a B_L of 0.005 was selected for the tracking mode in order to obtain adequately low clock jitter performance (See Table IV and V). In order to accomodate the range of transition densities expected, ζ_o was chosen to be 1.0 since this would result in a ζ of 0.55 for the minimum transition density. (For a given ω_n, a damping factor of 0.5 results in the minimum noise bandwidth for a classic second-order system.) This is also an adequate amount of damping to provide reasonable transient performance.

To some degree, discussion of loop parameters for acquisition is less clear because it is a stochastic process which is difficult to analyze except by simulation. The loop parameters selected for acquisition were chosen based upon i) the need to keep the ratio of parameters between acquisition and tracking modes reasonable so as not to loose lock when switching between acquisition and tracking modes, and ii) upon the rule of thumb to keep the associated rms jitter less than roughly 3%. This latter requirement was based upon the BER curves shown in Figure 14 where the 3% value results in negligible departure from theory. This is admittedly a very conservative position, and one which could be challenged. This rationale led to an acquisition bandwidth selection for B_L/R of 0.02. The damping factor choice for the acquisition mode was the same made for the tracking mode.

The forementioned bandwidths result in an acquisition to tracking loop bandwidth ratio of 4. This may seem small, but this requires for instance a 16:1 change in the loop τ_1. Larger ratios could of course be considered for faster acquisition performance, but not without an increased risk of loosing lock while handing off to the tracking mode. The adopted 4:1 ratio represented about the maximum ratio beyond which much more exhaustive analysis and simulation would be required to confirm performance. Based upon Figure 8, if the transition density is 100%, the data rate error zero, and the loop SNR > 15 dB, reliable synchronization should be achieved in $t \leq (B_L)^{-1}$ seconds which for NRZ symbols translates to 50 symbols. Based upon the available data (Appendix III), this is quite optimistic when random data is present, and a finite data rate error exists. Characterizing of the initial synchronization



Average probability of bit error versus E_b/N_0 with standard deviation of the symbol sync error σ_ϵ as a parameter (NRZ) [From Lindsey and Simon, 1973, 469, Fig. 9-37]

Figure 14.

statistics remains an area where additional evaluation would be valuable. Circuit implementation details are left to section 4.0.

3.4 Matched Filter Selection

Although the discussion of the bit synchronizer input filtering appears somewhat late in this discussion, it was in fact the first area that was analyzed during the design process. The principal reason for analyzing the matched filter performance first was that if the transmit premodulation filter had been chosen improperly, substantial intersymbol interference can result which degrades both the bit error rate performance due to eye closure as well as increasing the jitter on the recovered clock. Selection of the matched filter is a primary systems-level consideration which could have potentially involved the transmitter design also, so it only made sense to eliminate this possible problem as early as possible.

3.4.1 NRZ Matched Filter Selection

A simplified block diagram of the design situation for Canadair is shown in Figure 15. The FM subcarrier link is assumed to be transparent even though the input noise spectrum to the bit synchronizer will be parabolic rather than white as a result. In general, the complete analysis was carried on assuming that the synchronizer was baseband in nature. This was necessary since much of the needed information was unavailable to proceed otherwise and it led to significant simplification in the analysis/design effort.

It can be shown that the bit error probability for the system shown in Figure 15 can be computed as

$$P_e = \frac{1}{2} - \frac{1}{\pi} \int_0^{\infty} \frac{\sin[\omega p(t_o)]}{\omega} \, e^{-\frac{1}{2}\sigma^2\omega^2} \, C(\omega) \, d\omega \qquad (44)$$

where

$$C(\omega) = \prod_{e=-L;\neq 0}^{L} \cos[\, \omega \, p(t_o + e\,T) \,] \qquad (45)$$

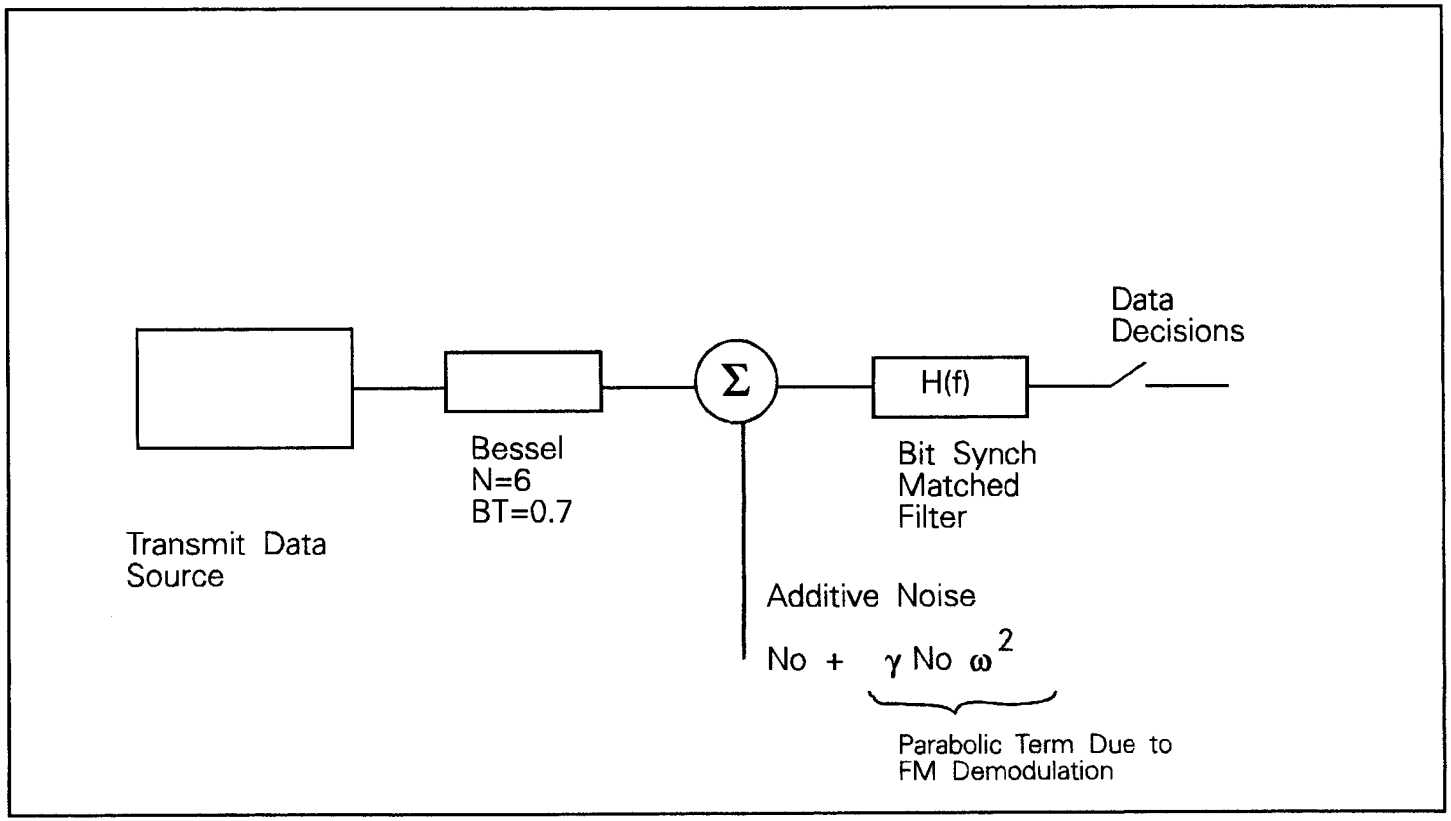


Figure 15. Analysis Model for Bit Synchronizer Matched Filter Optimization.

$$\sigma^2 = \int_{-\infty}^{\infty} \frac{N_o}{2} \left(1 + \gamma 4\pi^2 f^2 \right) | H(f) |^2 \, df \qquad (46)$$

and

- t_o Time corresponding to the received matched filter output peak
- T Symbol period, s
- L Number of adjacent symbols over which intersymbol interference is significant
- p(t) Received pulse shape out of the matched filter for a single symbol

A number of other approaches may be used to compute the bit-error probability but this is the approach used in the analysis software which I have written.

The data eye pattern immediately following the transmit filter $H_T(f)$ is shown in Figure 16. The constant group delay of the Bessel filter is clearly evident in that all of the signal trajectories are tight. Just arbitrarily selecting an N=3 Butterworth filter with BT= 0.5 for the bit synchronizer matched filter leads to the poor output eye pattern shown in Figure 17. Clearly, this haphazard choice would lead to substantial intersymbol interference (ISI).

In order to find a suitable matched filter for the bit synchronizer, the N=3 Butterworth and N=3 Chebyshev (0.1 dB ripple) families were initially considered for an acceptable solution since these filters were representative of the minimum useful complexity. The search was widened to a number of other filter types and these results are documented in the next several figures. In the end, an N=6 Bessel filter with BT= 0.6 was selected for the matched filter function. Once in PWB layout however, it was clear that the circuit density was going to be extreme, so an N=4 Bessel was actually implemented instead in order to reduce the parts count.

Once the bit synchronizer is integrated with the remaining elements of the Canadair system, the impact of the nonwhite noise spectrum (arising from the FM subcarrier demodulation) may become apparent, and tightening the matched filter bandwidth may be desirable. Again, if more information had been available at the outset, these factors could have been included in the original analysis. Since the noise spectrum will be an increasing function of frequency, it is important that the matched filter have an ultimate attenuation roll off which exceeds 20 dB per decade. Otherwise, the sample variance at the data decision point in the synchronizer will be unbounded. This condition is easily satisfied with the N=4 Bessel filter presently being used.

Additional plots are included in the next figures which show the performance degradation with respect to theory for the bit synchronizer as a function of static timing error in the clock recovery. These plots are valuable for quickly assessing the impact

of finite recovered clock jitter upon the actual matched filter mismatch loss. In lieu of having detailed information about the recovered clock jitter, normally the tracking error probability distribution is well approximated by the Tikhonov density which is given by

$$p(\theta) = \frac{e^{\rho \cos(\theta)}}{2\pi I_0(\rho)} \tag{47}$$

where ρ is the tracking loop SNR. The closed-loop system bit error probability can then be calculated as

$$P_e = \int_{-\pi}^{\pi} P_s(\theta)\ p(\theta)\ d\theta \tag{48}$$

and $P_s(\theta)$ is the probability of bit error given a static timing error of θ radians. This was precisely the procedure used in obtaining Figure 14.

Summarizing this section, the matched filter losses for the Canadair system (assuming a white noise spectrum out of the subcarrier demodulator) should be less than 1.0 dB based upon the results shown in Figure 38. Since the recovered clock jitter is being designed to be very small, losses relating to clock jitter should be negligible.

3.4.2 Mismatch Loss for Manchester Symbols

As stated earlier, originally Canadair was planning to use NRZ-L for the data link and this decision was later changed to Manchester. Use of the NRZ matched filter for receiving Manchester symbols leads to a 3 dB loss with respect to theory as we will now demonstrate. This loss could be almost completely avoided by going to 3-bit soft decisioning on the data decisions, but Loral chose not to incorporate this performance enhancement.

Assuming square NRZ symbols at the bit synchronizer input, the bit error rate is given by

$$P_{NRZ} = \frac{1}{2}\ erfc\left(\sqrt{\frac{E_s}{N_o}}\right) \tag{49}$$

where E_s is the energy per NRZ symbol and N_o is the one-sided noise power spectral density in watts/Hertz. In the Manchester symbol case, separate decisions are made on the first half and the second half of the symbol, treating each as an NRZ symbol. For Canadair, only the first half will be used to estimate the true data bit, and since this effectively results in throwing away half of the energy per symbol available, clearly, the loss must be 3 dB. Performing decisioning on the second half of the symbol leads to negligible improvement so the system is in fact left with a 3 dB performance loss.

Assuming that decisions are made on both halves of the Manchester symbol, further assume that the following decision rule has been adopted:

NRZ Bits Received=	10	01	11	00
Data Symbol Decision	1	0	1	0

Clearly the decision table entries for the "11" and "00" cases could be reversed, but this has no impact in the end. The probability of a Manchester symbol error is then

$$P_{se} = p_1 \left(p_{01|1} + p_{00|1} \right) + p_0 \left(p_{10|0} + p_{11|0} \right)$$

where

p_1	Probability of sending a data 1
p_0	Probability of sending a data 0
$p_{01\|1}$	Probability of receiving a 01 NRZ pattern when sending a data 1 Manchester symbol
$p_{00\|1}$	Probability of receiving a 00 NRZ pattern when sending a data 1 Manchester symbol
$p_{10\|0}$	Probability of receiving a 10 NRZ pattern when sending a data 0 Manchester symbol
$p_{11\|0}$	Probability of receiving a 11 NRZ pattern when sending a data 0 Manchester symbol

Assuming random 1 and 0 data symbols, the Manchester symbol error probability is given by

$$\begin{aligned} P_{se} &= \frac{1}{2}\left(p_b^2 + p_b(1-p_b) \right) + \frac{1}{2}\left(p_b^2 + p_b(1-p_b) \right) \\ &= p_b^2 + p_b(1-p_b) \\ &\approx p_b(1-p_b) \approx p_b \end{aligned} \qquad (50)$$

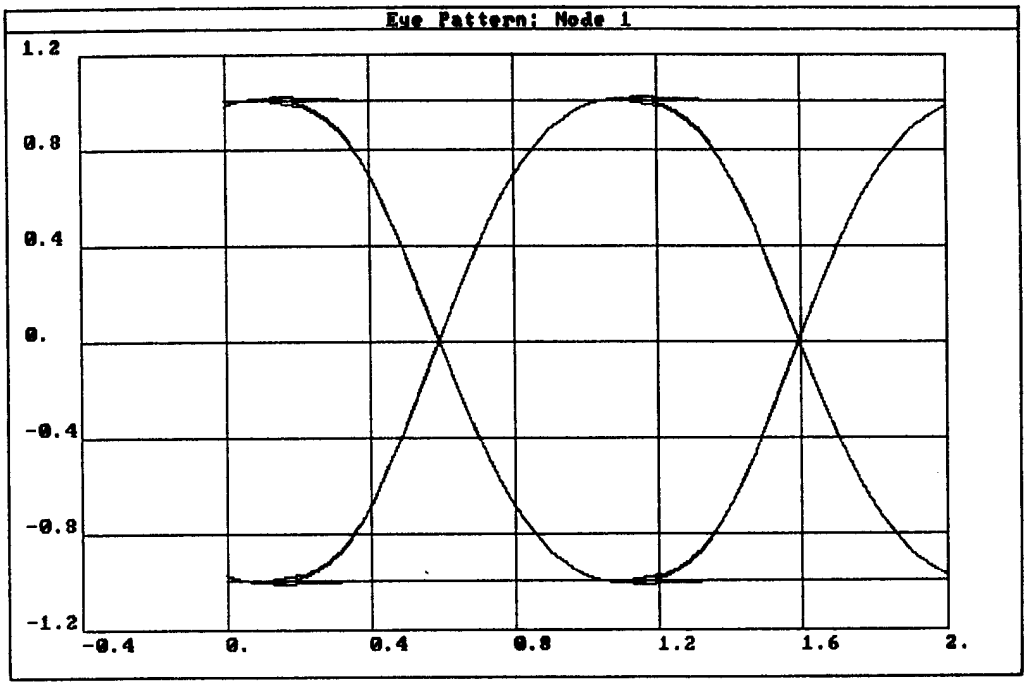


Figure 16. Eye diagram at the transmitter premodulation filter output.

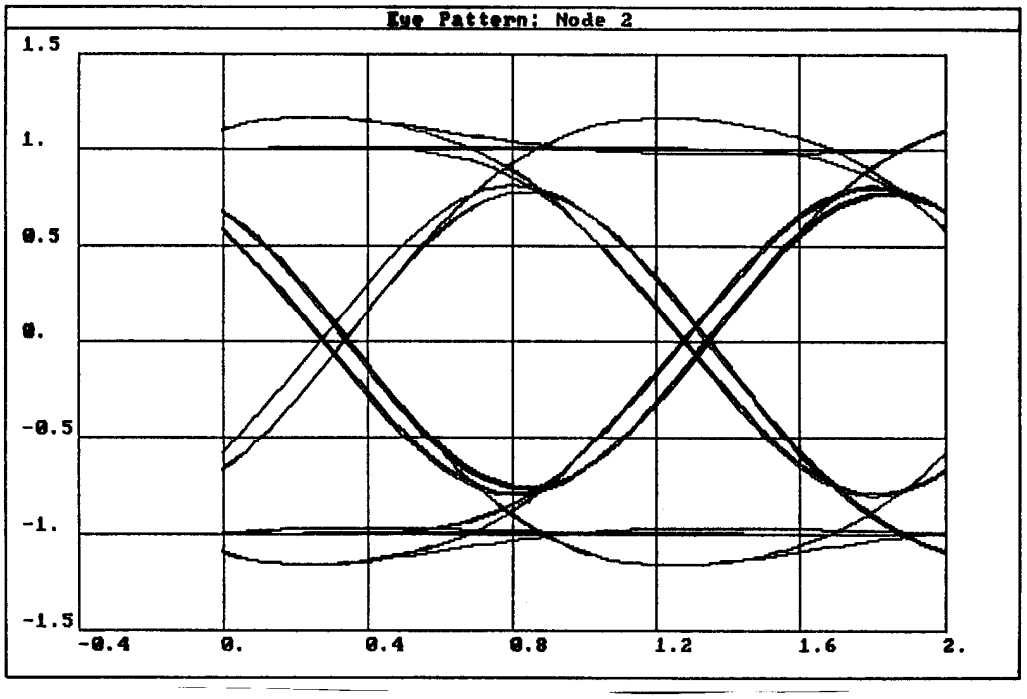


Figure 17. Recovered eye pattern at the bit synchronizer matched filter output for an N=3 Butterworth BT= 0.5 filter selection.

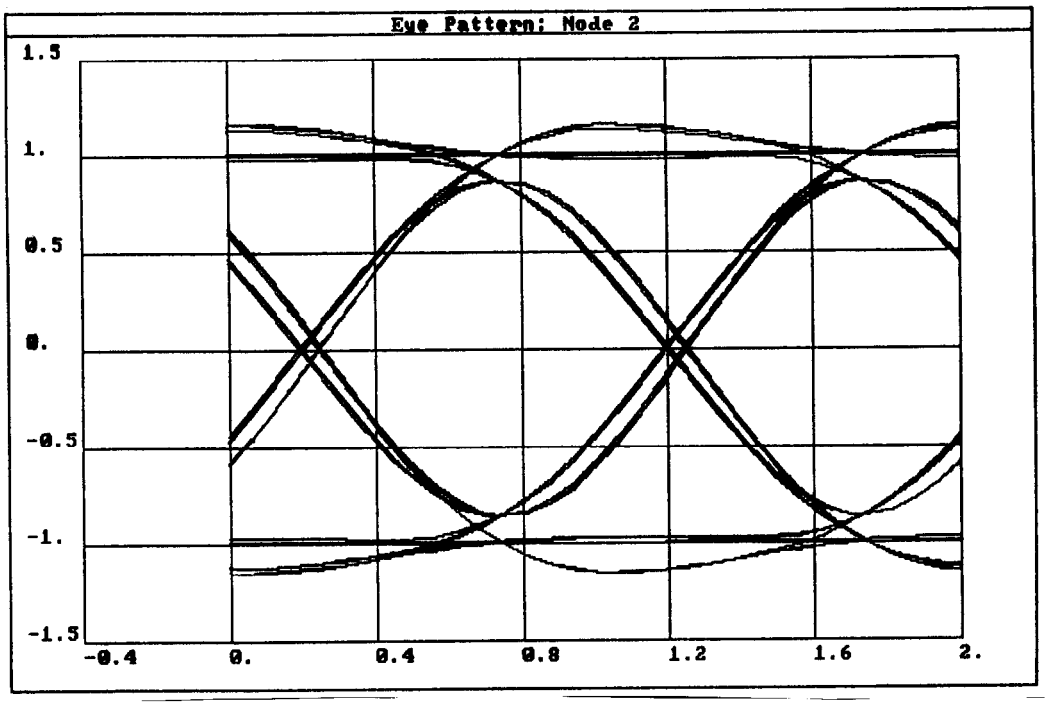


Figure 18. Bit synchronizer eye pattern for an N=3 Butterworth BT= 0.55 matched filter.

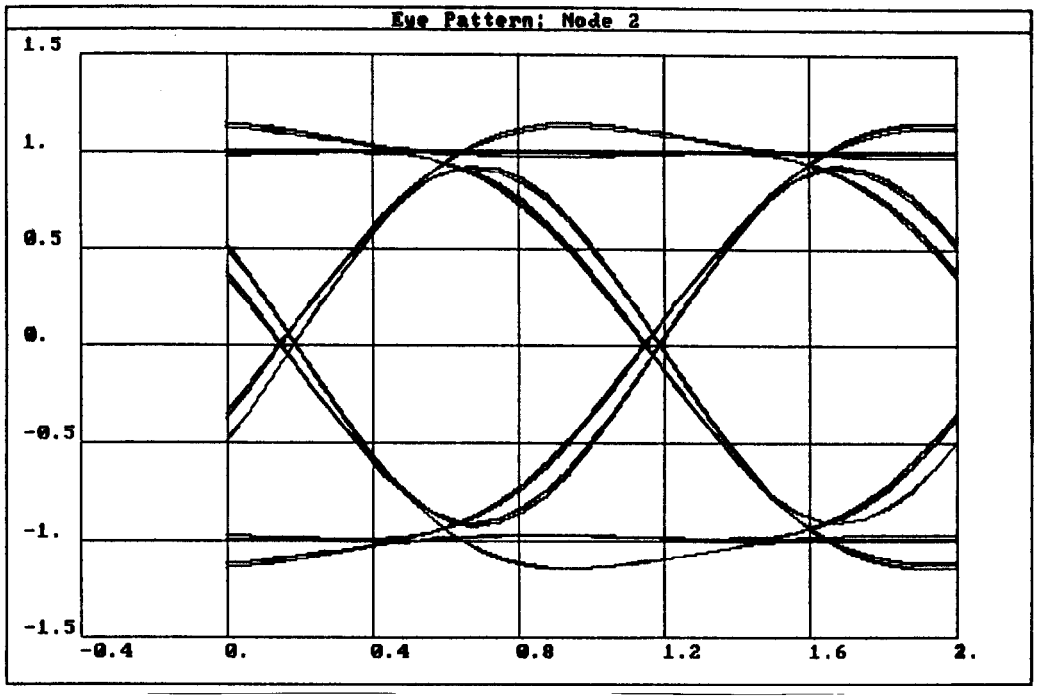


Figure 19. Bit synchronizer eye pattern for an N=3 Butterworth BT= 0.60 matched filter.

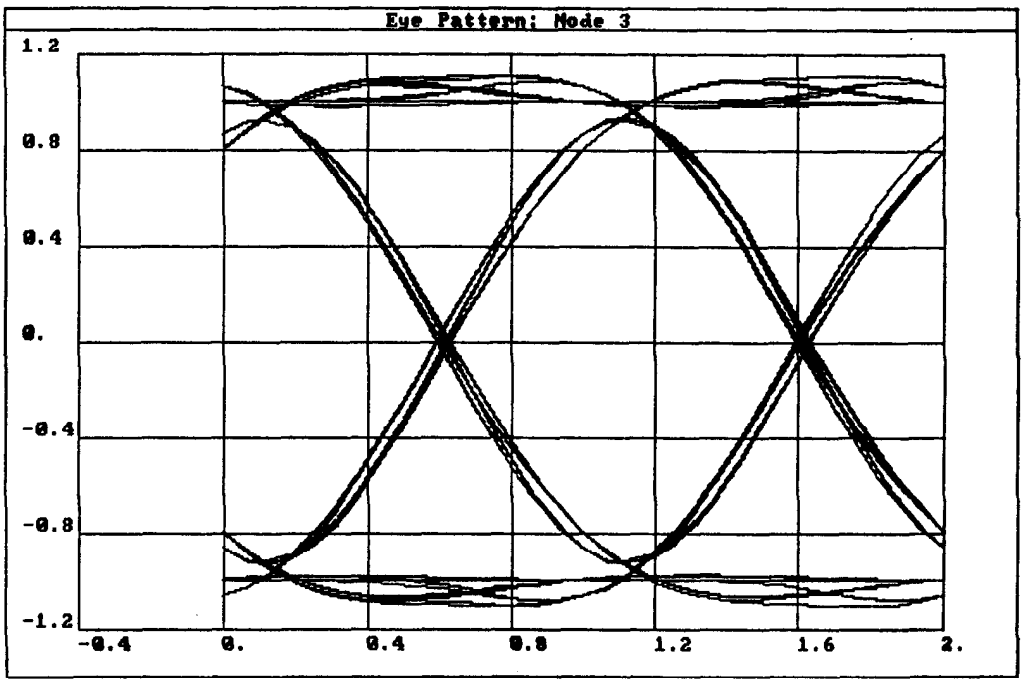


Figure 20. Bit synchronizer output eye pattern for an N=3 Butterworth BT= 0.60 matched filter with first order delay equalizer (equalizer BT=0.62).

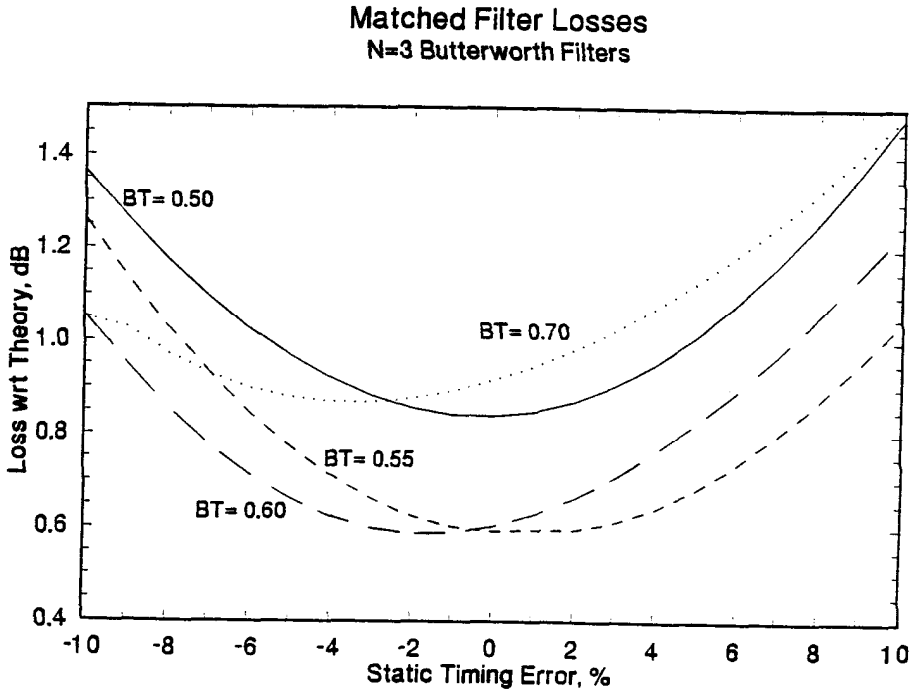


Figure 21. Bit synchronizer matched filter losses for the N=3 Butterworth family as a function of static clock recovery timing error.

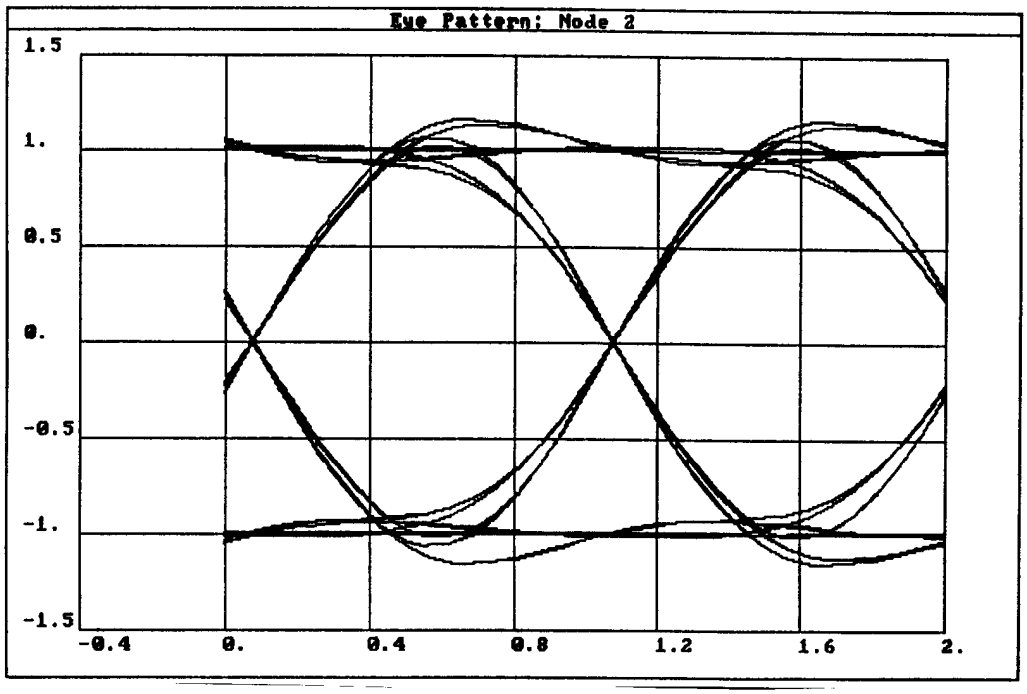


Figure 22. Bit synchronizer eye pattern for an N=3 Chebyshev 0.1 dB ripple BT= 0.55 matched filter.

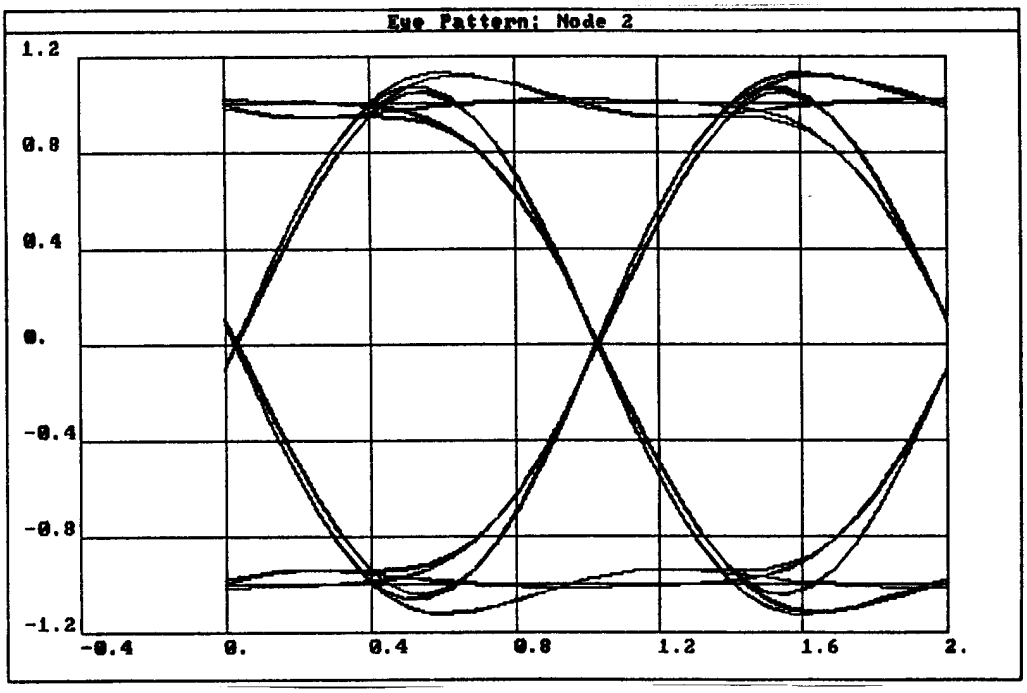


Figure 23. Bit synchronizer eye pattern for an N=3 Chebyshev 0.1 dB ripple BT= 0.60 matched filter.

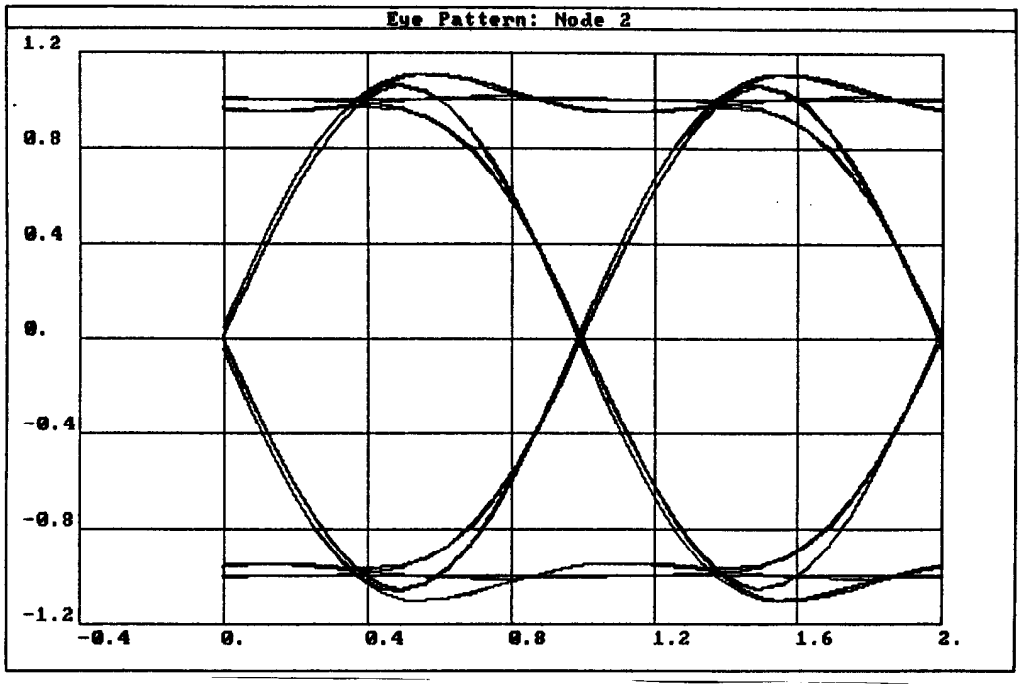


Figure 24. Bit synchronizer eye pattern for an N=3 Chebyshev 0.1 dB ripple BT= 0.65 matched filter.

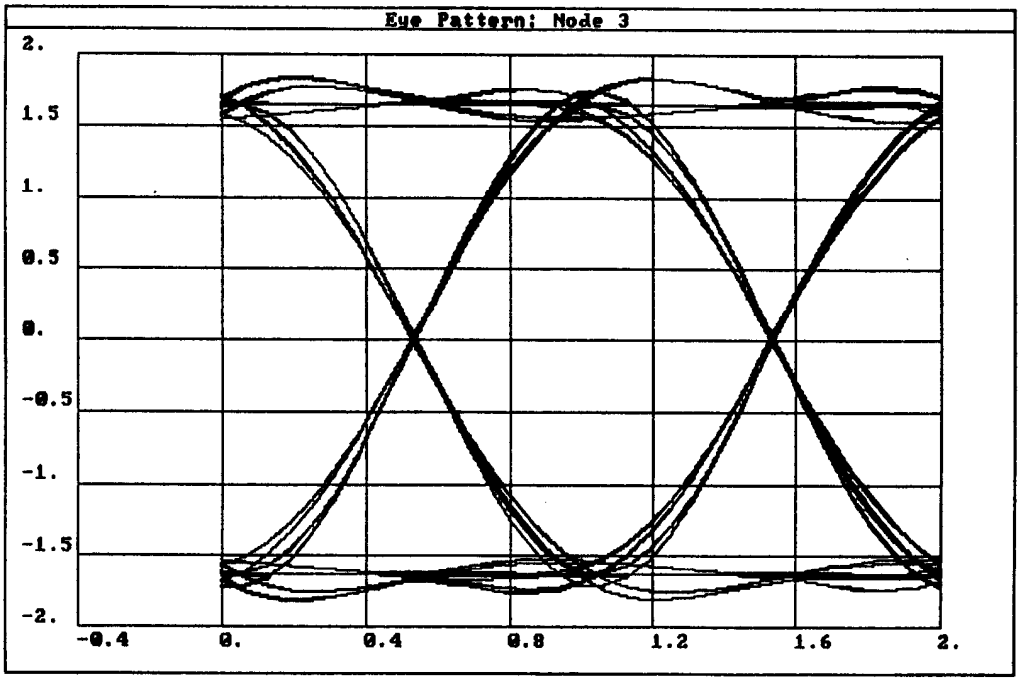


Figure 25. Bit synchronizer eye pattern for an N=3 Chebyshev 0.1 dB ripple BT= 0.50 matched filter with a first-order delay equalizer (equalizer BT=0.7).

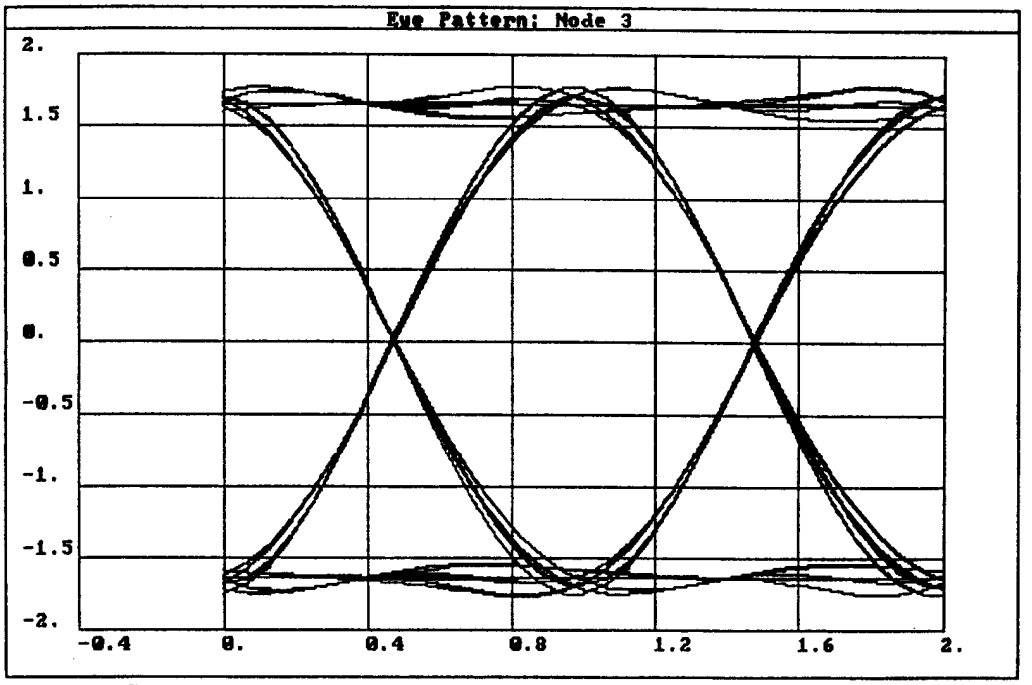


Figure 26. Bit synchronizer eye pattern for an N=3 Chebyshev 0.1 dB ripple BT= 0.55 matched filter with a first-order delay equalizer (equalizer BT=0.7).

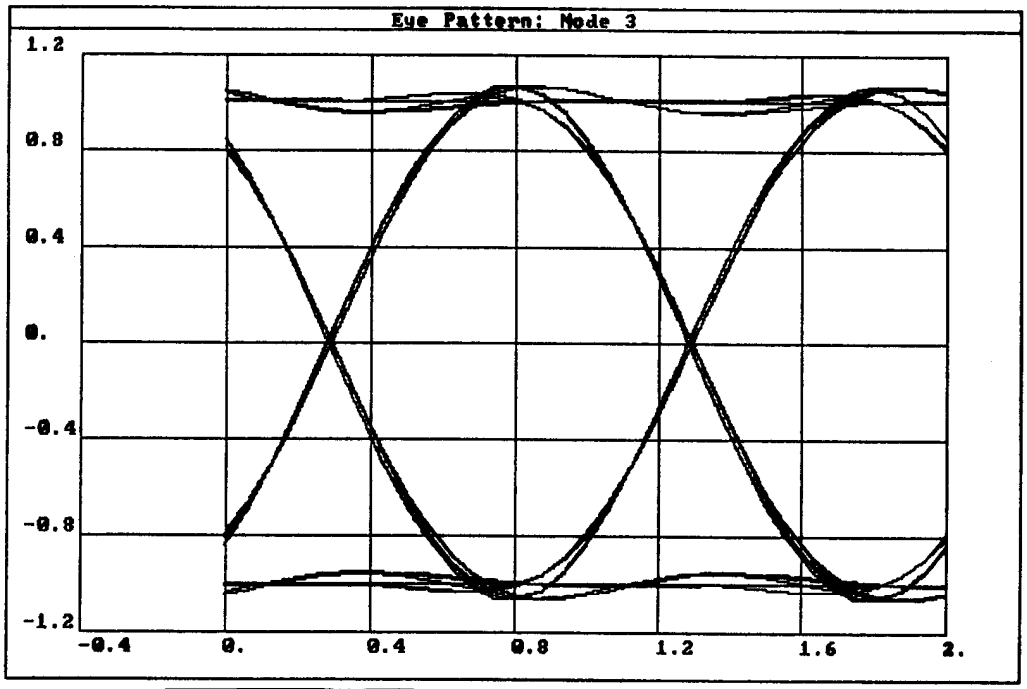


Figure 27. Bit synchronizer eye pattern for an N=3 Chebyshev 0.1 dB ripple BT= 0.65 matched filter with a first-order delay equalizer (equalizer BT=1.0).

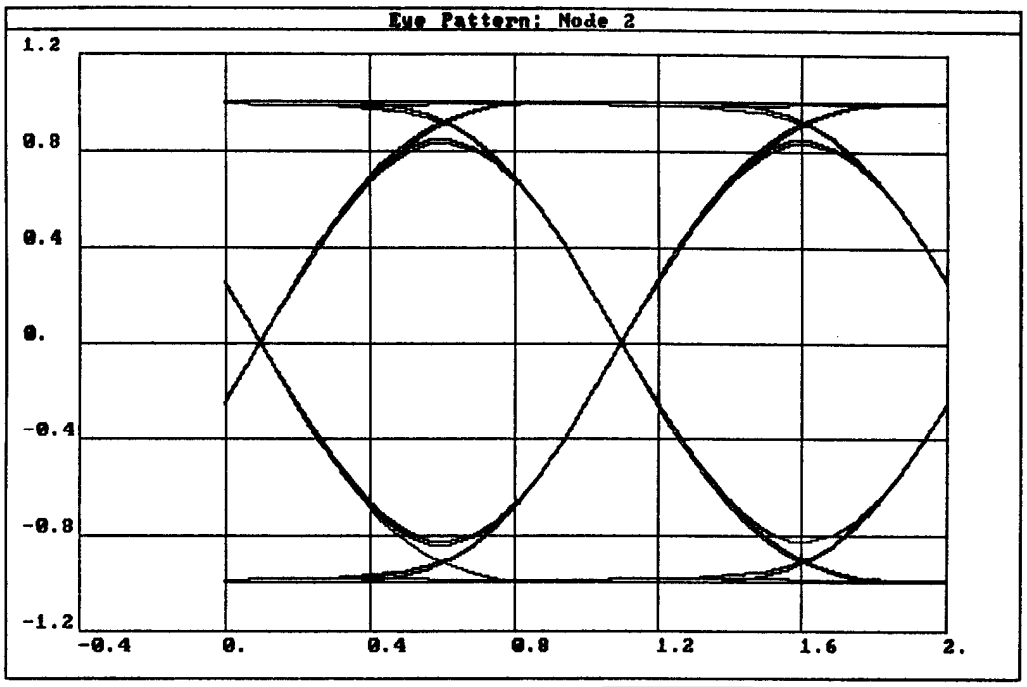


Figure 28. Bit synchronizer eye pattern for an N=3 0.5 degree Linear Phase BT= 0.60 matched filter.

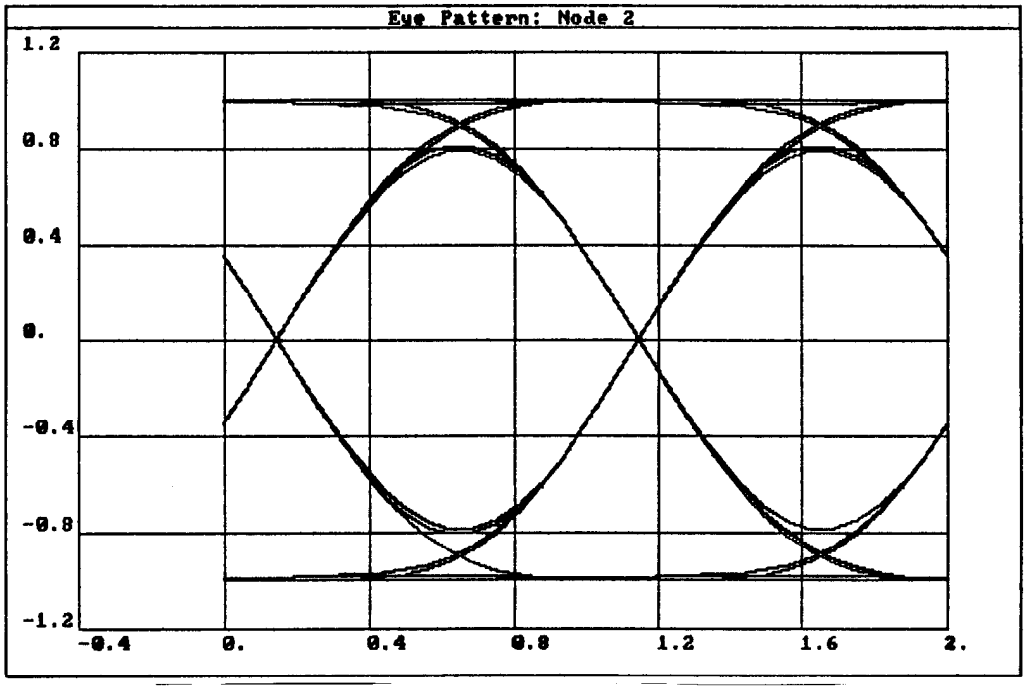


Figure 29. Bit synchronizer eye pattern for an N=3 0.5 degree Linear Phase BT= 0.55 matched filter.

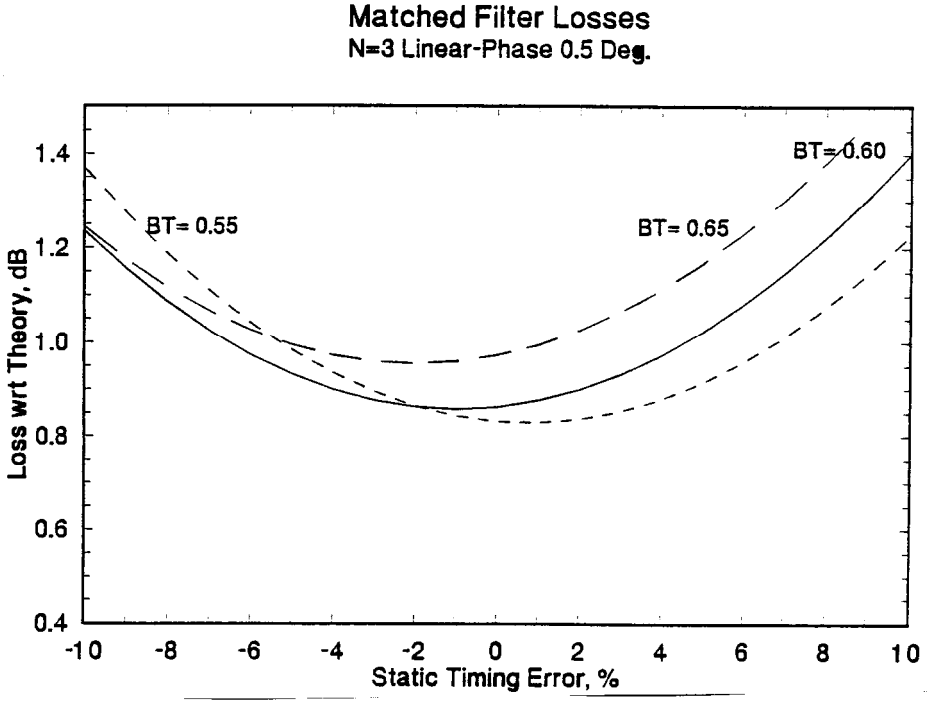


Figure 30. Bit synchronizer matched filter losses for the N=3 Linear Phase (0.5 Deg) family as a function of static clock recovery timing error.

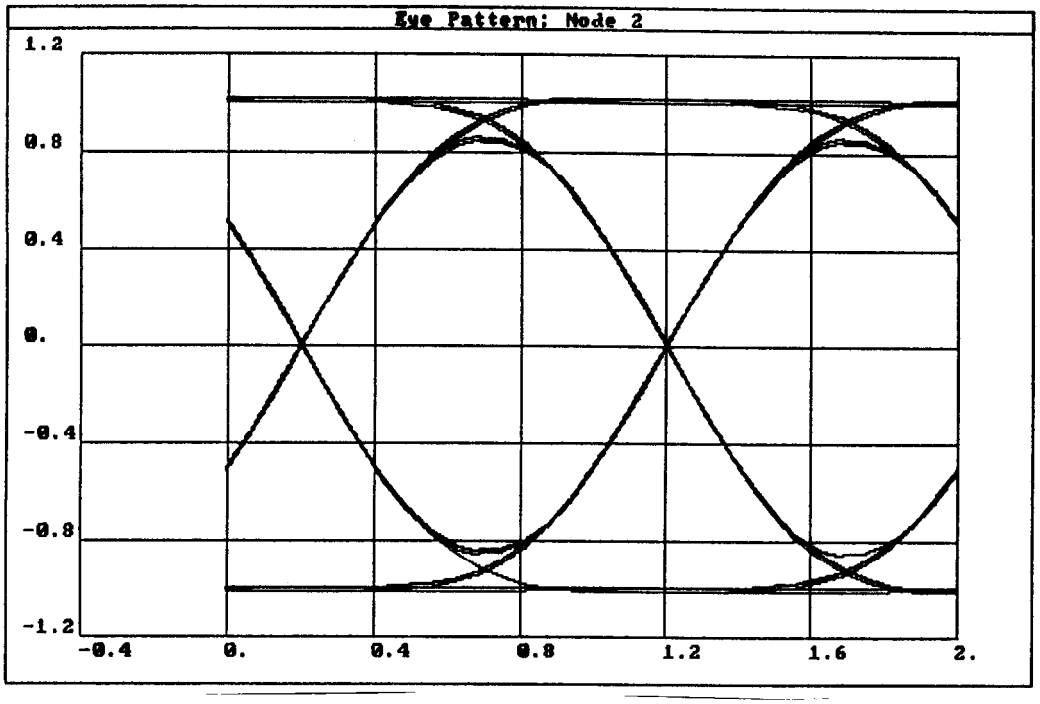


Figure 31. Bit synchronizer eye pattern for an N=4 0.5 degree Linear Phase BT= 0.60 matched filter.

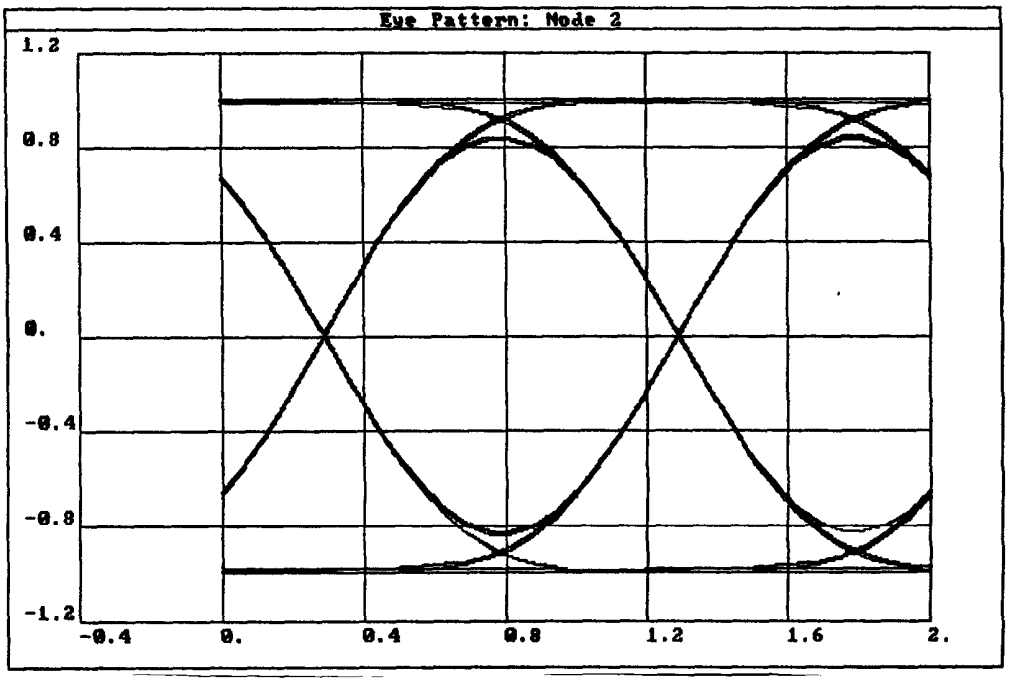


Figure 32. Bit synchronizer eye pattern for an N=5 0.5 degree Linear Phase BT= 0.60 matched filter.

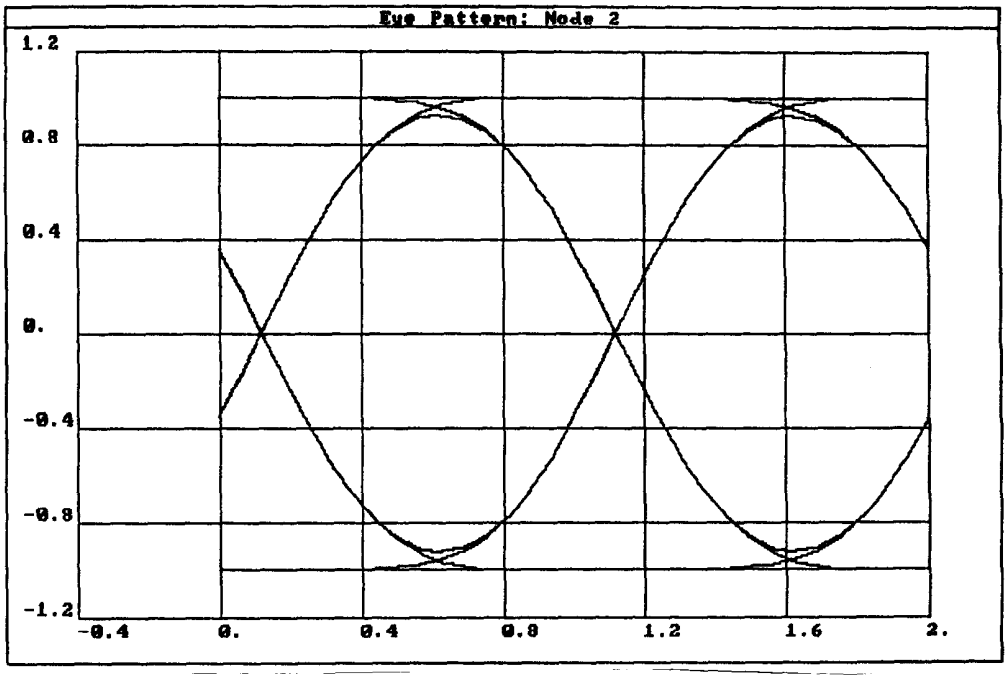


Figure 33. Bit synchronizer eye pattern for an N=6 Bessel BT= 0.80 matched filter.

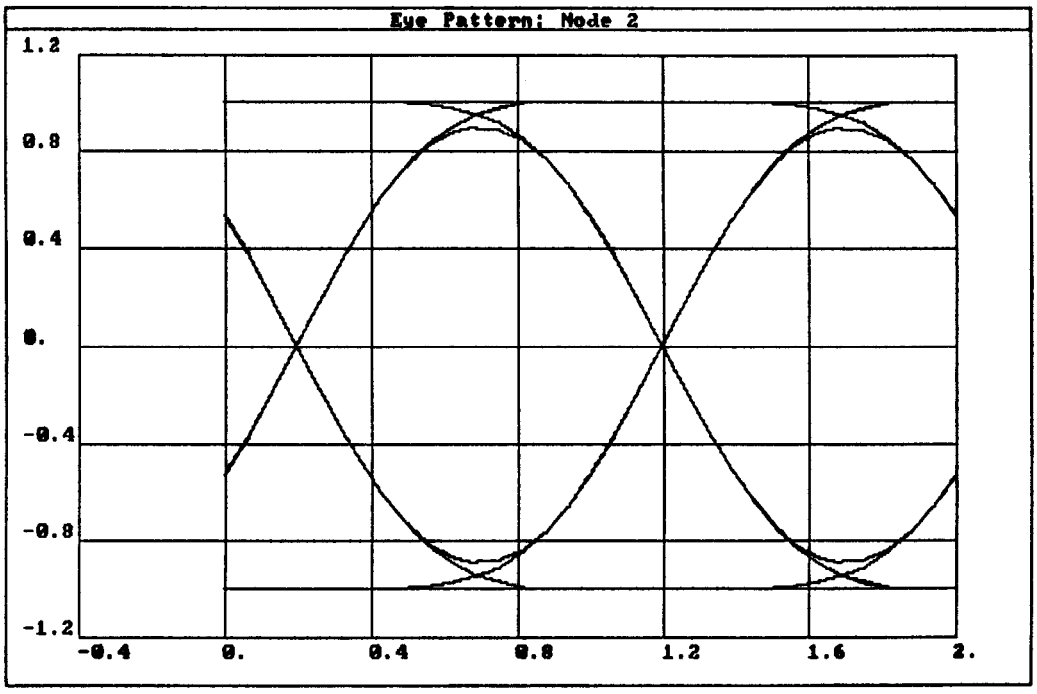


Figure 34. Bit synchronizer eye pattern for an N=6 Bessel BT= 0.70 matched filter.

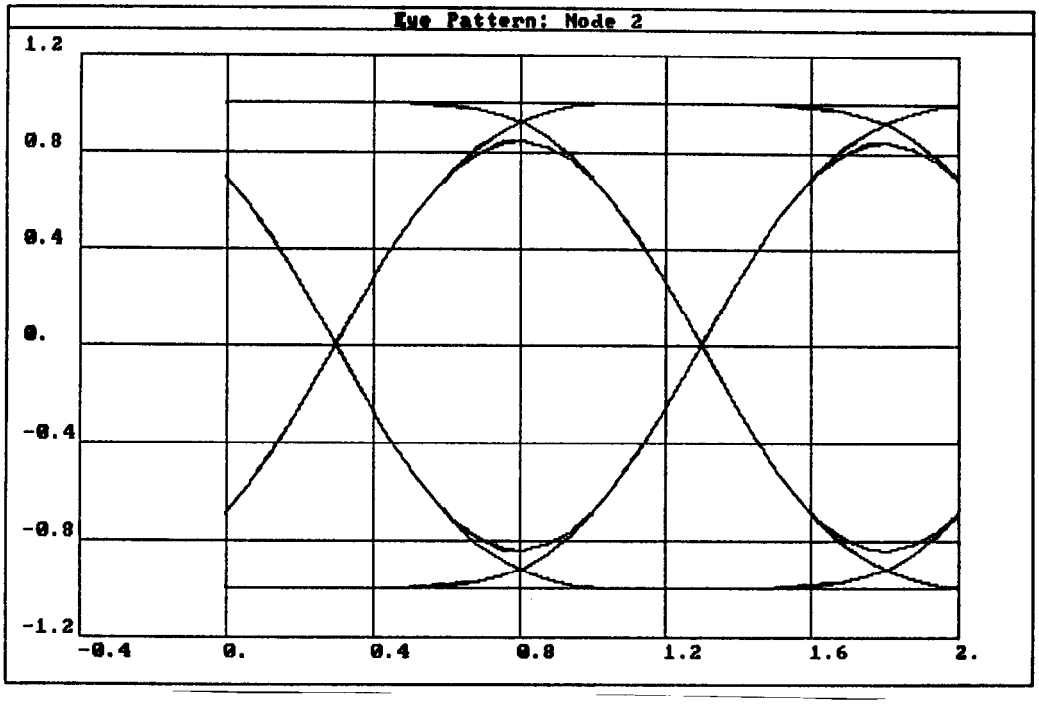


Figure 35. Bit synchronizer eye pattern for an N=6 Bessel BT= 0.60 matched filter.

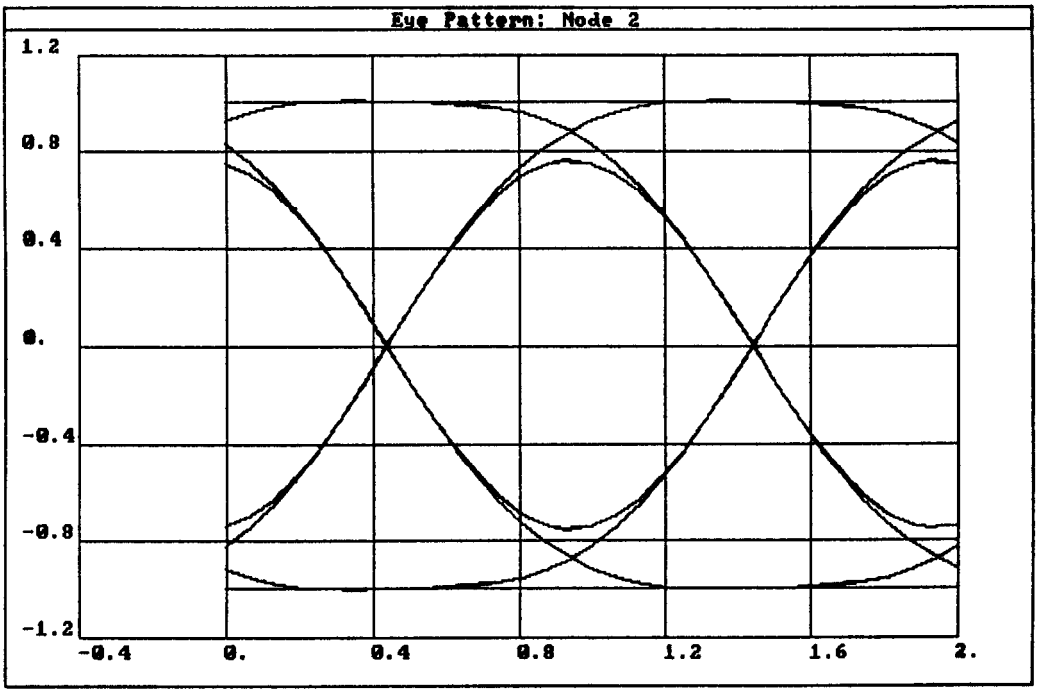


Figure 36. Bit synchronizer eye pattern for an N=6 Bessel BT= 0.50 matched filter.

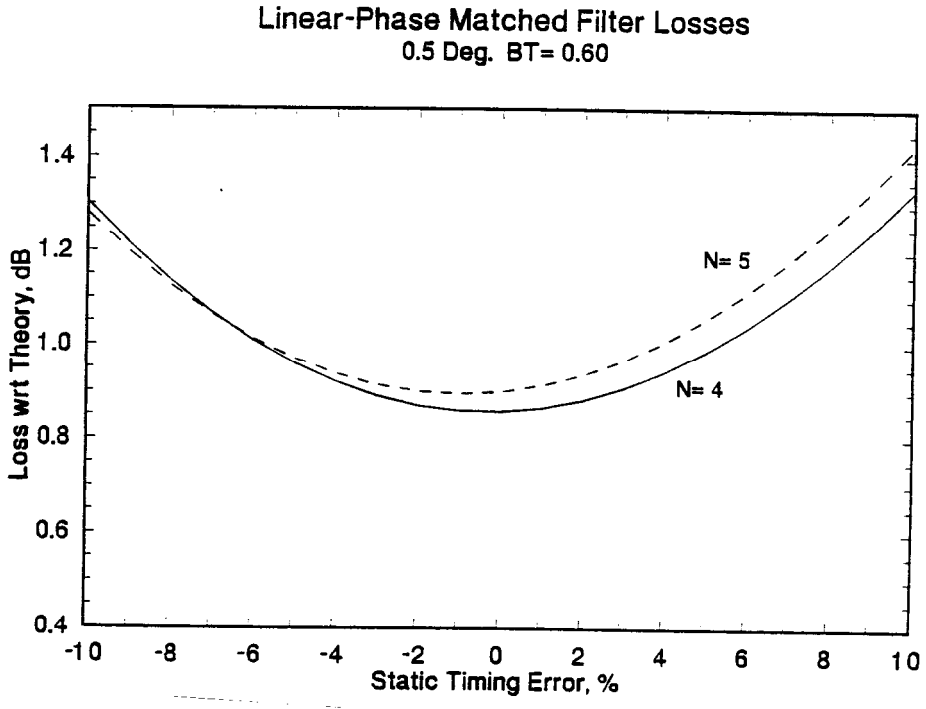


Figure 37. Bit synchronizer matched filter losses for the N=4 and N=5 Linear Phase (0.5 Deg) BT=0.60 filters as a function of static clock recovery timing error.

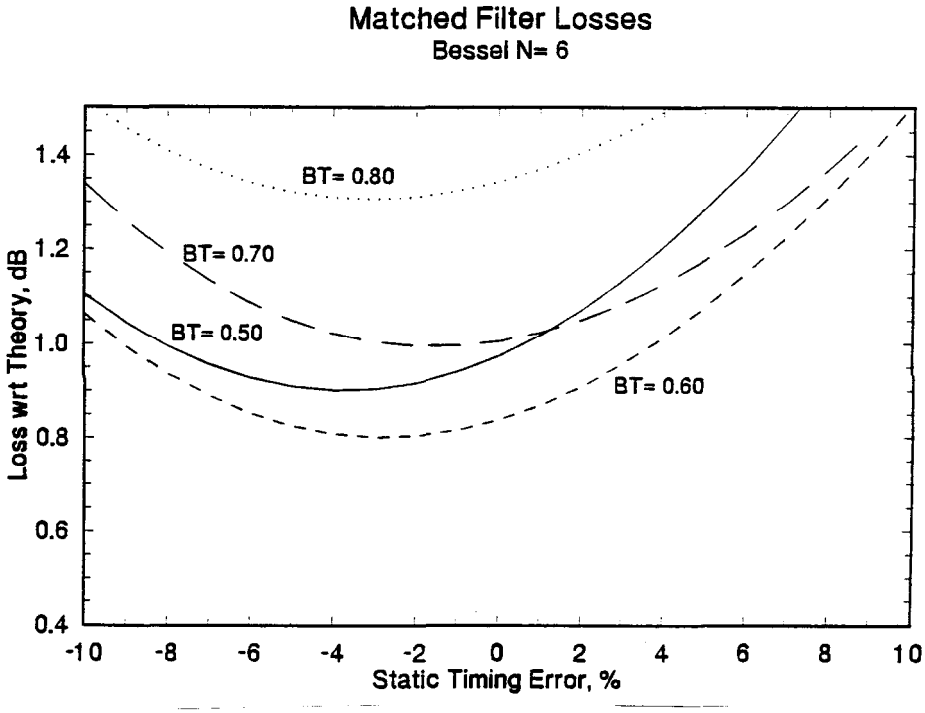


Figure 38. Bit synchronizer matched filter losses for the N=6 Bessel family as a function of static clock recovery timing error.

where p_b is the probability of an NRZ symbol (half Manchester symbol) being received in error. Although looking at both NRZ halves will help slightly at very poor p_b, in general, the bit error rate is simply that of the NRZ symbol stream implying once again a 3 dB impact to the synchronizer performance with respect to theory.

3.5 Lock Detection

The lock detection indicator is intended to be used to

1) indicate the lock/unlock condition to external devices (if present)

2) cause the synchronizer to switch from acquisition mode (wide bandwidth) to tracking mode (narrow bandwidth).

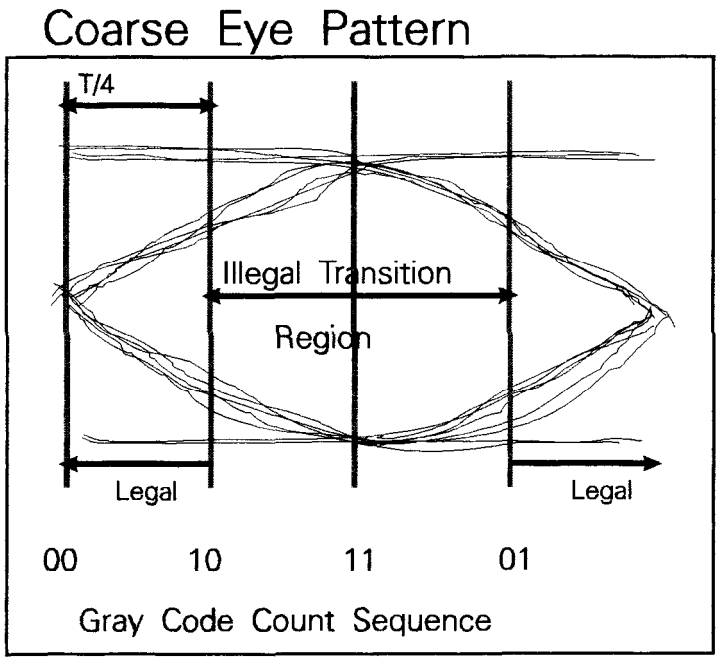
Because the switching action from acquisition to tracking mode is automatic, some hysteresis is required in the circuitry in order to guarantee smooth operation. As presented in Figure 39, the lock detector used in the Canadair bit synchronizer is based upon the following principles:

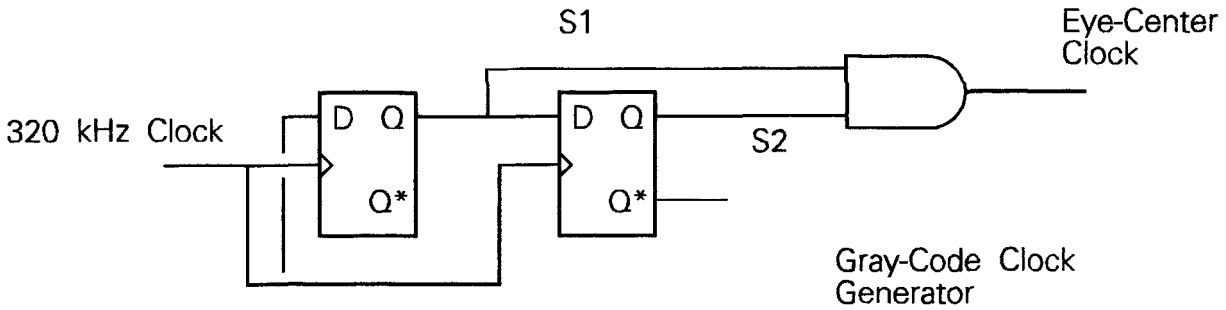
1) the number of observed legal bit transitions when averaged over a given time period must be greater than some value γ_T. The output from the lower filter in Figure 39 is proportional to the number of the valid bit transitions occuring over a time period which is given by roughly $\tau = RC$,

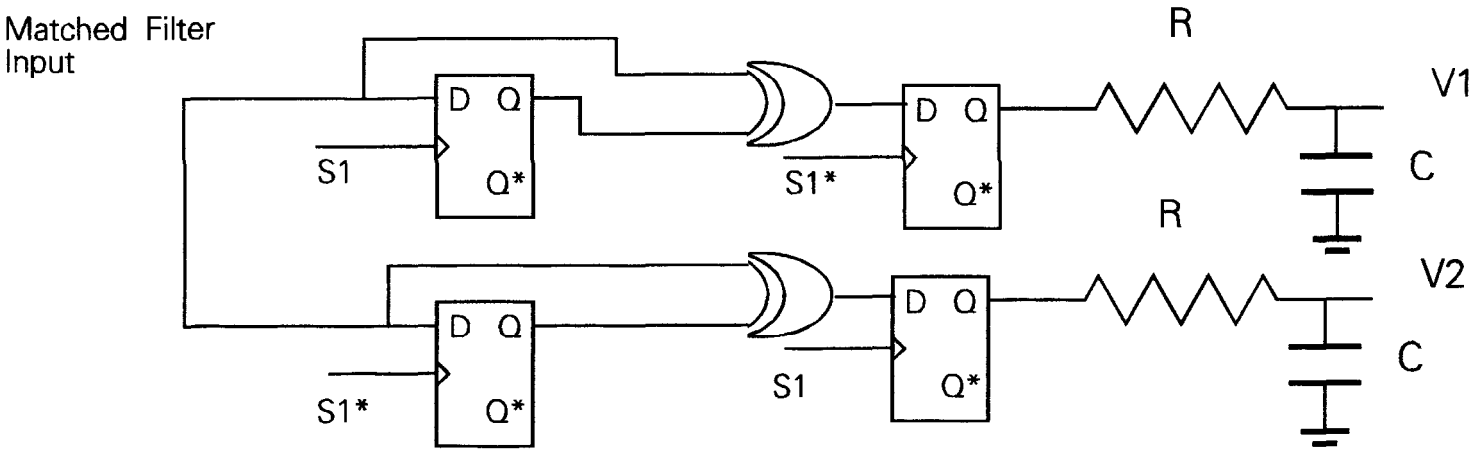
2) the number of illegal bit transitions when averaged over a given time period must be greater than some value γ_F. The output from the upper filter in Figure 39 is proportional to the number of the illegal bit transitions occuring over a time period which is given by roughly $\tau = RC$.

Ideally, γ_T, γ_F, and the two time constants are chosen to meet specified detection and false alarm probabilities. In order to simplify the analysis involved, we will focus on the 100% transition density case which is nearly equivalent to considering a sine wave in additive Gaussian noise at the matched filter output. Use of the number of legal bit transitions in a specified time interval is an insufficient indicator of synchronizer lock as we will now explore briefly. The observed signal at the bit synchronizer input may be represented by

$$x(t) = a\cos(\omega_o t) + b\sin(\omega_o t) + n(t) \qquad (51)$$







V1: Illegal Transition Detector
V2: Legal Transition Detector

Figure 39. Lock Detector Methodology for Canadair.

where a and b are independent mean-zero random Gaussian constants of variance σ^2 and n(t) is white Gaussian noise with spectral density S_o. The probability of a zero-crossing in the interval (t,t+τ) given an ideal lowpass filter with cutoff frequency ω_c (for the matched filter) is given by

$$p(\tau) = \frac{1}{\pi}\sqrt{\frac{\pi\omega_o^2\sigma^2 + S_o\omega_c^3/3}{\pi\sigma^2 + S_o\omega_c}} \qquad (52)$$

For the noise-only case,

$$p_n(\tau) = \frac{1}{\pi}\frac{\omega_c}{\sqrt{3}} \approx f_c\ 1.15 \qquad (53)$$

On the other hand, for a 1,0,1,... data pattern with no noise, the probability of a zero crossing in the interval (t,t+τ) is

$$p_s(\tau) = \frac{1}{\pi}\frac{2\pi f_c}{2} = f_c \qquad (54)$$

where a matched filter BT=0.5 was assumed. Since the ratio of p_s to p_n only varies from 1.0 to 1.15 over all possible signal to noise ratios, clearly the number of zero-crossings per unit time results at best in a very poor lock statistic. If the SNR is very high, the number of zero-crossings per unit time could be used to indicate an insufficient transition density on the incoming data stream, but this is rarely needed if a proper system design has been performed.

One of the most robust indicators of lock integrity is the location of the zero-crossings in time with respect to a fixed clock whose frequency is set to the nominal data rate. The probability density for the instantaneous phase of a sine wave immersed in additive white Gaussian noise is given by

$$p(\theta) = \frac{1}{2\pi}e^{-\rho}\left[\,1 + \sqrt{2\rho}\ e^{\rho\cos^2(\theta)}\ \cos(\theta)\ \psi(A,\theta,\sigma)\,\right] \qquad (55)$$

where

$$\psi(A,\theta,\sigma) = \int_{-\frac{A\cos(\theta)}{\sigma}}^{\infty} e^{-u^2/2}\,du \qquad (56)$$

$$\frac{A}{\sigma} = \sqrt{2\rho}$$

A	sine wave amplitude
σ^2	noise variance
ρ	signal-to-noise ratio

Several plots of $p(\theta)$ versus ρ are provided in Figures 40 through 45. As the signal-to-noise ratio becomes small, $p(\theta)$ tends toward the uniform probability density function as we would expect. From Figures 40 through 42 it is obvious that the zero crossings are tightly held to their nominal noise-free location (at zero radians) which is what we need for a reliable lock indicator function.

For best response time, the smoothing time constants would be selected differently for the acquisition and tracking modes. However, in the interest of saving board space, this was not done since we are only required to operate at fairly good E_b/N_o values. We note that the smoothing time constants must be at least on the order of several tracking loop time constants in order to prevent the circuitry from construing a saddle-point phase error trajectory as a locked condition.

Obviously, we have that

Prob{ Valid Zero Crossing | Transition Occurred } +

Prob{ Invalid Zero Crossing | Transition Occurred } = 1

for every transition. Assuming that the bit synchronizer clock is stationary during the smoothing interval due to the supposed lock condition, a sufficient lock indication can be had as

E{ Prob[Valid Crossing | Transition Present] } -

E{ Prob[Invalid Crossing | Transition Present] }

where E{} denotes time averaging. If this quantity is greater than a threshold Λ_o, lock has occurred. Using the relationship for the total probability, it suffices to consider

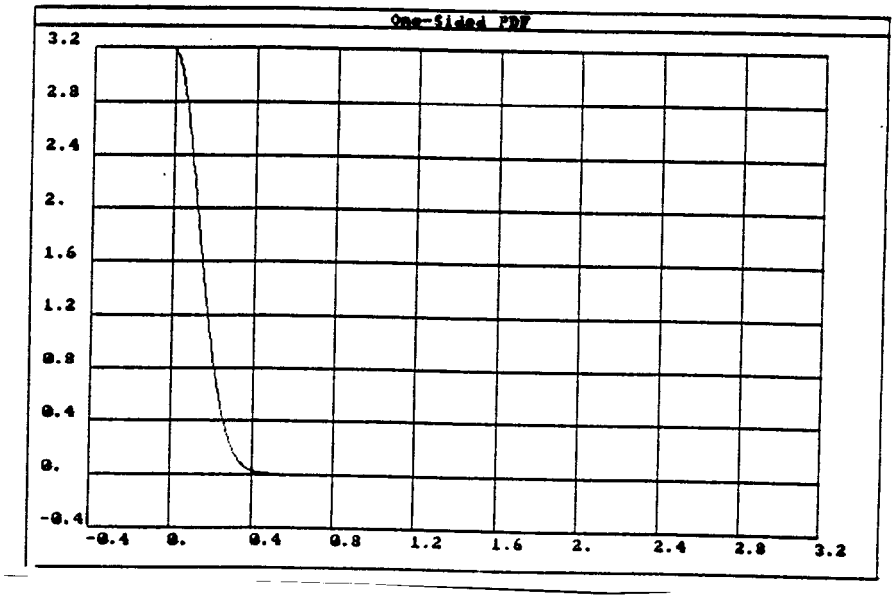


Figure 40. $p(\theta)$, θ in radians. SNR= 15 dB.

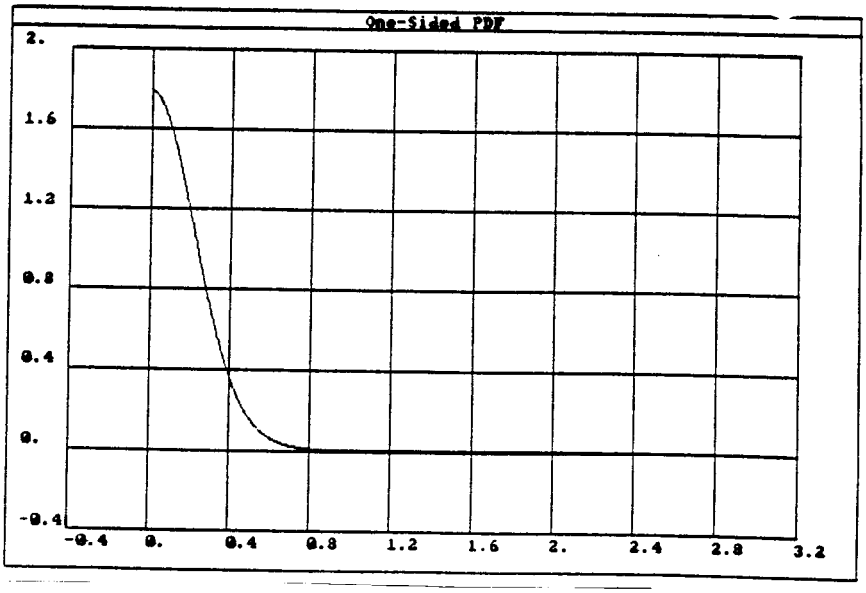


Figure 41. $p(\theta)$, θ in radians. SNR= 10 dB.

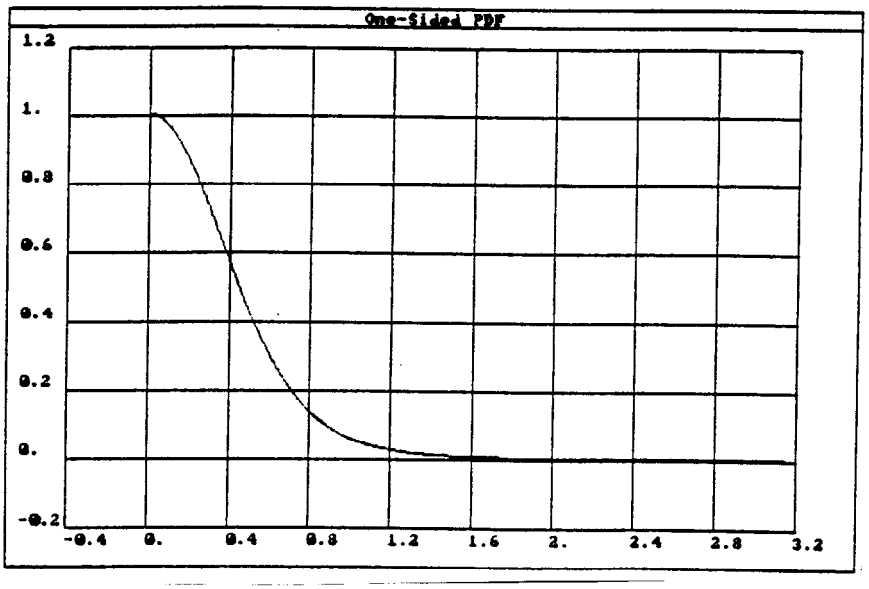


Figure 42. $p(\theta)$, θ in radians. SNR= 5 dB.

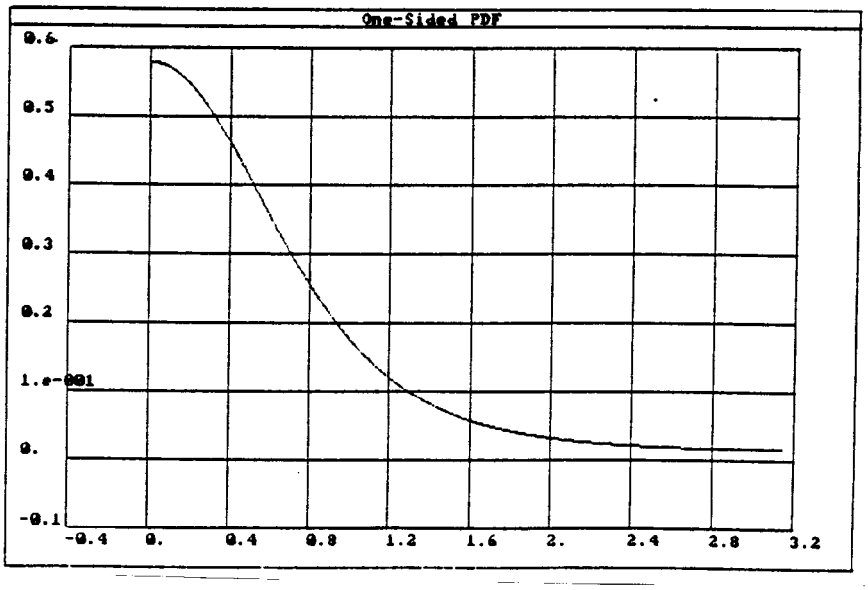


Figure 43. $p(\theta)$, θ in radians. SNR= 0 dB.

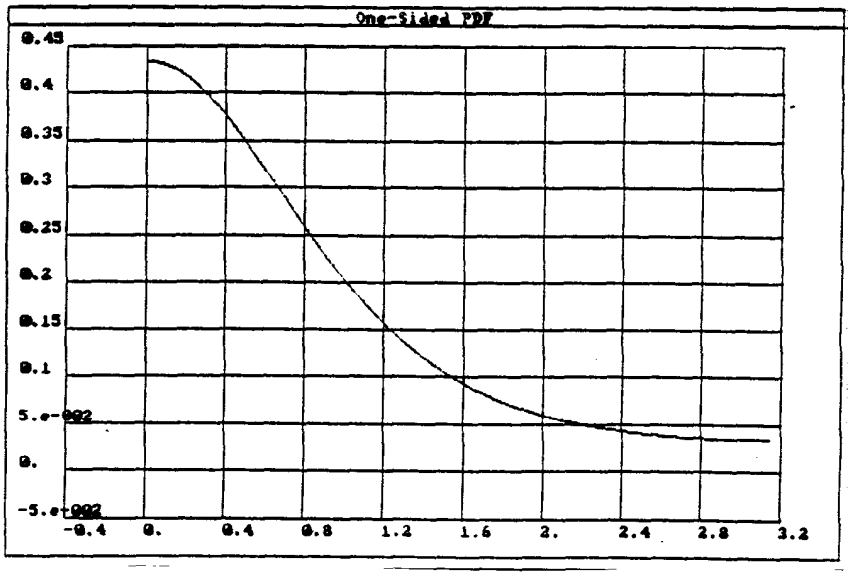


Figure 44. $p(\theta)$, θ in radians. SNR= -3 dB.

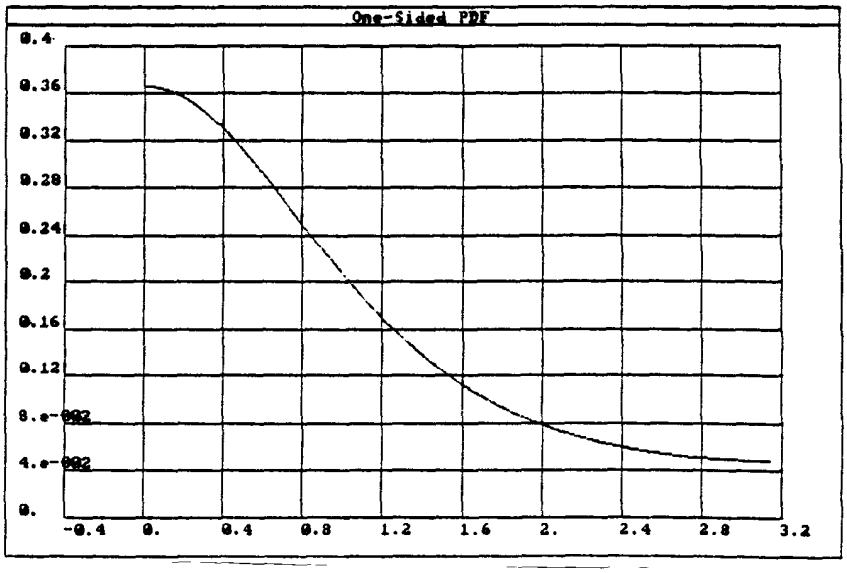


Figure 45. $p(\theta)$, θ in radians. SNR= -5 dB.

$$\mathbf{E}\{\, Prob(\, Valid\ Transition \mid Transition\ Present\,)\,\} \underset{No\ Lock}{\overset{Lock}{\gtrless}} \frac{1-\Lambda_o}{2} \qquad (57)$$

The expected probability here can be approximated by an appropriate integral of p(θ) given by (55).

If the synchronizer clock is assumed to be properly positioned in the 1,0,1,... eye pattern, the probability of a valid zero-crossing is

$$p_v = \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} p(\theta)\, d\theta \qquad (58)$$

where p(θ) is given by (55). For the noise-only case, since p(θ) becomes uniform, the probability of an illegal transition during each T-second symbol period is simply 0.5. Each symbol period may then be viewed as a discrete event where lock is declared only if Q or more of the last M observed transitions were valid. The probability of properly detecting lock on one block of M transitions is then given by

$$P_d = \sum_{i=Q}^{M} \binom{M}{i} p_v^{\,i}\, (1-p_v)^{M-i} \qquad (59)$$

For the noise-only case, the probability of erroneously declaring lock is therefore given by

$$P_f = \sum_{i=Q}^{M} \binom{M}{i} \left(\frac{1}{2}\right)^{i} \qquad (60)$$

Since we will be working with fairly large M values, these discrete probabilities (binomial distribution) may be approximated using the DeMoivre-Laplace theorm as

$$\binom{n}{k} p^{k}\, q^{n-k} \approx \frac{1}{\sqrt{2\pi npq}}\; e^{-\frac{(k-np)^2}{2npq}} \qquad (61)$$

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December 1990

Using this theorem, we obtain

$$P_d = \frac{1}{2} + erf\left(\frac{-Q+Mp_v}{\sqrt{Mp_v(1-p_v)}} \right)_{Mp_v > Q}$$

$$P_f = \frac{1}{2} - erf\left(\frac{Q-M/2}{\sqrt{M/4}} \right) \qquad (62)$$

where

$$erf(\alpha) = \int_0^{\alpha} \frac{e^{-x^2/2}}{\sqrt{2\pi}}\, dx$$

The false-alarm rate may be roughly approximated (without rigorous justification) by

$$R_f \approx \frac{P_f}{MT} \ Alarms/\text{sec} \qquad (63)$$

As stated earlier, MT must correspond to a number of tracking loop time constants in order to avoid erroneous lock indications due to saddle-points. Assuming that 4 loop time constants is adequate,

$$M \approx \frac{1}{T}\,\frac{4}{\zeta\omega_n} = \frac{4R}{\zeta\omega_n} \qquad (64)$$

In the simple lock detector context (Figure 39), we can consider the simple lowpass filters as having memory length τ= RC from which

$$M = \frac{\tau}{T} = \tau R \qquad (65)$$

which leads to

$$\tau = \frac{4}{\zeta\omega_n} \qquad (66)$$

or finally

$$\tau = 4\,\frac{\zeta+1/4\zeta}{2B_L\zeta} = \frac{2}{B_L}\left(1+\frac{1}{4\zeta^2}\right) \qquad (67)$$

For the situation at hand, B_L= 0.02 R, ζ= 1.0, and R= 80 kbps which gives τ = 0.00156 s or f_c = 102 Hz. The τ used in the final design corresponds to roughly double this value (3 msec) thinking in terms of Manchester symbols rather than NRZ symbols. The value can be easily changed as further measurements warrant by a single resistor change if desired.

> NOTE: The 3 ms τ value corresponds to 120 Manchester symbols periods. The delay could be shortened at the expense of an increased false alarm rate but this should be a non-issue for the Canadair project.

For a false-alarm rate of less than once per every 24 hours (86,400 seconds), for the noise-only case,

$$P_f \le R_f MT - R_f\,\tau \Rightarrow P_f \le 1.4\ 10^{-7} \qquad (68)$$

From (62), we have

$$P_f \approx \frac{e^{-x^2/2}}{x\sqrt{2\pi}}\Big|_{x\,-\,\frac{Q-M/2}{\sqrt{M/4}}} \qquad (69)$$

leading to x ≥ 5.2 or Q ≥ 308 for the case where M=500. Hence, if the devices in Figure 39 are CMOS operating from +5 volts, the V2 threshold for comparison would be set at roughly (308/500) 5 = 3.1 volts.

For the probability of proper lock detection, from (62) we have the following results:

p_v	γ	P_d
0.55	-2.967	0.001
0.60	-0.73	0.24
0.65	1.594	0.95
0.70	4.099	>0.999978
0.75	6.920	~1.0
0.80	10.286	~1.0

Recognizing that p_v is given by (58), casual examination of Figures 40 through 42 shows that P_d at SNRs of 5 dB should be essentially unity. In other words, explicit evaluation of (62) at different SNRs is not required to substantiate the claim that this approach should provide good detection performance.

The foregoing lock detection analysis has made use of a number of assumptions and approximations. The indication of lock can without question be asserted faster if τ is shortened as suggested, but careful measurements would be necessary to thoroughly investigate all of the possible ramifications.

4.0 Detailed Design Considerations

Time and space do not allow every aspect of the design details to be recorded in this document, but an attempt will be made to identify the most important elements of the design approach. The bit synchronizer signal interface is quite simple and is described below.

Bit Synchronizer Interface Signals (Less Power)

Inputs:

J1-8	Analog baseband positive signal input, ±1 volt maximum
J1-7	Analog baseband negative signal input, or signal return (ground), ±1 volt maximum.

Outputs:

P1-31	Open-collector lock indication. LOW = Locked
P1-60	Bit synchronizer recovered clock, 80 kHz, CMOS
P1-63	Bit synchronizer recovered data, CMOS

4.1 Matched Filter

The matched filter design is an N=4 Bessel with BT= 0.60. This was adopted rather than the N=6 Bessel in order to conserve board real estate. Device U1 functions as a unity-gain differential or single-ended buffer amplifier. The OP-42 is compensated internally for unity gain stability. In the case of a 1,0,1,... NRZ data pattern at 2 Mbps, under bandlimited conditions, the maximum input slew rate is

$$S_{max} = \omega V_p \qquad (70)$$

where V_p is the peak signal swing. If the input signal amplitude is limited to 1 volt peak, the maximum slew rate is approximately 6.28 volts/usec. This leaves substantial margin compared to the Op-42E slew rate capability which is roughly 50 V/usec at 25 C. Decoupling capacitors of 0.1 uF are used as recommended by the manufacturer.

The Bessel filter is designed using the normalized poles given below:

$-\alpha$	β
1.3596	0.4071
0.9877	1.2476

The filter topology used for the active Bessel filter was chosen with two primary factors in mind. First of all, although the unity-gain single-feedback realization has fewer resistors, the capacitor values are not the same. This could potentially lead to difficulties in realizing matched filter responses over the wide data rate range required. The configuration adopted for Canadair uses like capacitor values in the active filter. A second yet minor point is that the op-amps selected for service here do not have to be unity-gain stable.

The comparator U5 is intended to provide symmetric shaping at its output so as to not add to the self-noise level in the timing recovery circuit. Inclusion of this device all but eliminates problems with insufficient input signal level at the bit synchronizer input, and also eliminates potential problems with inadequate slew rate at very low data rates where meta-stable considerations must be addressed.

4.2 Loop Filter and Phase Detector

The Hogge phase detector is implemented within the PAL U5. The logic diagram with pin outs of the phase detector are shown in Figure 46. The actual PAL program listing is provided in Figure 47.

Although the CMOS gate stucture should help in keeping rising and falling edge assymmetry small, this will be an increasing concern wherever the bit synchronizer is used at data rates approaching 2 Mbps. These issues must necessarily be investigated for such use. (Although the Hogge topology has been used into the gigabit per second regime, implementation details cannot be taken for granted.)

Care must be exercised in selecting the RC values which immediately follow the phase detector. On one hand, the pulse slew rate is to be decreased into the op-amp by the RC filter, but on the other, loading on the PAL outputs must not be excessive. (This is really only a problem at high data rates.) In order to keep the maximum PAL output currents < 2 mA, R16 and R18 were selected to be 3.01 K. Good tolerance devices are needed in this area so as not to introduce any static tracking errors.

After considerable algebra, the combined transfer function for the Hogge phase detector and U7 circuitry is

$$P(s) = \frac{K_{do}}{2} \frac{1}{1 + s\tau_0} \qquad (71)$$

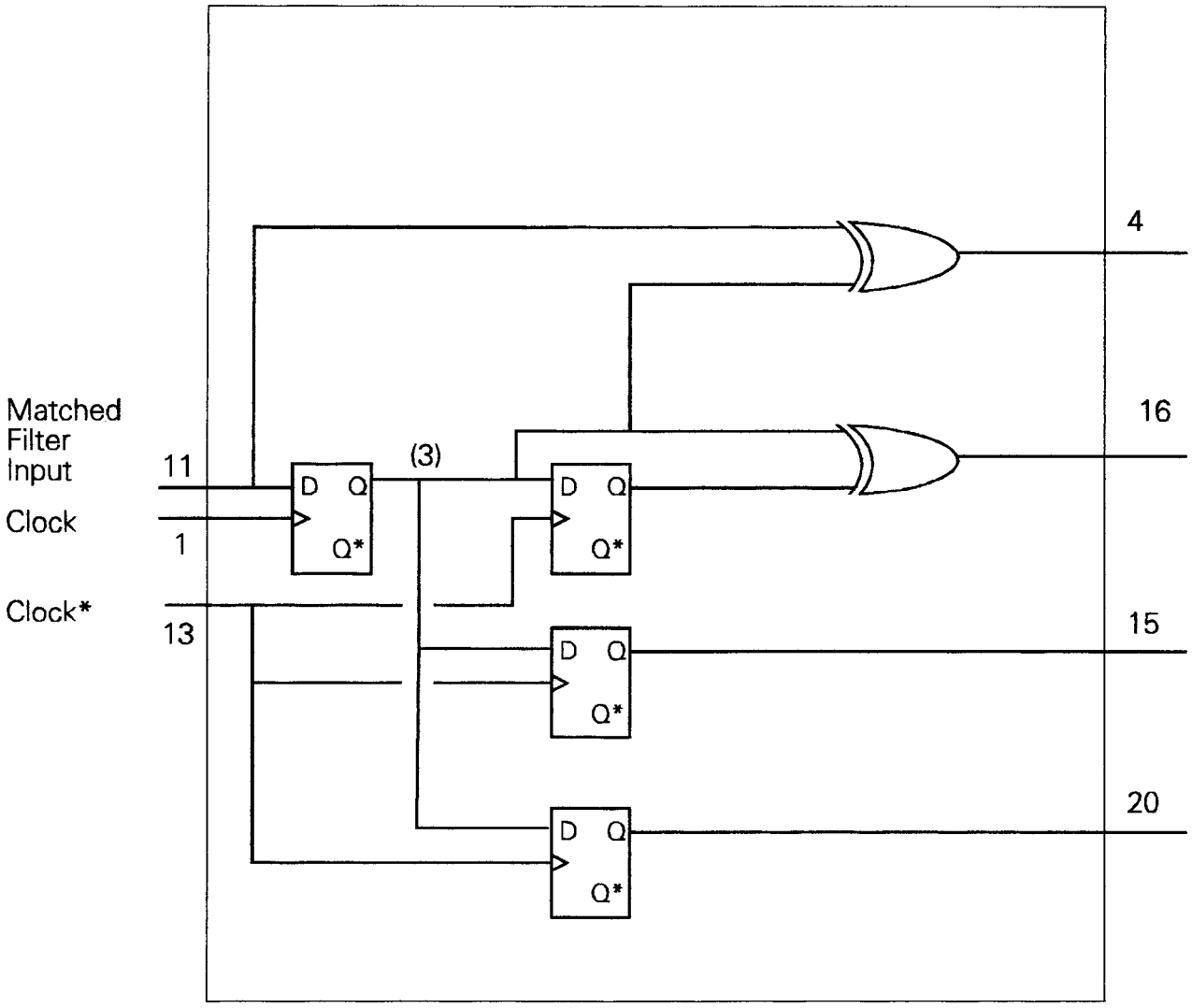

Figure 46. Internal PAL Logic Diagram.
(Hogge Phase Detector Portion Only)

```
Name            BSYNC1;
Partno          ;
Date            11/06/90;
Revision        0.1;
Designer        Robert J. Wisner;
Company         Loral Conic;
Assembly        CANADAIR BIT SYNC BREADBOARD;
Location        U?;
Device          EP600;

/*************************************************************************/
/*      PROGRAMMABLE LOGIC FOR DLP BIT SYNC                              */
/*                                                                       */
/*                                                                       */
/*************************************************************************/

/**  Inputs  **/
Pin 1           = CLOCK         ;       /* FROM PIN 8                   */

Pin 13          = CLOCKBAR      ;       /* FROM PIN 9                   */
Pin 2           = CTRIN         ;       /* FROM 7 STAGE RIPPLE COUNTER  */
Pin 11          = CMPIN         ;       /* FROM COMPARATOR              */
/* PIN 14,23 ARE SPARE INPUTS */


/**  Outputs  **/
Pin 3           = U5AQ          ;       /*                              */
Pin 4           = U6AY          ;       /*                              */
Pin 5           = S1            ;       /*                              */
Pin 6           = S1BAR         ;       /*                              */
Pin 7           = U14BQ         ;       /*                              */
Pin 8           = CLOCKOUT      ;       /* TO PIN 1                     */
Pin 9           = CLKBAROUT     ;       /* TO PIN 13                    */
Pin 10          = U8AQ          ;       /*                              */
Pin 15          = DATAOUT1      ;       /* DATA TO TEST POINT           */
Pin 16          = U6BY          ;       /*                              */
Pin 17          = !U8BQ         ;       /*                              */
Pin 18          = CLOCKOUT1     ;       /* CLOCK TO DLP BUS             */
Pin 19          = CLKBAROUT1    ;       /*                              */
Pin 20          = DATAOUT       ;       /* DATA OUT TO DLP BUS          */
Pin 21          = U5BQ          ;       /* FED BACK INTERNALLY          */
Pin 22          = SP1           ;       /* SPARE IO                     */


/** Declarations and Intermediate Variable Definitions**/
H       = 'B'1;
L       = 'B'0;
SP1 = L;
SP2 = L;
SP3 = L;
SP4 = L;
SP5 = L;

/**  Logic Equations  &=AND  #=OR  !=NOT  $=XOR  **/
S1.D = !U14BQ;
S1.CK = CTRIN;
S1BAR.D = U14BQ;
S1BAR.CK = CTRIN;
U14BQ.D = S1;
U14BQ.CK = CTRIN;
CLOCKOUT = S1 & U14BQ;
CLKBAROUT = S1BAR & !U14BQ;
CLOCKOUT1 = S1 & U14BQ;
CLKBAROUT1 = S1BAR & !U14BQ;
U5AQ.D = CMPIN;
U5BQ.D = U5AQ;
DATAOUT.D = U5AQ;
DATAOUT1.D = U5AQ;
U6AY = CMPIN $ U5AQ;
U6BY = U5AQ $ U5BQ;
U8AQ.D = CMPIN;
U8AQ.CK = S1;
U8BQ.D = CMPIN $ U8AQ;
U8BQ.CK = S1BAR;
```

Figure 47 PAL Listing

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Chip Diagram

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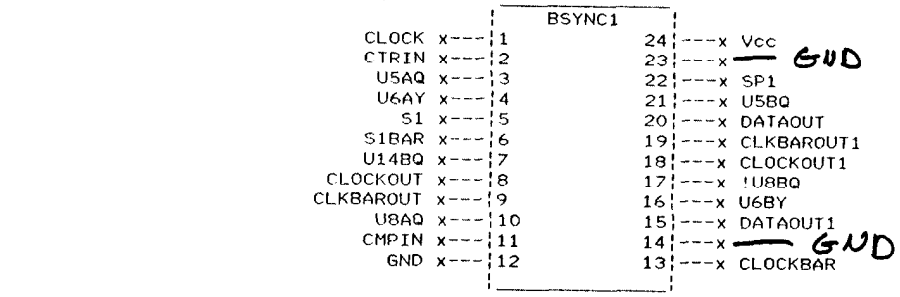

where

τ_0 $R_{18}\ C_{21} = R_{16}\ C_{21}$ etc.

K_{do} $Vcc/(2\pi) = 0.80$ volts/radian

As shown in section 5.0, the VCO sensitivity seen by the loop filter is approximately 617 Hz/volt prior to the resistive divider comprized of R_{36} and R_{37}. Including the resistive divider, the lead-lag filter sees a VCO sensitivity of only 77 Hz per volt. If a lower lead-lag filter voltage compliance range is needed, R_{37} could be increased as needed. Neglecting the 1 M resistor shunting C_{30} in the lead-lag filter, the open_loop gain function is given by

$$G_{OL}(s) = K_{d0}\eta \frac{1}{1 + s\tau_0} \frac{1 + s\tau_2}{s\tau_1} \frac{R_{37}}{R_{36}+R_{37}} \frac{1}{1 + s\tau_3} \frac{K_v}{s} \qquad (72)$$

where

η = Transition Density

τ_0 = 30.1 usec

τ_3 = 2.89 usec

K_v = 3877 rad/sec/volt

and τ_1 and τ_2 are set differently depending upon whether the synchronizer is in acquisition or tracking mode.

JFET switches are used to switch new values of τ_1 and τ_2 in for the two different modes. The source side of each JFET is at the virtual ground provided by U10A which simplifies the gating signals provided to the JFETs Q4 and Q5. Different time constants are used for the JFET gate signals in order to help insure that the switching transient which occurs between acquisition and tracking modes is minimized.

The Bode plot for the bit synchronization loop in acquisition mode is shown in Figure 48 assuming a transition density of 100%. The gain margin is in excess of 30 dB. For the 100% transition density case, the synchronizer can be equivalenced to a frequency synthesis phase-locked loop using a reference frequency of R/2 or 40 kHz. Using this equivalence, the acquisition behavior for the synchronizer in the absence of noise is shown in Figure 49 for a full 1% initial data rate error. Although the sawtooth behavior may look severe, its impact is completely negligible since even a sawtooth peak frequency deviation of 200 Hz is equivalent to roughly 20 log(200 Hz/(2 40 kHz)) = -52 dBc at most. The Bode plot for the synchronizer in tracking mode is shown in Figure 50, again assuming a transition density of 100%. An examination of the

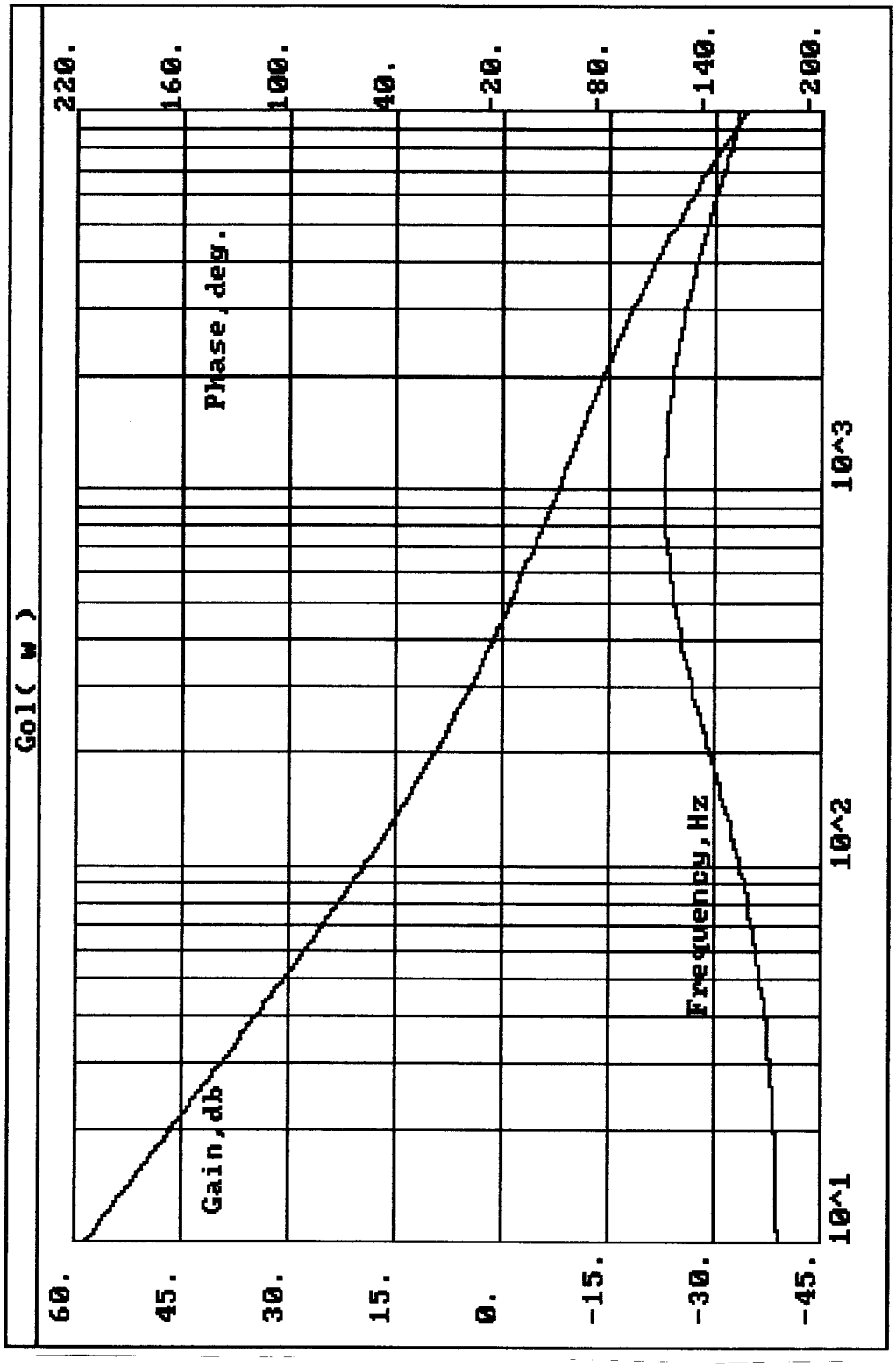

Figure 48. Open-loop gain function for the bit synchronizer in acquisition mode assuming a transition density of 100%.

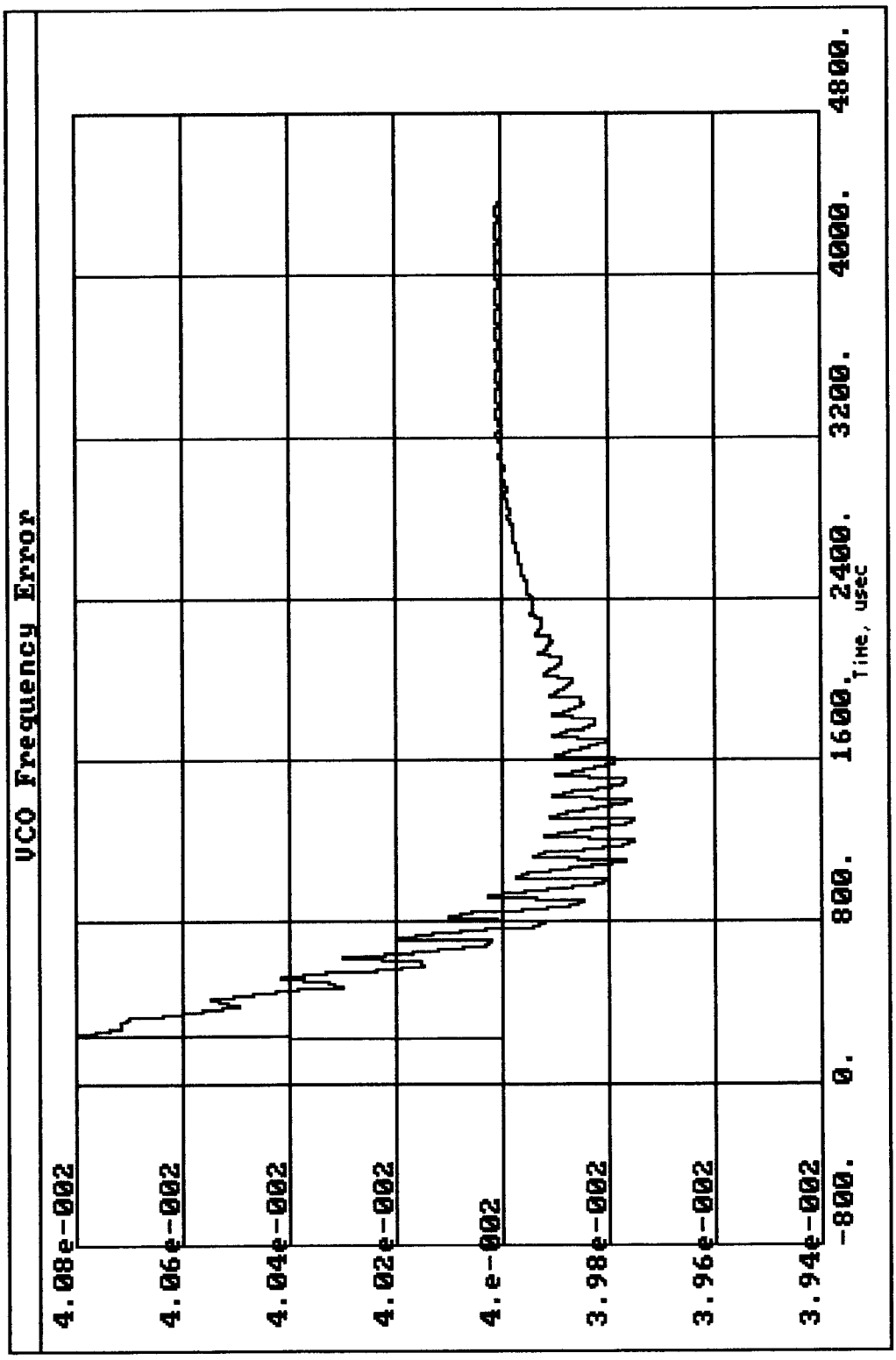

Figure 49. Step-frequency response of the bit synchronizer for a full 1% initial data rate error assuming no noise and a data transition density of 100%.

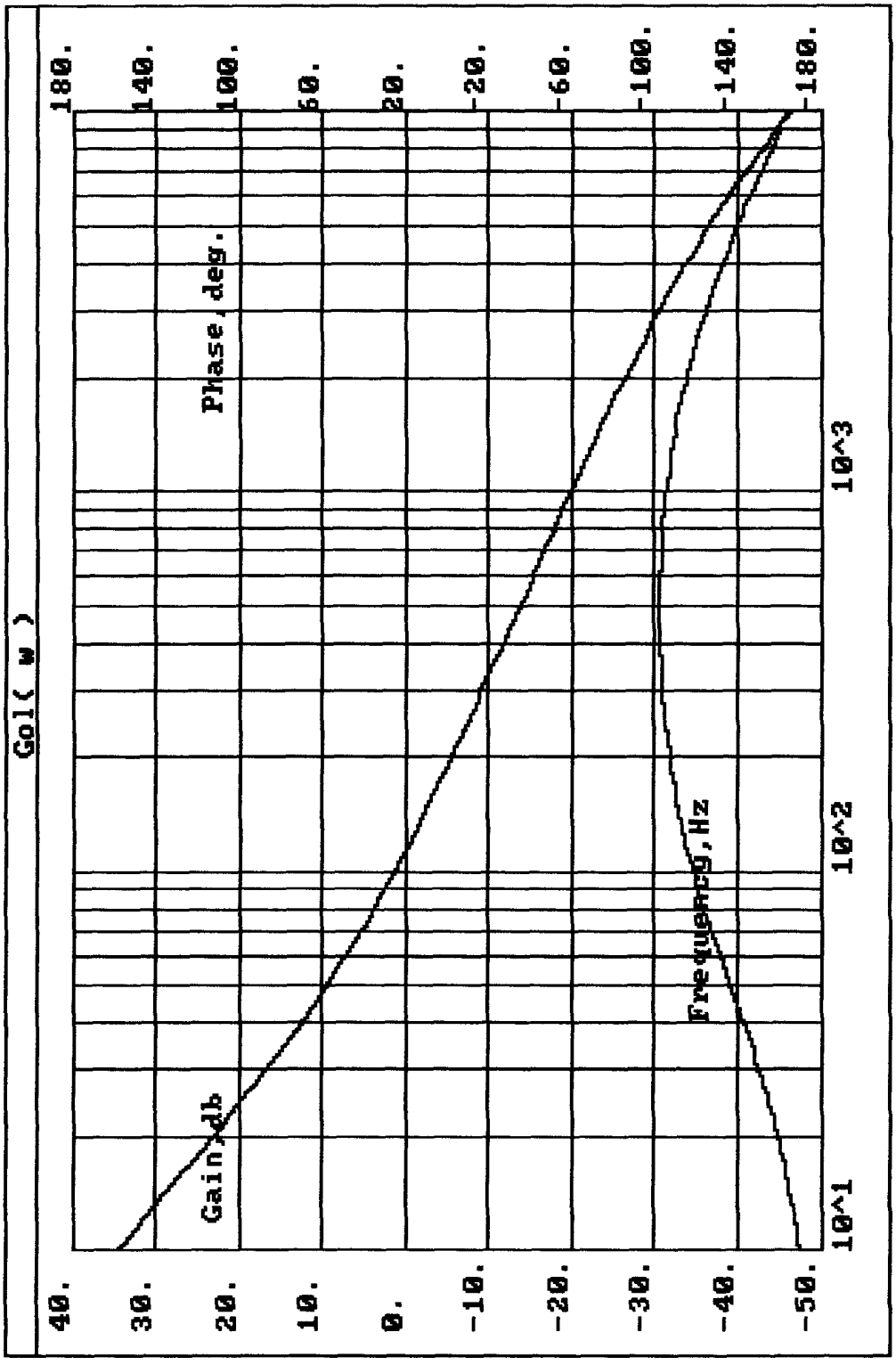

Figure 50. Open-loop gain characteristic for the bit synchronizer in tracking mode assuming a transition density of 100%.

open-loop gain plots shows that the acquisition and tracking loop bandwidths are as recommended, roughly 400 Hz and 100 Hz for the 0 dB open-loop gain points which correspond to 0.02 R and 0.005 R for the loop B_L respectively.

4.3 Voltage-Controlled Oscillator

The VCO function as mentioned earlier is a complicated design primarily due to the ±1% data rate uncertainty which it must accomodate while maintaining precise center frequency control in order to keep the required capture range small. The first step involved in designing the VCO was to arrive at a reasonable frequency plan which was relatively spurious free and which resulted in suitably relaxed requirements for the LC oscillator which was to be included. The frequency plan which was arrived at for the Canadair task utilizes a fixed crystal oscillator at 16.257 MHz and an LC oscillator which tunes from 4.02 to 4.43 MHz. This choice of frequencies results in a relatively spurious free frequency output spanning the range of 20.275 MHz to 20.685 MHz (±1% coverage). This frequency is divided by 64 and used to create a 4-phase clock whose nominal frequency is 80 kHz. The effective divide by 256 results in a spectral cleanup factor of 48 dB so any spurious components which are present at the mixer output are reduced 48 dB. Details of the mixer spurious analysis parameters are provided in Figure 51 and the actual mixer analysis results are presented in Figures 52 and 53. A generic +7 dBm LO mixer spur table was used to predict the spurious product levels. The analysis reveals that the strongest spurious product which appears is -53 dBc which in and of itself is more than adequate for bit synchronizer service. (The local oscillator leakage is expected to be on the order of -35 dBc.) This level is reduced another 48 dB by the forementioned divider action which makes the worst case predicted spur level more on the order of -101 dBc ! Mixer spurs should be the least of our concerns for Canadair. The picture will change with each data rate application. For instance, this same frequency plan could be used for a data rate of 2.56 Mbps in which case the predicted spur level would be -53 - 20 log(8)= -74 dBc. This is on the order of 30 dB better than required. These calculations assume an ideal local oscillator waveform and a sinusoidal RF waveform. The RF signal is supplied by the LC oscillator using a single-pole LC tank circuit to remove most of the oscillator harmonics. Since the mixer RF port is linear, elimination of the oscillator harmonics is needed in order to obtain the best mixer performance. The single-pole filter on the LC oscillator output reduces the harmonic outputs to a level where their contribution in the mixer output spectrum is quite negligible even without including the cleanup due to the divide-by-256 element.

The spectral purity of the crystal oscillator is not an issue since it may be considered to be essentially ideal. It is important to check the spectral purity for the LC oscillator however. The LC

Figure 51. Mixer spurious analysis parameter screen.

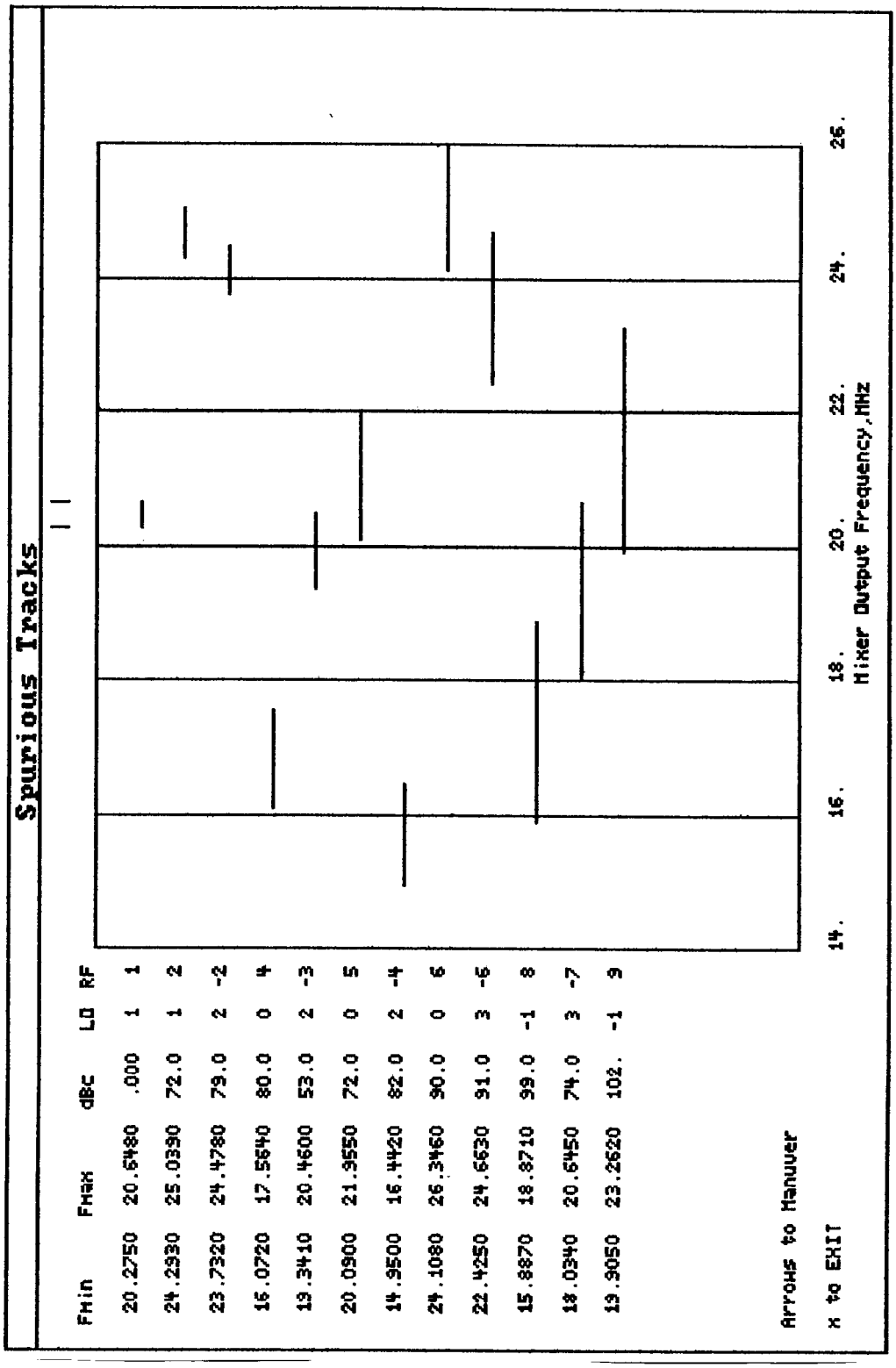

Figure 52. Far-removed mixer spurious products.

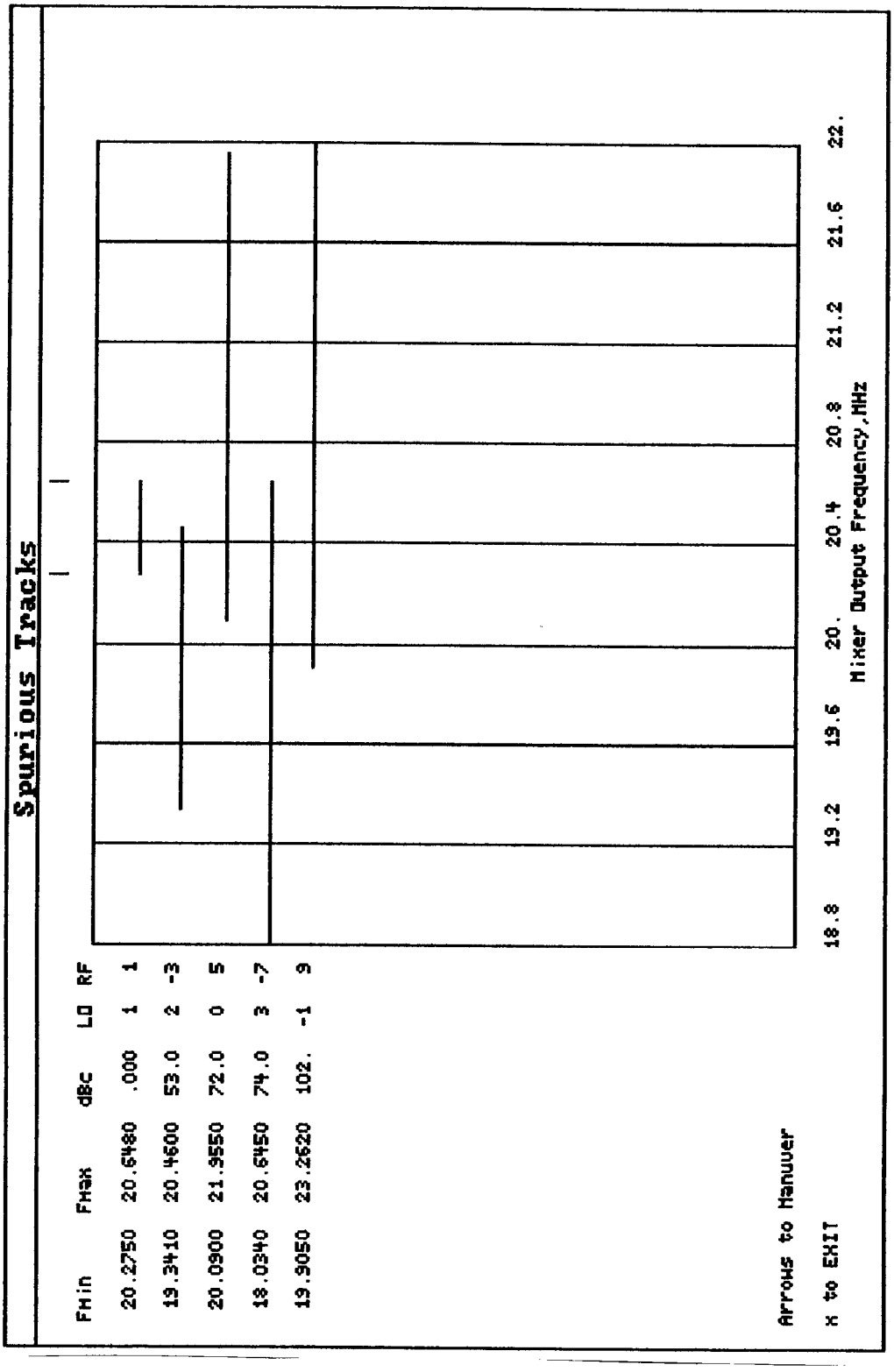

Figure 53. Close-in mixer spurious products.

oscillator design which was chosen is based upon a differential oscillator topology. The differential form provides an inherent isolation benefit and equally important, since the output limiting is well defined, the signal level control into the mixer is well controlled as well. The loaded resonator Q for the oscillator was purposely reduced in order to obtain a reasonably good sinusoidal waveform at the output. The loaded Q is only 3. Using the standard Leeson's phase noise model, the phase noise level at 1 kHz from the carrier is

$$\mathcal{L}(f) = \frac{FkT_o}{2P_o}\left[1 + \left(\frac{f_o}{2Q_L f}\right)^2\right] \qquad (73)$$

$$= -130 \ dBc/Hz$$

which is very very good. This calculation assumed a device noise figure F of 5 dB, a standard temperature of 290 C, and a resonator power level of 30 mW. The feedback capacitors which form the resonator tank were purposely chosen to provide a near linear tuning characteristic (See Appendix III) given the hyper-abrupt tuning diodes which were selected.

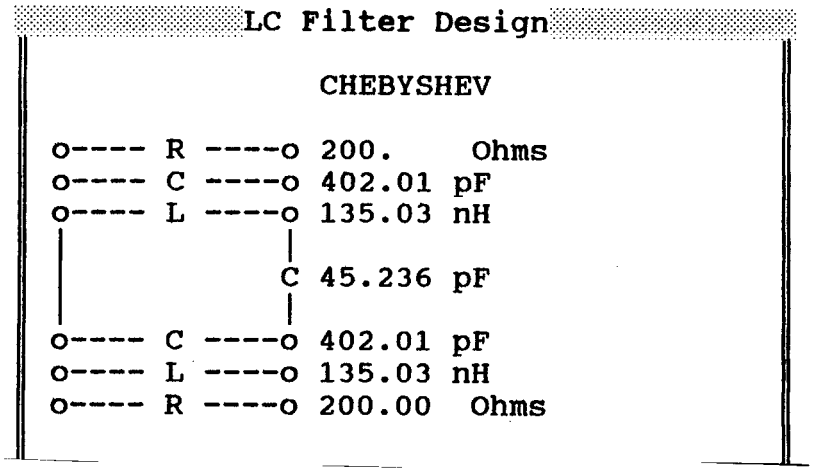

Figure 54. Baseline LC filter design.

The LC filter which follows the active mixer is primarily present to eliminate the image frequency which is roughly at 12 MHz. The image was purposely chosen to be on the low side of the carrier to make the filtering operation somewhat easier. As a result of this choice, capacitive coupling (in contrast to inductive coupling) between LC resonators led to both a simple yet improved attenuation result for the undesired image at 12 MHz. The Bartlett bisection theorem was used to change the impedance level from the mixer output (200 ohms) to the MSA input (50 ohms). Although the local oscillator leakage for the active mixer should be fairly small, the LC filter also aids in reducing this spurious component. The exact design values which were obtained are shown in Figure 54 and a frequency sweep of the filter is provided in Figure 55. This figure predicts that the LO leakage term (16.257 MHz) will be reduced approximately 22 dB by the filtering (to ≈ -35-22= -57 dBc) and the undesired image will be reduced to approximately -42 dBc prior to the additional 48 dB provided by the divide-by-256 function.

In order to provide some measure of what is an acceptable spur level, it is insightful to consider what spurious level corresponds to 1% rms jitter. Since the spurious level is given by approximately

$$Level = 20\ Log_{10}\left(\frac{\Delta\phi}{2} \right)\ dBc \qquad (74)$$

a 1% rms sinusoidal phase jitter component results in a spurious component of -27 dBc. Therefore, spurious levels on the order of the spurious predictions just developed are clearly negligible.

4.4 Lock Detector

The lock detector approach was developed in great detail in section 3.5. Some departure was made in the actual hardware implementation due to space constraints. Rather than implement both the legal transition and illegal transition threshold detectors described earlier, only the illegal transition detector is implemented. Aside from this change, the theory presented in section 3.5 remains unchanged.

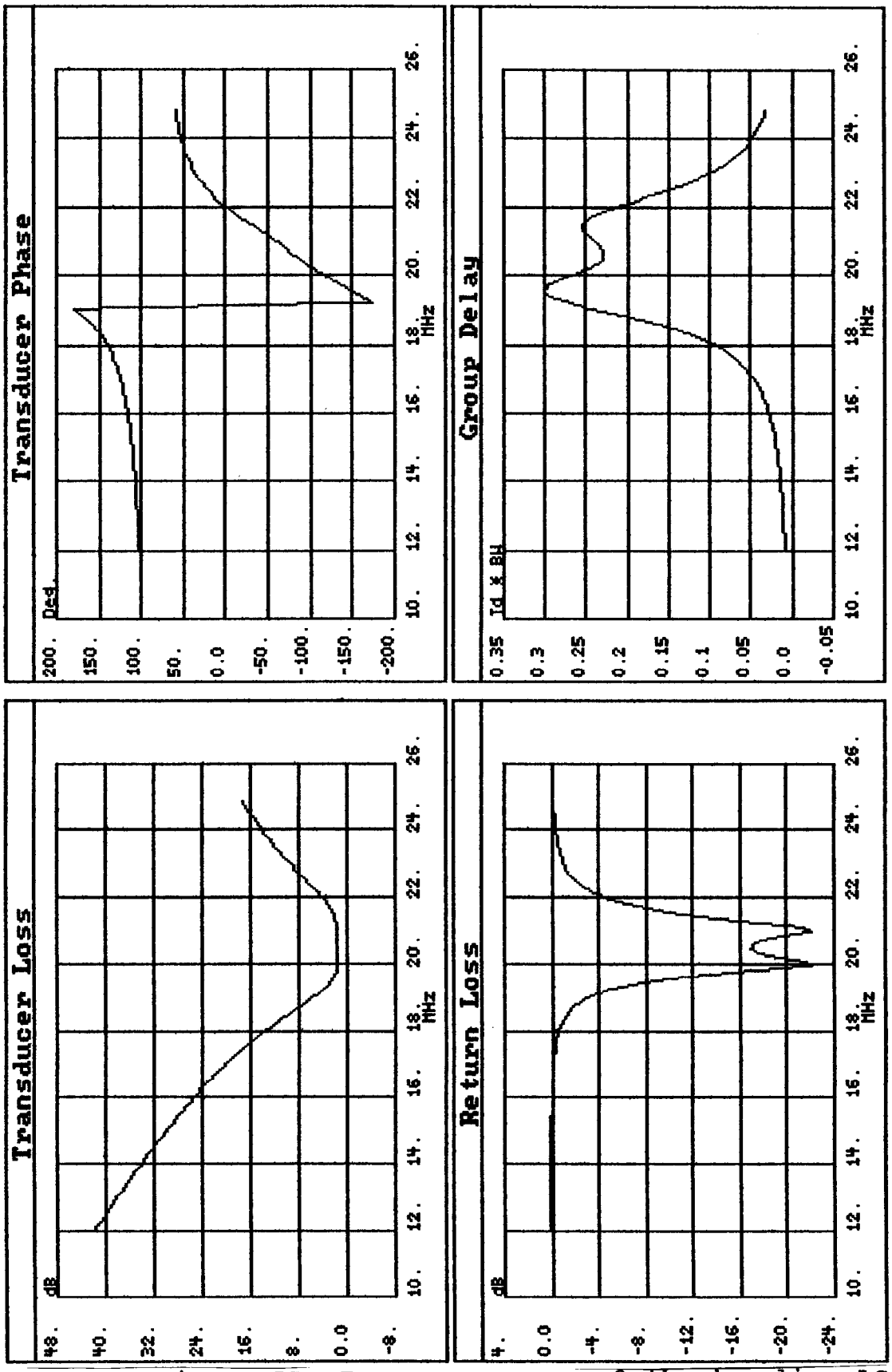

Figure 55. Frequency sweep of the baseline LC filter design.

5.0 Measured Bit Synchronizer Performance

A bit synchronizer such as the one developed for Canadair requires a large committment of time and manpower to thoroughly characterize. The data presented here should at best be considered a first examination of its true performance. Areas such as acquisition speed versus E_b/N_o and data rate anomoly were only scratched on the surface. Other areas were reasonably well examined.

None of the measurements presented are of high precision since none of the measurements were made with a calibrated white noise source. Owing to the large baseband SNR which has been promised, this should not be a problem however. At the same time, the noise spectrum which will be present at the bit synchronizer input in Canadair will be parabolic to some degree due to the FM subcarrier demodulation involved. The best evaluations of the synchronizer performance will therefore come during full system integration. It was also discovered only after the measurements had been made that one resistor value had been incorrectly calculated in the active matched filter resulting in a 3 dB corner frequency of 65 kHz rather than 48 kHz. Given that factor, some compensation for the nonwhite spectra was already included.

Although the noise sources available were not white, a good attempt was made to at least guarantee that the noise power entering our calibration lowpass filter was representative of the E_b/N_o we were attempting to emulate. Since the equivalent noise bandwidth for an n^{th}-order Butterworth lowpass filter is given by

$$B_n = \frac{f_c}{\frac{2n}{\pi}\sin\left(\frac{\pi}{2n}\right)} \quad Hz \tag{75}$$

for n=1,

$$B_n = \frac{\pi f_c}{2} \quad Hz \tag{76}$$

The noise variance at the lowpass filter output is given by

$$\sigma^2 = N_o B_n \tag{77}$$

Solving for the spectral density, we obtain

$$N_o = \frac{2\sigma^2}{\pi f_c} \; W/Hz \qquad (78)$$

Since the input data stream used was square NRZ rather than shaped NRZ, the energy per bit was simply A^2 T. Using these results, we then obtained

$$\frac{E_b}{N_o} = \left(\frac{A}{\sigma}\right)^2 \frac{\pi f_c T}{2} \qquad (79)$$

For the case at hand, A was set to 1 volt, T= $(80\ kHz)^{-1}$, and f_c was 33 kHz leading to

$$\frac{E_b}{N_o} = -20 \log(\sigma) - 1.9 \; dB \qquad (80)$$

where σ was the rms voltage value measured at the lowpass filter output.

As mentioned earlier, the input noise power spectral density was not white for the measurements which follow. The power spectral density of the noise (only) is shown in Figure 56.

The bit error performance for a nominal 80 kbps NRZ signal with no rate anomoly is shown below.

Equiv. Eb/No, dB (equ.80)	BER
6.06	3.8×10^{-3}
7.05	1.6×10^{-3}
8.05	5.1×10^{-4}
9.06	1.5×10^{-4}
10.04	3.2×10^{-5}
11.06	0.35×10^{-5}
12.03	0.10×10^{-5}

A number of measurements were made over temperature while the thermal equipment was available for our use. These results are summarized in the next few pages. In general, the performance changed very little over temperature.

A wide range of other measured data is provided in Appendix III and is fairly self-explanatory. Thermal analysis for the initial parts layout is also included in this appendix.

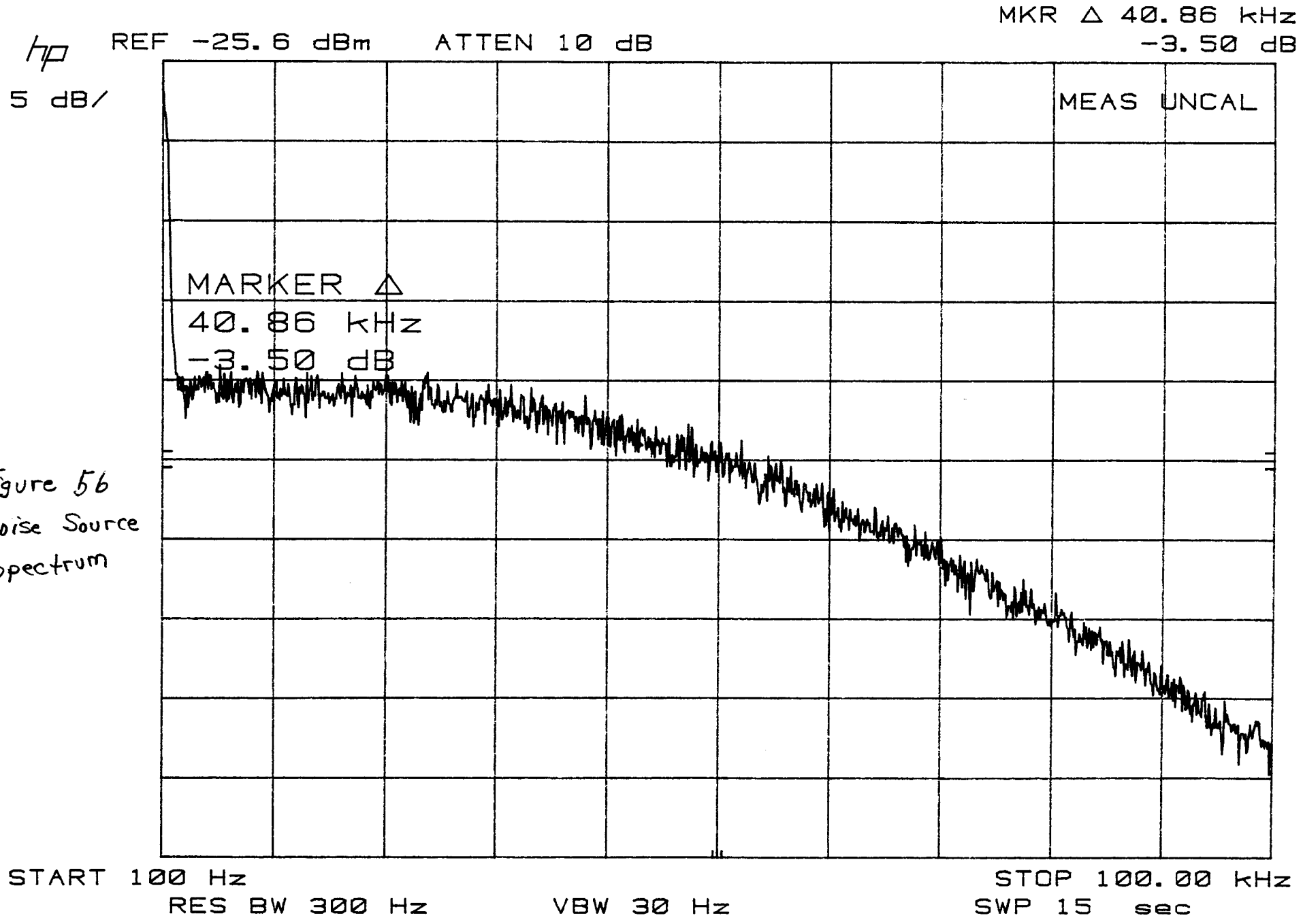

Figure 56
Noise Source
Spectrum

Temperature: +25 C
Rate: 80 kbps

SNR	Capture Range From	To	Hold Range From	To
8 dB	78.873	81.099 kbps	78.88	81.097
10	78.68	81.1	78.87	81.1
12	78.868	81.1	78.87	81.1
14	78.87	81.1	78.87	81.1

Bit Error Rate: (BER Count=10^6

SNR	@ Ro	@ Ro + 1 kbps	@ Ro - 1 kbps
8 dB	2.8×10^{-3}	2.8×10^{-3}	2.9×10^{-3}
10	3.9×10^{-4}	3.8×10^{-4}	3.9×10^{-4}
12	1.5×10^{-5}	1.5×10^{-5}	2.0×10^{-5}

//

Temperature: 0 C
Rate: 80 kbps

SNR	Capture Range From	To	Hold Range From	To
8 dB	78.853	81.250 kbps	78.88	81.25
10	78.845	81.249	78.85	81.25
12	78.843	81.251	78.84	81.25
14	78.843	81.251	78.84	81.25

Bit Error Rate: (BER Count=10^6

SNR	@ Ro	@ Ro + 1 kbps	@ Ro - 1 kbps
8 dB	3.1×10^{-3}	3.1×10^{-3}	x 10^{-3}
10	3.2×10^{-4}	3.4×10^{-4}	3.3×10^{-4}
12	2.1×10^{-5}	2.1×10^{-5}	2.1×10^{-5}

//

Temperature: -30 C
Rate: 80 kbps

SNR	Capture Range From	To	Hold Range From	To
8 dB	78.939	81.320 kbps	78.94	81.327
10	78.934	81.328	78.93	81.329
12	78.933	81.322	78.93	81.327
14	78.933	81.322	78.93	81.328

Bit Error Rate: (BER Count=10^6

	SNR	@ Ro	@ Ro + 1 kbps	@ Ro - 1 kbps
	8 dB	2.9×10^{-3}	2.7×10^{-3}	2.8×10^{-3}
	10	3.7×10^{-4}	3.7×10^{-4}	3.5×10^{-4}
**	12	1.5×10^{-5}	1.6×10^{-5}	1.5×10^{-5}

**NOTE: Data was recorded with exponents of -4. I believe this was in error based upon all the other measurements, and the fact that all of the BERs at 14 dB were 0.0×10^{-5}.

//

Temperature: 40 C
Rate: 80 kbps

SNR	Capture Range From	To	Hold Range From	To
8 dB	78.735	81.144 kbps	78.744	81.143
10	78.732	81.146	78.736	81.148
12	78.731	81.147	78.733	81.141
14	78.731	81.147	78.731	81.147

Bit Error Rate: (BER Count=10^6

SNR	@ Ro	@ Ro + 1 kbps	@ Ro - 1 kbps
8 dB	2.9×10^{-3}	2.9×10^{-3}	2.9×10^{-3}
10	3.7×10^{-4}	4.6×10^{-4}	4.0×10^{-4}
12	1.5×10^{-5}	4.9×10^{-5}	1.5×10^{-5}

//

6.0 Accomodating Other Data Rates

Time and schedule do not permit us to examine this area in appropriate depth at this time. The information provided herein should provide enough guidance to perform the needed modification for simple situations. Applications with substantially different requirements will of course require a more rigorous treatment as demonstrated in section 3.

In brief, the frequency plan for the VCO should be changed as little as possible for best results. The divide-by-N ratio should be adjusted first before modifying the frequency plan substantially. Otherwise, inductor and capacitor values in the oscillator and LC filter will more than likely change in physical size let alone introduce other performance ramifications. Note that the total divide-by-N ratio is the binary ripple counter modulo times an additional factor of four due to the 4-state Gray code counter which is used to create the four phase clock within the PAL.

More than sufficient detail is provided in the text concerning calculation of the loop parameters. The lock detector, although certainly more involved if detection and false alarm probabilities are both specified, is described in sufficient detail as well to accomodate most simple modifications.

The synthesized frequency created within the bit synchronizer is the sum of the crystal oscillator frequency and the LC oscillator frequency. (If the difference product is used rather than the sum product, this would introduce an additional -1 in the loop transfer function.) A number of criteria must be observed before these frequencies should be changed. First of all, since the LC oscillator drives the mixer's linear port, the LC oscillator frequency must be high enough such that the tuning range can be met while at the same time adequately filtering out harmonics of the oscillator before they enter the mixer. If LO leakage is a problem in the mixer, the LC oscillator frequency must also be kept high enough that the desired sum product from the mixer can be filtered from the LO term. Finally, some scrutiny of the mixer spurious performance should also be done before settling upon a particular frequency plan. Since the divide-by-N which follows the synthesis stage reduces spurious components by 20 Log(N), the largest N possible should always be used (minimum possible N is 4). The divider ratio is set in powers of two, and can be adjusted by selecting different tap outputs on the HC4024. Therefore, it is only necessary to consider frequency plans which will cover the upper octave of desired data rates (1 Mbps to 2 Mbps), all lower rates being handled by a different choice of N. A table of recommended oscillator frequencies for the upper decade of data rates is provided below.

Rate, Mbps	LC Freq, MHz	XO Freq, MHz	Range,%	N	L,dB
2.0	4.0 - 4.4	11.8	± 1.25	8	18
1.9	"	11.0	± 1.32	8	18
1.8	"	10.2	± 1.39	8	18
1.7	"	9.4	± 1.47	8	18
1.6	"	21.4	± 0.78	16	24
1.5	"	19.8	± 0.83	16	24
1.4	"	18.2	± 0.89	16	24
1.3	"	16.6	± 0.96	16	24
1.2	"	15.0	± 1.04	16	24
1.1	"	13.4	± 1.14	16	24

Recommended guidelines for oscillator frequency choices versus required data rate. The L quantity corresponds to the dBc enhancement which results from the 20 Log(N) factor.

Owing to the divide-by-N, the spurious performance at the filtered mixer output does not have to be very good in order to still have excellent bit synchronizer performance even at the 2 Mbps maximum rate. Normally, a 3% RMS jitter requirement is quite adequate for a single bit synchronizer unless systematic jitter and/or ranging type requirements are imposed. If we assume that the jitter due to possible spurious components may be at most 1% RMS, a single spurious component may be as strong as -27 dBc at the divided down output, or L dB greater at the filtered mixer output. Since L is a minimum of 18 dB, mixer spurious performance should not be a major concern. If the mixer output spurious components after filtering are kept at a maximum of -25 dBc, the maximum clock jitter which can result will be at -25 -18 = -43 dBc which is equivalent to only 0.16 % RMS.

7.0 Schematics and Parts List

Schematics, parts list, and assembly drawings follow.

8.0 Alignment Procedures

Following a basic test for electrical integrity, the first alignment step must be calibration of the VCO center frequency. The most straight-forward approach is to lift the U10A end of R_{36} and apply a ground potential to it. Then, by select-and-test, modify resistor R_{34} until the nominal clock rate out of the Gray code counter is 80 kHz ±100 Hz. Once this step has been completed, R_{36} should be put back in place. This should be the only alignment step required to bring the bit synchronizer to life.

Appendix I Computing Synchronizer Loop SNR

In this appendix, equations (9) and (10) of the main text will be derived assuming a repeating 1,0,1,... NRZ data pattern. Once the incoming baseband signal has passed through the matched filter, we will assume that it may be represented by

$$x(t) = A\cos(\omega_o t) + n(t) \tag{81}$$

where n(t) represents the Gaussian noise component out of the matched filter which is no longer white. It will nonetheless be assumed to be flat across the effective bandwidth of the tracking loop which is assumed to be much smaller than 1/(2T) Hertz. The noise is assumed to be bandpass in nature, centered at f_o, having a bandwidth of B Hz. The noise may be represented as

$$n(t) = n_c(t)\cos(\omega_o t) - n_s(t)\sin(\omega_o t) \tag{82}$$

Assuming that the noise is wide-sense stationary, we may compute the autocorrelation of the noise as

$$R_n(\tau) = \mathbf{E}\left[n_c(t)\cos(\omega_o t) - n_s(t)\sin(\omega_o t) \right] \left[n_c(t-\tau)\cos(\omega_o(t-\tau)) - n_s(t-\tau)\sin(\omega_o(t-\tau)) \right] \tag{83}$$

where E represents statistical expectation. Assuming a symmetrical spectrum for the noise, this becomes

$$R_n(\tau) = \frac{1}{2}\left[R_{n_c}(\tau) + R_{n_s}(\tau) \right]\cos(\omega_o \tau) \tag{84}$$

which simplifies to

$$R_n(\tau) = R_{n_c}(\tau)\cos(\omega_o \tau) \tag{85}$$

Employing the Wiener-Khinchin theorem, the power spectral density of the noise is given by

$$S_n(\omega) = \int_{-\infty}^{\infty} R_n(\tau)\, e^{-j\omega\tau} d\tau$$
$$= \frac{1}{2}\left[\psi(-\omega_o+\omega) + \psi(-\omega_o-\omega) \right] \qquad (86)$$

where

$$\psi(\omega) = \int_{-\infty}^{\infty} R_{n_c}(\tau)\, e^{-j\omega\tau} d\tau \qquad (87)$$

Therefore, if the original noise spectrum had a one-sided power spectral density of N_o watts/Hz,

$$\psi(\omega) = N_o \qquad for \ |\omega| < \frac{B}{2}\, 2\pi \qquad (88)$$

This is clearly a two-sided power spectral density.

Shifting now to consideration of the phase detector within the tracking loop, we will assume that it is a multiplicative type phase detector. In this case, the phase detector output may be represented as

$$v(t) = K_d \left[A \cos(\omega_i t+\phi_i) + n(t) \right] \sin(\omega_o t+\phi_o) \qquad (89)$$

where ω_o is the radian frequency of the loop VCO and φ_o is its phase. If we take the two radian frequencies and two phase angles as equal in tracking mode, and define a new phase detector gain given by K_d A, the resulting additive noise term of interest at the phase detector output is given by

$$n'(t) = \frac{n_c(t)\, \sin(\phi_o) - n_s(t)\, \cos(\phi_o)}{A} \quad rad \qquad (90)$$

The autocorrelation of n′ is given by

$$R_{n'}(\tau) = \frac{R_{n_c}(\tau)}{A^2} \tag{91}$$

which leads to a power spectral density for the noise at the phase detector output of

$$S_{n'}(f) = \frac{S_{n_c}(f)}{A^2} = \frac{\Psi(\omega)}{A^2} = \frac{N_o}{A^2} \tag{92}$$

for $|f| \leq B/2$ once more. The one-sided power spectral density for the additive noise at the phase detector output is therefore given by

$$\frac{2N_o}{A^2} \quad for \quad 0 \leq f \leq \frac{B}{2} \tag{93}$$

Assuming a linearized phase detector, the phase error variance within the tracking loop bandwidth is given by

$$\sigma_\theta^2 = \frac{2N_o B_L}{A^2} \; rad^2 \tag{94}$$

The signal-to-noise ratio within the tracking loop bandwidth is then given by

$$\rho = \frac{A^2/2}{2B_L N_o} = \frac{1}{2\sigma_\theta^2} \tag{95}$$

Appendix II VCO Phase Noise Relationships

In this appendix, we will derive the basic relationship between the phase noise spectrum $S_\theta(f)$ and the measured quantity $\mathcal{L}(f)$. Consider the real voltage waveform at the oscillator output represented by

$$v(t) = Re\left[e^{j\omega_o t}\, e^{j\theta(t)} \right] \tag{96}$$

where ω_o is the oscillator radian frequency and $\theta(t)$ is assumed to be a wide-sense stationary random noise process. The noise voltage autocorrelation function is given by

$$R_v(\tau) = \frac{1}{2} Re\left\{ e^{j\omega_o \tau}\, \mathbf{E}\left[e^{j[\,\theta(t) - \theta(t-\tau)\,]} \right] \right\} \tag{97}$$

Taking the expectation, we finally obtain

$$\begin{aligned} R_v(\tau) &= \frac{1}{2}\cos(\omega_o\tau)\ \mathbf{E}\{\cos[\,\theta(t)-\theta(t-\tau)\,]\} \\ &\approx \frac{1}{2}\cos(\omega_o\tau)\ \mathbf{E}\left(1 - \frac{[\theta(t)-\theta(t-\tau)]^2}{2}\right) \\ &= \frac{1}{2}\cos(\omega_o\tau)\,[\,1 - R_\theta(0)\,] + \frac{1}{2}\cos(\omega_o\tau)\ R_\theta(\tau) \end{aligned} \tag{98}$$

Employing the Wiener-Khinchin theorem, this leads to a power spectral density of

$$\begin{aligned} S_v(f) &= \frac{1-R_\theta(0)}{4}[\,\delta(\omega-\omega_o) + \delta(\omega+\omega_o)\,] \\ &\quad + \frac{1}{4}S_\theta(\omega-\omega_o) + \frac{1}{4}S_\theta(\omega+\omega_o) \end{aligned} \tag{99}$$

$S_v(f)$ and $S_\theta(f)$ are clearly both two-sided spectra. The spectrum which we measure on a spectrum analyzer is one-sided and is given by

$$\mathcal{L}(f) = 2\, S_v(f) - \frac{1-R_\theta(0)}{2}\,\delta(\omega-\omega_o) + \frac{1}{2}S_\theta(\omega-\omega_o) \qquad (100)$$

Aside from the delta function term, we have (22) given in the main text.

End result (100) is off by a factor of 2 because (96) should have had an additional factor of $\sqrt{2}$.