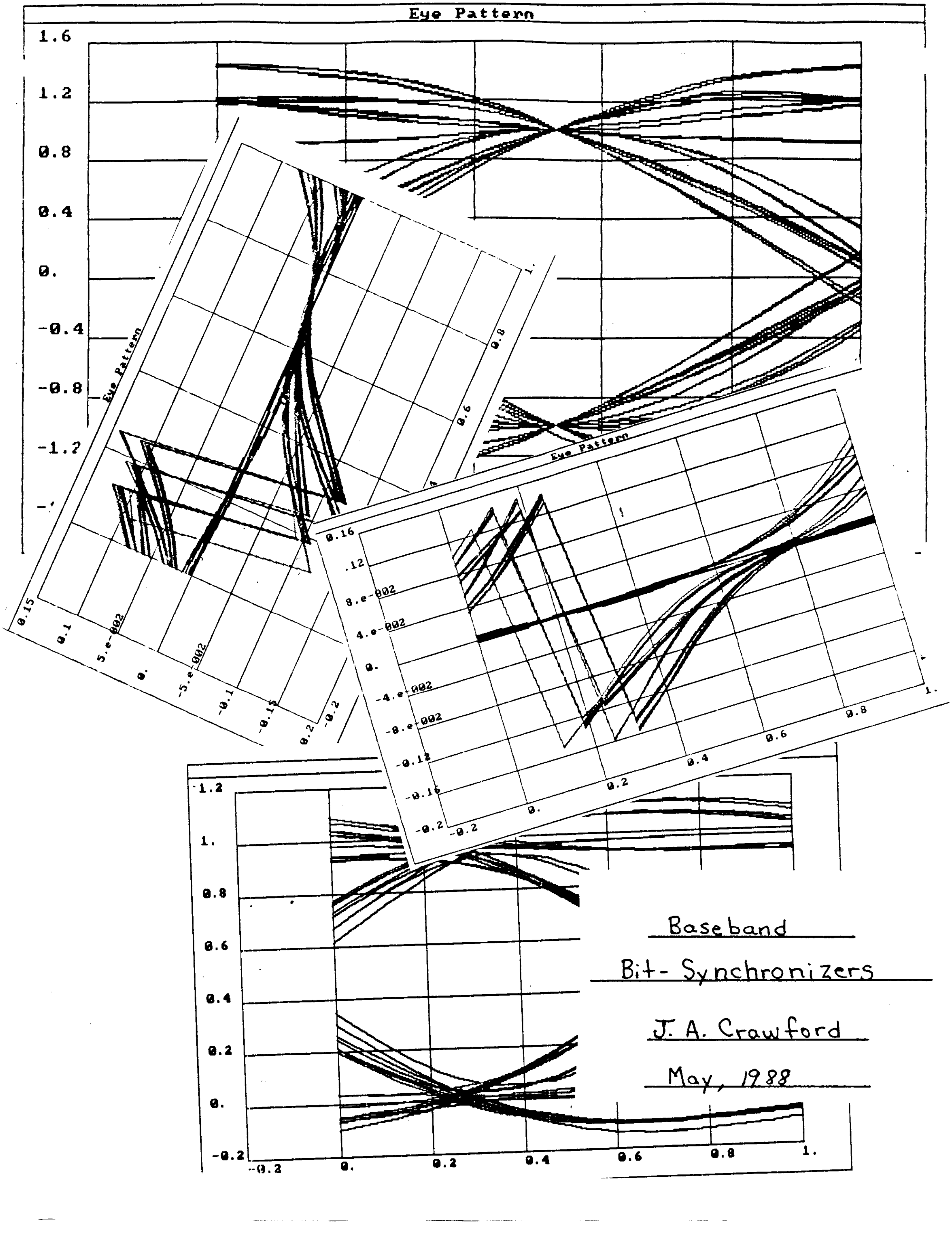


Baseband Bit-Synchronizers

J. A. Crawford

May, 1988

Bit Synchronizers

In digital communication systems, optimum estimation and detection algorithms require that precise Knowledge of the bit transition time be Known to the receiver before a bit-by-bit detection can be made.

Bit Synchronizer : A device/circuit which recovers or reconstructs the underlying digital signal timing thereby allowing high-quality data bit detections (ie. conversion to "ones" and "zeros") to be made.

Of coarse for best performance, timing recovery and data detection should be done in an optimal manner.

In the context of digital RF communications, it is possible to consider RF carrier phase and symbol synchronization jointly. (see [1], [4])

We will only address baseband bit Synchronization in a linear additive white Gaussian noise channel (AWGN).

Rigorously speaking, design and analysis of high performance bit synchronizers involves a number of disciplines:

- Digital Communications Theory
- Estimation Theory

  optimum detection & timing extraction

- Phase-Locked Loops
  - Digital
  - Analog
- Stochastic Processes
  - Stationary
  - Cyclostationary

  Tracking loop behavior with poor signal-to-noise ratio

- Probability
  - Markov Chains
  - Fokker-Planck
  - Renewal Theory

  Complex multi-mode acquisition/behavior

We will address only the basics of bit synchronizer design/analysis.

Note 1: In general, bit synchronizer complexity is strongly driven by two factors:

1) Performance degradation with respect to theory

2) Data rate

Other factors can also drive complexity substantially:

3) Rapid initial synchronization requirement

4) Large data rate anomolies

5) Signal level changes, fading, AGC interactions

6) BER performance floor (ie. P_b as $\frac{E_b}{N_0} \to \infty$)

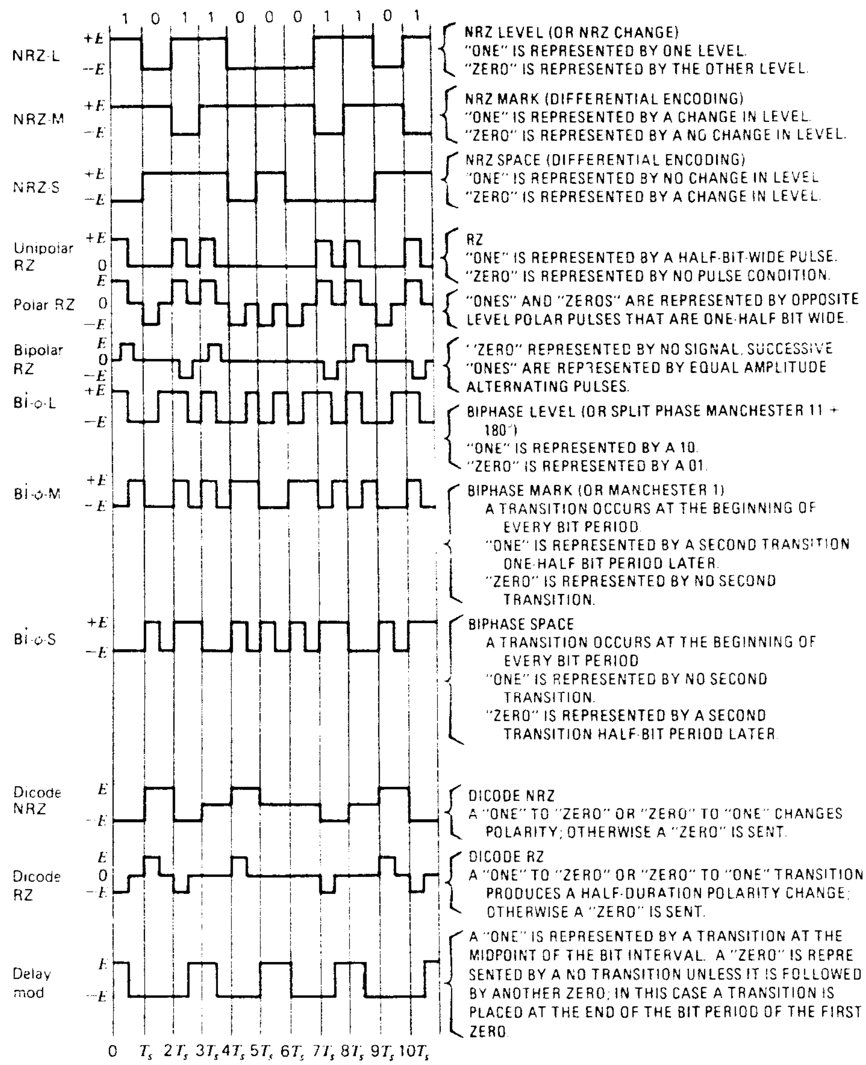
7) Non ideal channel aspects
e.g. nonlinearities, or non-Gaussian noise

System trade-offs are normally necessary.

At "low" data rates, digital signal processing techniques can be employed to achieve nearly optimal results.

At "medium" to "high" data rates, approaches necessarily tend toward all-analog in nature.
Designs with too many "tweaks" and adjustments can produce a manufacturing nightmare.

<u>Note 2</u>: Many different data communication symbol shapes are in use, each in general requiring separate bit synchronizer design consideration.



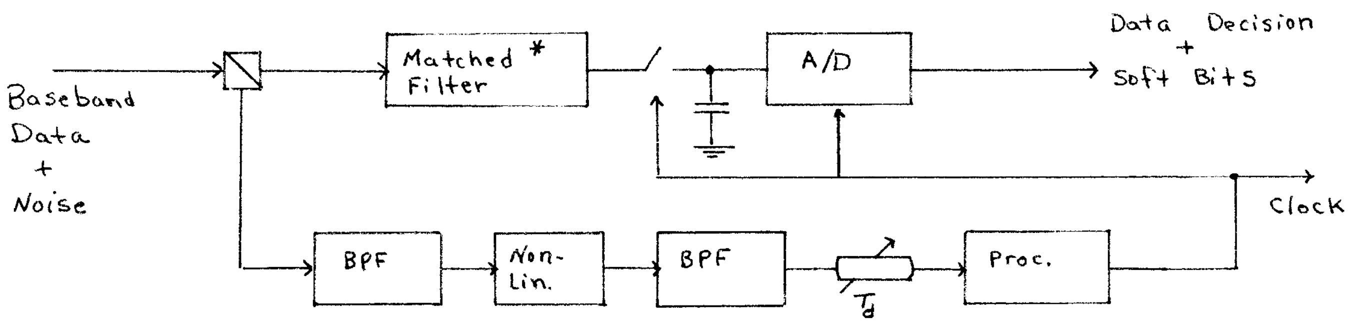
Pulse shaping methods are often employed to conserve bandwidth, etc. (e.g. Nyquist) or obtain other desirable qualities.

Seminar Approach

* Block Diagram Level
  - Indirect* Synchronization
  - Direct* Synchronization
* Data Detection
  - Optimal Detection Assuming Ideal Recovered Data Clock
  - Effects of Adjacent Data Symbols (Intersymbol Interference)
    - Nyquist Pulses (Raised-Cosine)
  - Effects of Static Timing Error
* Timing Recovery
  - An Indirect Approach (Filter-Square-Filter)
  - Direct Approach
    - Phase-Locked Loop Origins
    - Phase Detector Selection
* Detailed Examples
  - Minimum Mean-Square Error Synchronizer
  - Modified Maximum-likelihood Synchronizer
* Other Considerations.

Simplified Bit Synchronizer Block Diagrams

Indirect**



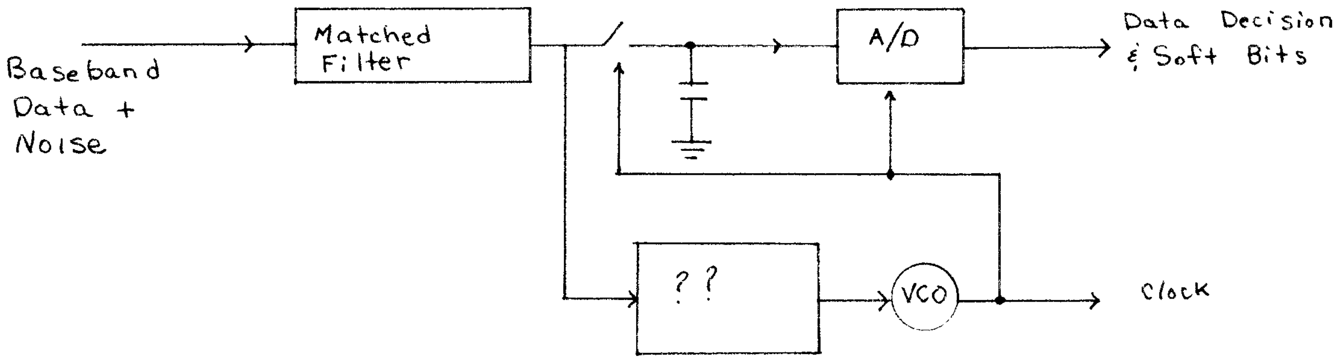
- Employs nonlinear processing of baseband signal to extract data rate.
- Adjustments must be made in the delay line to properly center the sampling operation in the data eye.
- Sampling point is in general not self-correcting
- Improper selection of the two BPF's and nonlinearity can result in poor performance due to high self-noise [2]. Results from noise processes being cyclostationary [3] rather than stationary.
- Detailed analysis for optimal performance provided in [5]. Straightforward symmetry and bandwidth guideline apply to the BPF's. See also [6,7].

* Discussed Later

** My own notation

Block Diagrams (Cont.)

Direct



- The optimal sampling point in the data eye pattern is tracked directly.

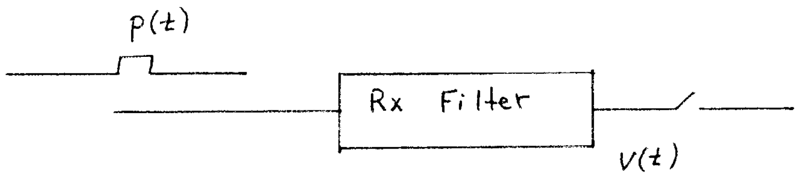
- A control-loop provides precise selection of VCO phase for proper Sampling

- No bandpass filters required. Considerably less hardware than indirect approach usually.

- Self-correcting

Data Detection : Optimal Detection Assuming Ideal Recovered Clock

Consider one data symbol (pulse) alone.



Assume that we know the precise time at which to sample the filter output in order to achieve the maximum sample signal-to-noise ratio.

<u>Question</u>: How shall the receive filter (Rx) be selected for optimal performance?

Total received signal $r(t) = p(t) + n(t)$

$n(t)$ — Additive Wideband Gaussian Noise

$p(t)$ — signal pulse shape

Suppose we sample the filter output $v(t)$ at $t = \hat{t}$

$$V(\hat{t}) = p(t) \circledast h(t)\Big|_{t=\hat{t}} + n(t) \circledast h(t)\Big|_{t=\hat{t}}$$

$\circledast$ — Convolution

$h(t)$ — Filter impulse response

The signal-to-noise ratio (power) is

$$\frac{P_{sig}}{P_N} = \frac{\left| \int_{-\infty}^{\infty} P(f)\, e^{-j2\pi f \hat{t}} H(f)\, df \right|^2}{\frac{N_0}{2} \int_{-\infty}^{\infty} |H(f)|^2\, df}$$

From the Cauchy-Schwartz Inequality,

$$\frac{P_{sig}}{P_N} \leq \frac{\int_{-\infty}^{\infty} |P(f)|^2 df \int_{-\infty}^{\infty} |H(f)|^2 df}{\frac{N_0}{2} \int_{-\infty}^{\infty} |H(f)|^2 df}$$

where $P(f) \overset{\mathcal{F}}{\Longleftrightarrow} p(t)$

$H(f) \overset{\mathcal{F}}{\Longleftrightarrow} h(t)$

$\frac{N_0}{2}$ 2-sided noise power spectral density

$$\frac{P_{sig}}{P_N} \leq 2\frac{E_b}{N_0}$$

E_b = Energy in received pulse

<u>Note 3</u> For maximum output signal-to-noise ratio, R_x filter should be the "matched filter." Equality is satisfied for the matched filter ie

$$\frac{P_{sig}}{P_N} = \frac{2E_b}{N_0}$$

The matched filter is mathematically equal to the complex conjugate of the received pulse shape Fourier transform.

Note 4: The matched filter's impulse response is closely related to the incoming signal pulse shape:

$$H_{MF}(f) = P^{*}(f)$$

$$P(f) = \int_{-\infty}^{\infty} p(t)\, e^{-j2\pi f t}\, dt$$

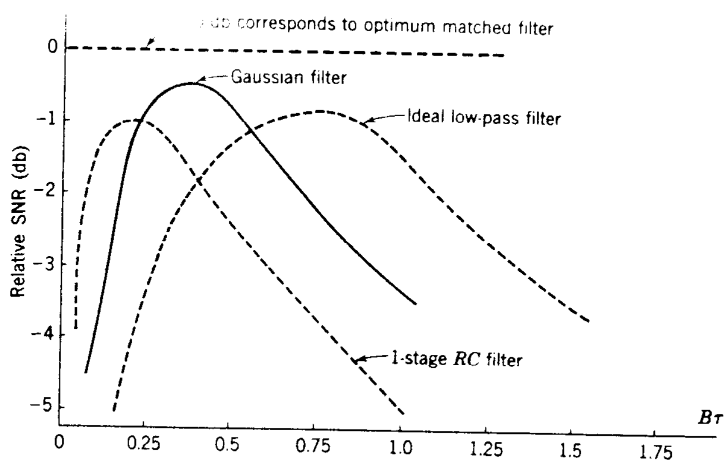
$$\therefore\ P^{*}(f) = \int_{-\infty}^{\infty} p(t)\, e^{j2\pi f t}\, dt = \int_{-\infty}^{\infty} p(-t)\, e^{-j2\pi f t}\, dt$$

$$\therefore\ h_{MF}(t) = p(-t)$$ (Causality issues ignored)

signal pulse reflected about $t = 0$

The theoretical bit error rate performance is

$$P_b = \frac{1}{2}\,\mathrm{erfc}\left(\sqrt{\frac{E_b}{N_0}}\right).$$

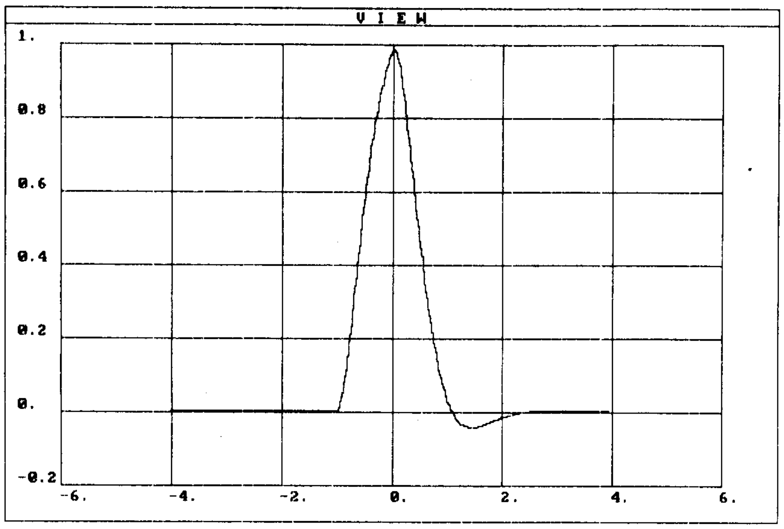


Peak SNR for various filters, compared with matched filter (rectangular-pulse input).

Data Detection: Effects of Adjacent Data Symbols (Intersymbol Interference)

Since the receiver's matched filter has "memory" (ie. impulse response extends over several symbol periods) the presence of adjacent data symbols can degrade performance from theoretical

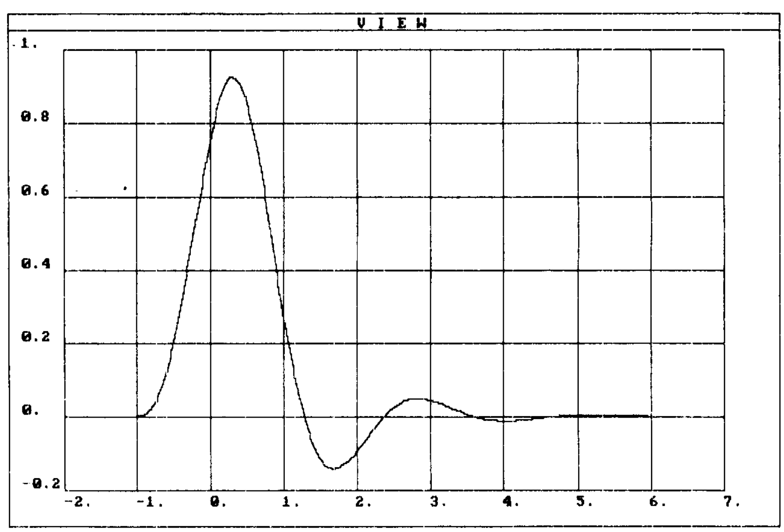
Consider the case of one NRZ data pulse with two different receive filters.



Time t/T

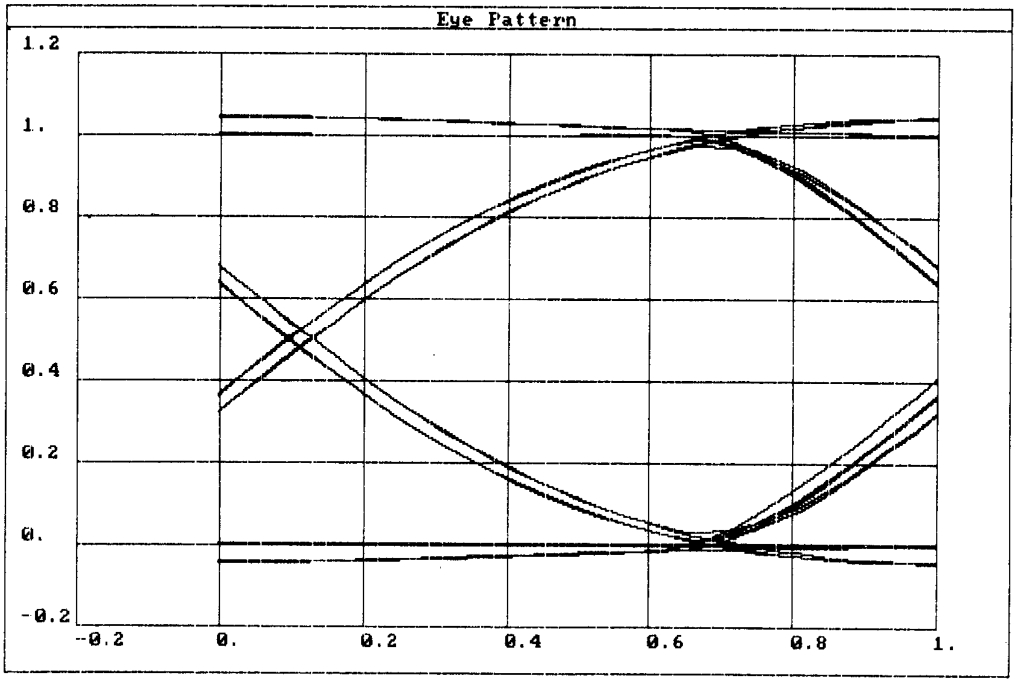
Butterworth
$N = 2$
$BT = \frac{1}{2}$
Symbol period = T sec.

Chebyshev
$N = 3$
$BT = 0.35$
0.1 dB ripple



Time, t/T

Given a data stream, the foregoing single-pulse output shapes may be superimposed assuming random data and an eye pattern constructed assuming ideal clock recovery



Butterworth

N= 2

BT= 0.5

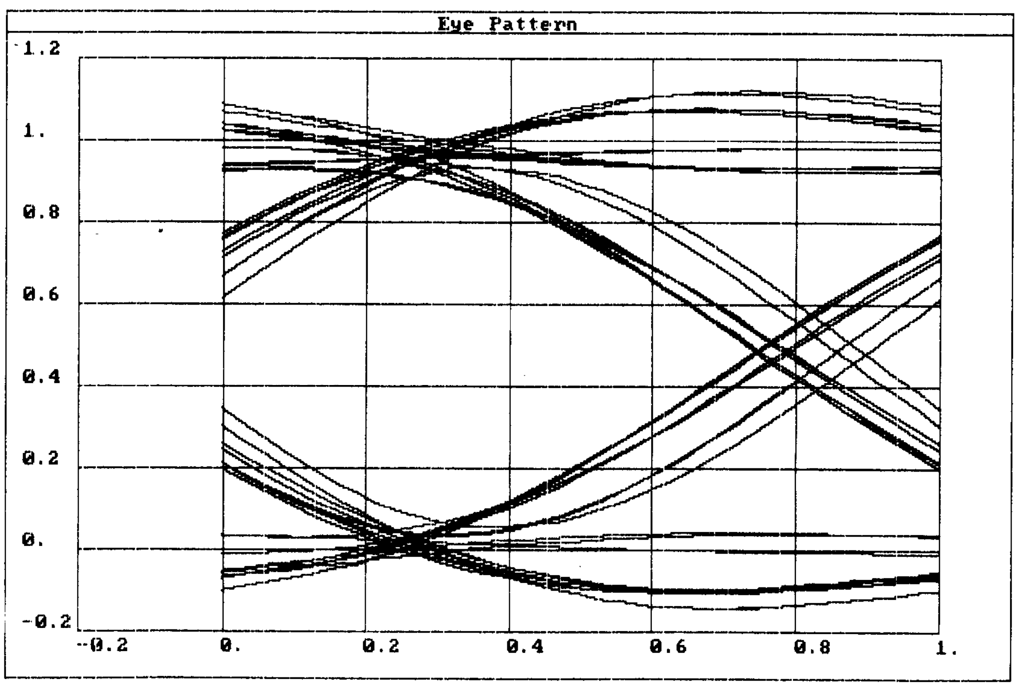
Large open eye.

Chebyshev

N= 3

BT =0.35

0.1 dB ripple



Intersymbol interference effects can be ideally eliminated (assuming ideal clock recovery) provided that pulse shapes satisfying the Nyquist Criteria are used.

Nyquist Criteria for Pulse Shapes Having Zero Intersymbol Interference

The effects of ISI can be completely negated if it is possible to obtain a received pulse shape $p_r(t)$ with the property

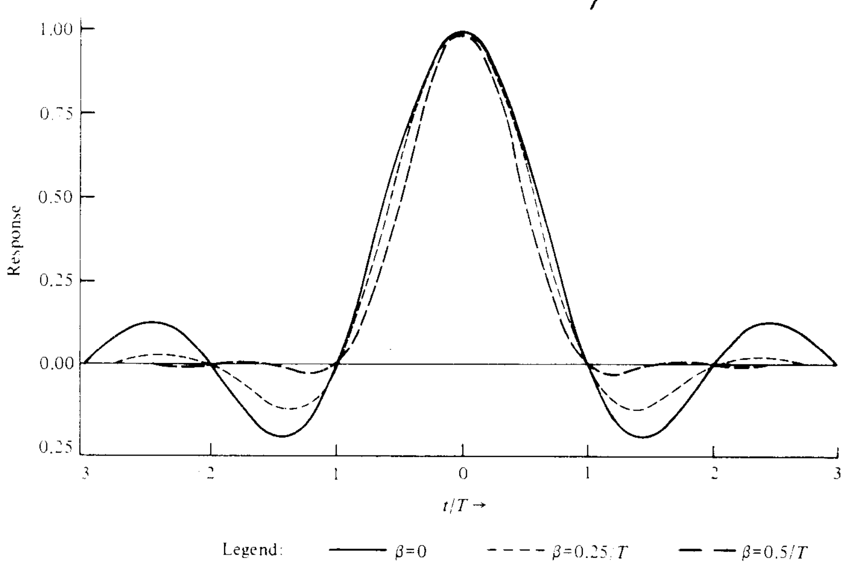
$$p_r(nT) = \begin{cases} 1 & n = 0 \\ 0 & n \neq 0 \end{cases}$$

This goal is met provided

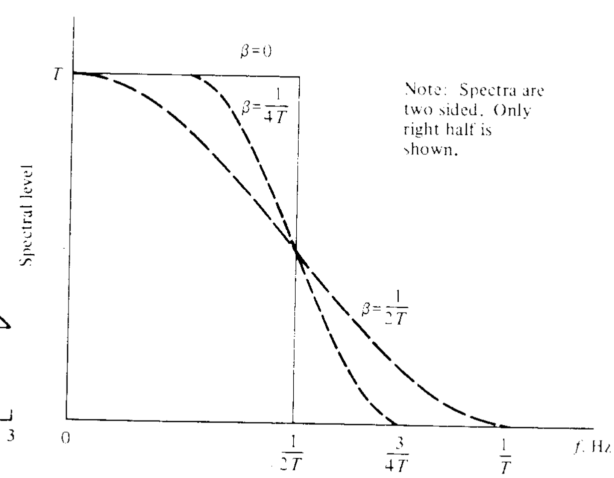
$$\sum_{K=-\infty}^{\infty} P_r\left(f + \frac{K}{T}\right) = T \qquad |f| \leq \frac{1}{2T}$$

where $P_r(f) \overset{\mathcal{F}}{\Longleftrightarrow} p_r(t)$

One family of pulses satisfying this criteria is the raised cosine family

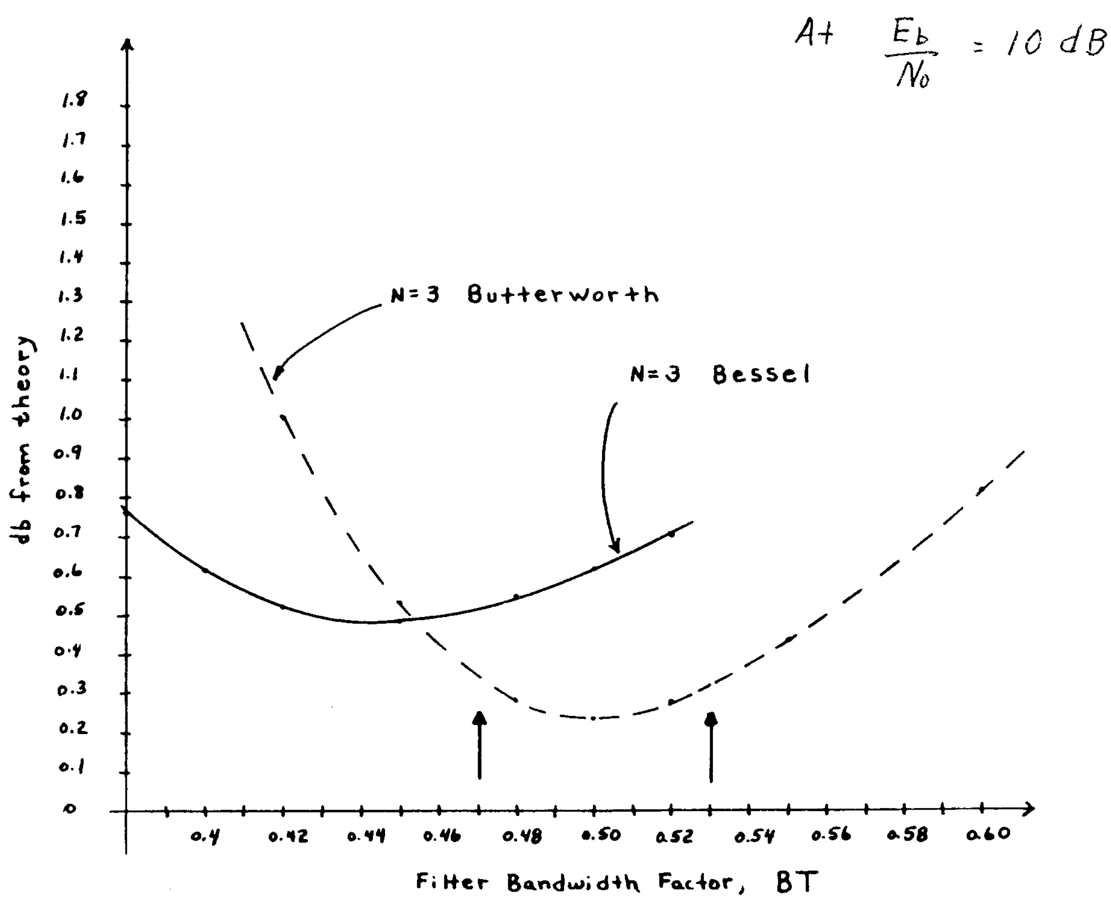


Pulses with raised-cosine spectra.



Raised-cosine spectra.

Imperfect Matched Filter Performance for Square-Root Raised-Cosine Pulses ($\beta = 1/2$)



Note : Although the Butterworth filter is more optimal, its tolerance to BT deviations from nominal is less than for the Bessel.

Later, we will see that the Bessel filter allows slightly better clock recovery compared to the Butterworth.

Calculation of Intersymbol Interference Effects Upon Bit Error Rate (BER) Performance

A number of calculation methods exist.

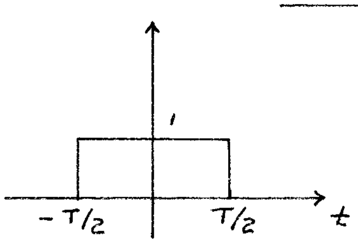
We will consider only

I. Direct ISI Pattern Enumeration

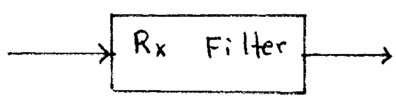
II. Analytical Approach using Characteristic Functions

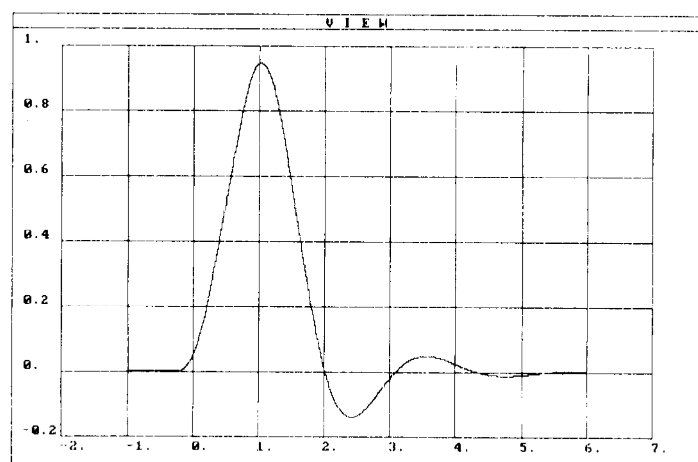
I. Direct ISI Pattern Enumeration

Assume that the matched filter output pulse shape for one input pulse extends only $\pm M$ symbol periods to either side (Beyond which amplitude is "negligible")



Input Pulse



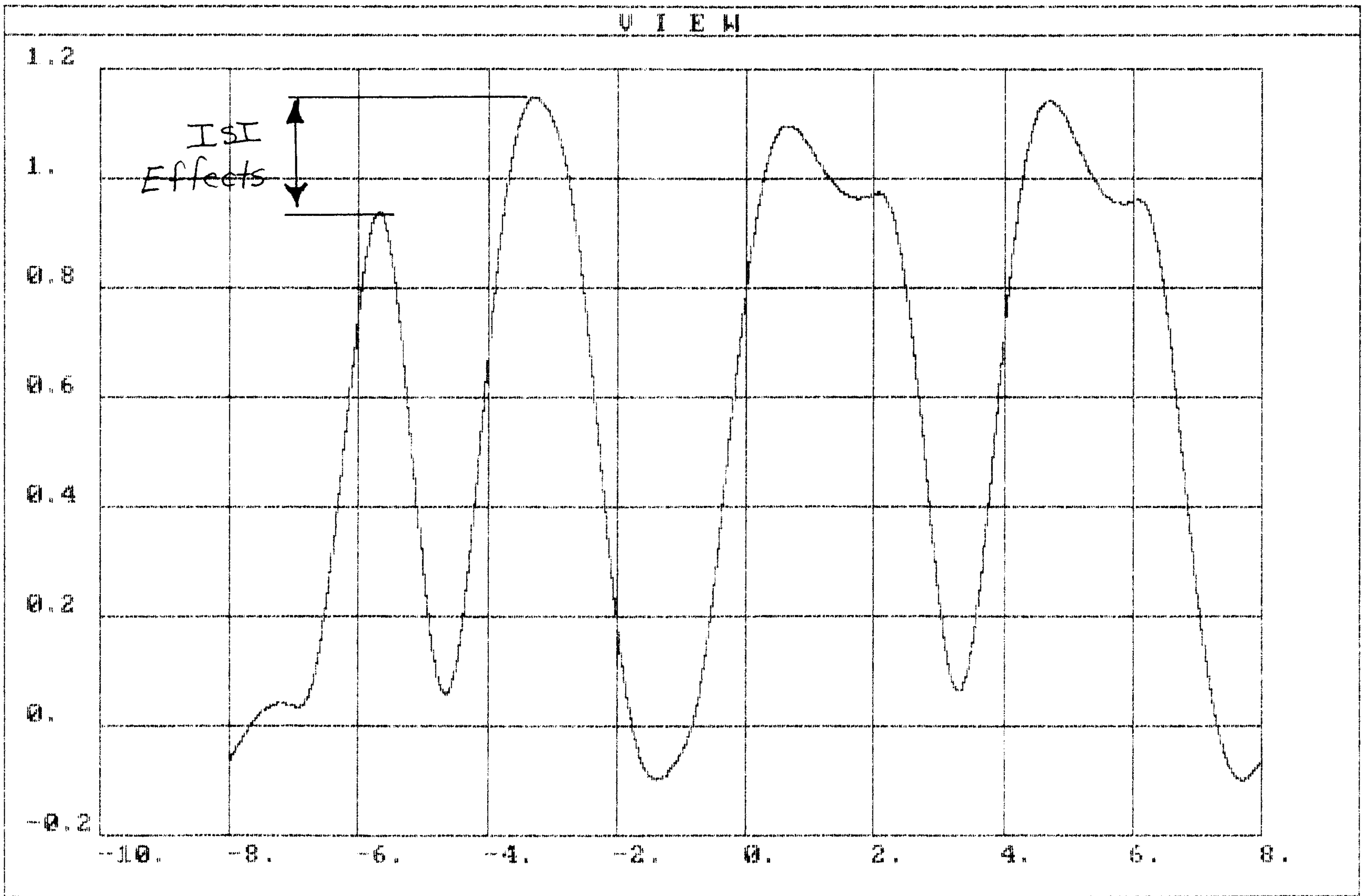


Symbol Period

Then, for a given bit, we must consider the effects of only the adjacent $\pm M$ pulses.

For random bipolar (ie one/zero) data, there are a total of 2^{2M} possible data patterns and therefore 2^{2M} different ISI contributions at the bit in question, all equally likely. <u>and</u> deterministic

16 random NRZ pulses
thru N= 3 Chebyshev filter
BT = 0.35
0.1 dB ripple



Total probability of bit error is

$$P_B = \sum_{i} P_P(i) \; P_B\left(\frac{E_b}{N_o} \,\middle|\, \text{pattern } i \right)$$

All data patterns

Probability of single error given pattern i sent

probability of pattern i

$\left(\frac{1}{2^{2M}}\right)$ for random data

Recall the ideal matched filter result

$$\frac{(\text{Sample Value, no noise})^2}{\text{Noise Variance}} = \frac{2E_b}{N_o}$$

$$P_b = \frac{1}{2} \operatorname{erfc}\left(\sqrt{\frac{E_b}{N_o}} \right) \qquad \text{Theoretical}$$

The presence of ISI merely adds to or subtracts from the filter output sample value.

Effective $\frac{E_b}{N_o}$ with ISI pattern i present is

$$\frac{[V_S + V_{ISI}(i)]^2}{2 \text{ Noise Variance}} = \left(\frac{E_b}{N_o}\right)_{\text{eff } i}$$

Note that some patterns will aid the signal, others will detract.

$$P_B\left(\frac{E_b}{N_o} \,\middle|\, \text{pattern } i \right) = \frac{1}{2} \operatorname{erfc}\left(\sqrt{\left(\frac{E_b}{N_o}\right)_{\text{eff } i}} \right)$$

(V_S is the observed peak matched filter output for one pulse, no noise).

II. Analytical Approach Using Characteristic Functions

Think of a data eye pattern with Gaussian noise and Intersymbol Interference (ISI) present.

If ISI effects are considered over $\pm M$ adjacent symbols as $M \to \infty$, the ISI contribution in the eye is a random variable (certainly not Gaussian) independent of the additive Gaussian noise.

Since the pdf of a sum of two random independent variables is a convolution of each respective pdf, we can use characteristic functions in the frequency domain to obtain

$$P_b = \frac{1}{2} - \frac{1}{\pi} \int_0^{\infty} \frac{\sin[\omega h(t_0)]}{\omega} e^{-\frac{1}{2}\sigma^2\omega^2} C(\omega) \, d\omega$$

where

$$C(\omega) = \prod_{\substack{e=-L \\ \neq 0}}^{L} \cos(\omega h_e)$$

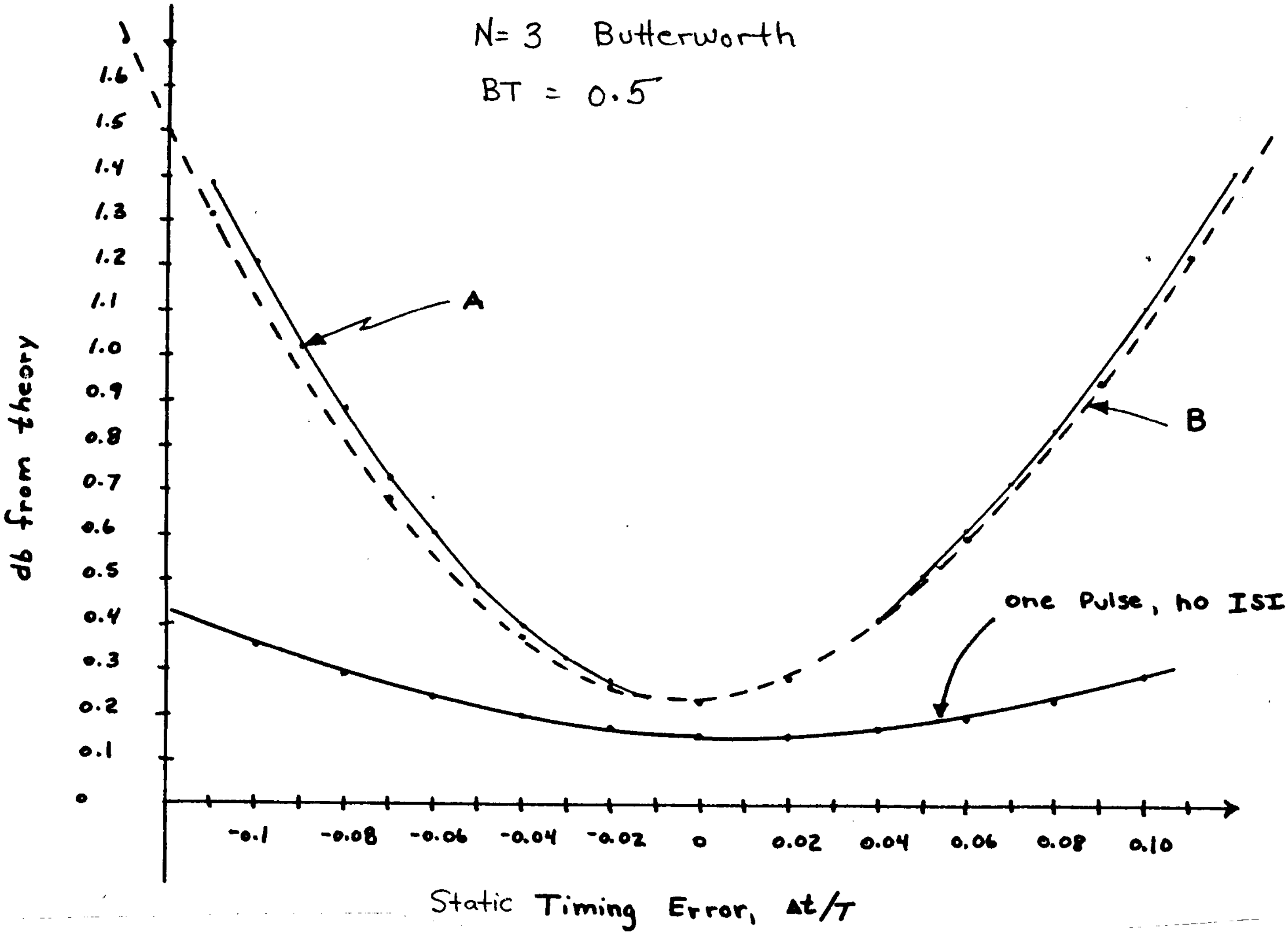
h_e is the output pulse shape value sampled eT seconds from the peak value which occurs at $t = t_0$

σ^2 Variance of output Gaussian noise from filter $= N_0 B_n$ where B_n is the effective filter noise bandwidth

Comparison of ISI Calculations

Square-Root Raised Cosine Pulse $\beta = 1/2$

(Ideal Clock Recovery)



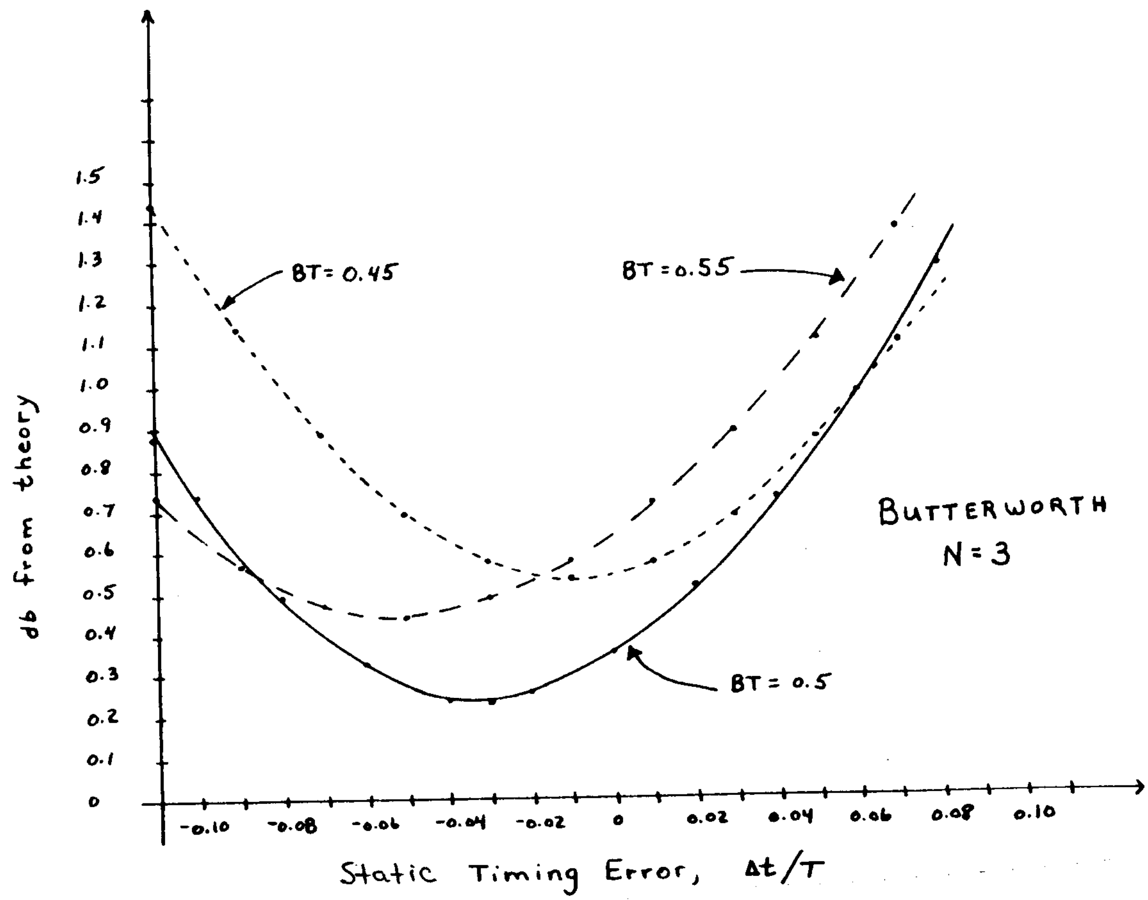
A ISI Pattern Enumeration $E_b/N_0 = 10$ dB

B Characteristic Function Method $E_b/N_0 = 9.6$ dB

Note that the one-pulse result is a lower bound on performance degradation.

Data Detection: Effects of Static Timing Error

If the recovered data clock causes the data eye to be sampled too late or early, degradation in performance results.

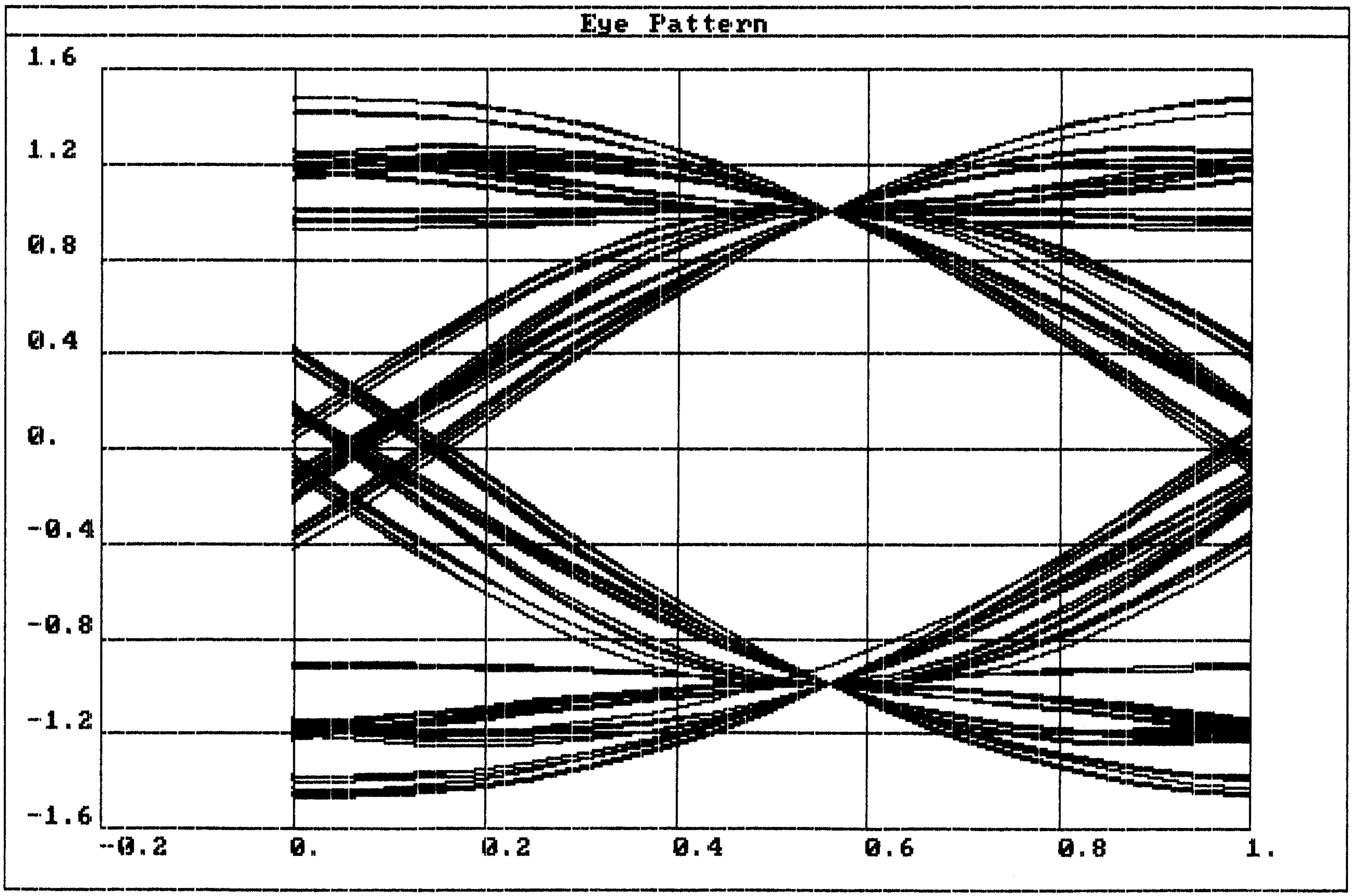


Short of brute-force simulation, ascertainment of combined degradation due to matched filter aspects & timing errors is difficult.

When timing is recovered via a phase-locked loop, the total performance degradation can be approximated by weighting the above curves with an assumed pdf for the timing error (normally Tikhonov) and integrating (convert "dB from theory" to BER first).

Ideal Raised-Cosine $\beta = \frac{1}{2}$

Note that the Sample Variance is a strong function of static timing error.



Timing Recovery

Optimal data stream clock recovery is mandatory for high performance bit synchronizers.

Clock recovery analysis/design is often complicated by the use of *nonlinear* signal processing techniques.

Optimal approaches are linked closely to MAP, ML, MMSE, etc. estimators of the true data clock.

The employed clock-recovery technique is highly dependent upon the underlying data stream pulse shape

e.g. Manchester data guarantees that each data symbol will have a *mid-symbol* transition which makes clock recovery particularly easy

Square-and-filter techniques (discussed next) are often used in clock-recovery of NRZ data but are useless over (ideally) infinite bandwidth channels

Many synchronization techniques exist ⌣ appropriate use must be carefully assessed.

Ref. [8]

Optimum Estimation of Bit Synchronization

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Abstract

In digital communication systems, optimum estimation and detection algorithms require that precise knowledge of the bit transition time be known to the receiver before bit-by-bit detection can be made. This paper presents the derivation of Bayes or maximum a posteriori estimation algorithms for optimum estimation of bit timing. Performance of the optimum system is evaluated and suboptimal realizations suggested.

Manuscript received October 12, 1968.

I. Introduction

In digital communication systems, the theory of optimum data detection requires that precise knowledge of the bit transition time be known to the receiver before a bit-by-bit detection can be implemented. The optimum receiver for a PSK modulated waveform embedded in additive Gaussian noise is the matched filter or the correlation detector. This device is usually implemented by an integrate and dump circuit which requires the bit timing of the incoming sequence; this timing is supplied by the bit synchronizer. Self-synchronization systems, systems which acquire bit synchronization timing directly from the incoming modulated data sequence, are generally required for most applications. The majority of the present-day bit synchronizers are designed to operate on the noisy baseband analog data. This may not be the best technique for a completely digitalized receiver since it requires that the sampled IF or carrier data be used to estimate carrier and/or subcarrier frequency and phase of the incoming sequence. The resulting estimate is then used to convert the received waveform to an analog baseband process. Although the idea of converting from analog to digital signals, estimating frequency and phase, then converting back to an analog baseband process may not be too appealing from the digitized receiver viewpoint, it does place the bit synchronization estimation problem within the framework where a large amount of research has been performed. Furthermore, this conversion to an analog baseband process can probably be avoided while still using the available theory and digital implementation techniques developed for the baseband model.

Two metrics are generally used to measure the performance of bit synchronizers, the rms jitter or timing misalignment and bit slippage. Which of these is more important depends on the type of data being transmitted and the type of modulation employed. Probably the most widely used performance metric for digital communication systems is the bit error probability (BEP) versus the average bit energy per noise density, E/N_0. Degradation in BEP performance can be directly related to the bit timing misalignment. On the other hand, the effect of bit slippage is not easily related to the BEP performance, and is usually related to how it effects the word synchronization.

Lindsey [1] has determined the effect of phase jitter on BEP performance, the phase jitter being caused by the noisy subcarrier which is acquired by phase-lock loop techniques. Wintz and Hancock [2] determine the effect on BEP performance caused by errors in arrival time of exponential nonoverlapping pulses. Neither of these techniques are directly applicable to the static timing misalignment effect on the BEP performance. Wintz and Hancock do not consider the effect of observing a bit interval of time which overlaps two consecutive incoming bit intervals. This overlapping is necessarily the case in most PCM bi-level systems before bit synchronization has been acquired. Lindsey's work is mainly concerned with phase error associated with subcarrier acquisition and its

An Indirect Approach

Filter - Square - Filter

This approach is now fairly classical having seen much application.

From [5]

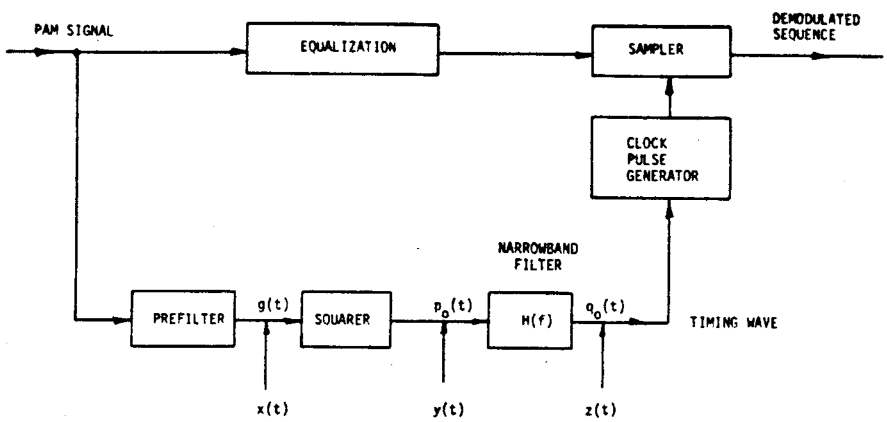


Fig. 1. Signal path and timing path in a PAM receiver. In practice, the major portion of the equalization would precede both paths.

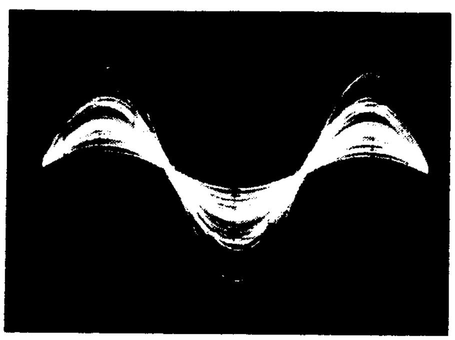


Fig. 2. Oscillographic display of the timing wave process. See text for details.

Simple symmetry criteria have been derived for the pre-filter and narrowband filter to achieve optimal performance.

Major drawbacks include the necessity of potentially 2 additional filters, group delay adjustment, and degradation for other than nominal data rate.

Occasionally performance requirements and system attributes result in particularly simple synchronization solutions [9]

Channel constraints or implementation may also dictate the proper design approach.

e.g. a *digital transition tracking approach is described in [10]. An all-digital implementation.*

<u>Direct Approach</u> (MMSE)

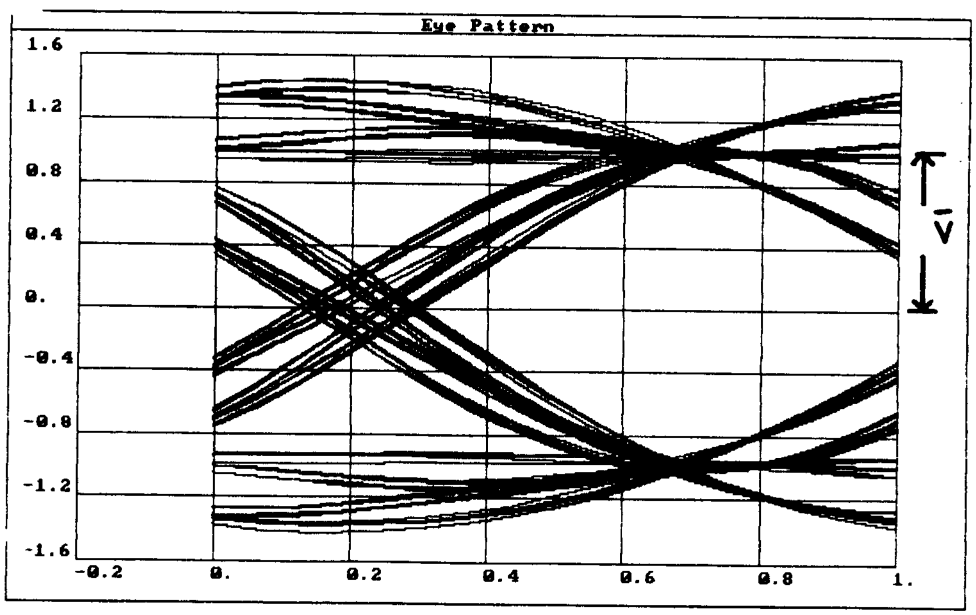
The approach(es) I have termed "direct" seek to track the optimal sampling point in the eye-pattern <u>directly</u>.

These approaches do not assume for instance a constant time period between transitions and sampling point in the data eye.

The minimum mean-square error criteria causes the synchronizer electronics to position the sampling point within the eye pattern such that the sample variance is minimized

$$\text{Variance} = \overline{\left[V(\hat{t}) - a_i \bar{V} \right]^2} \quad ; \quad \hat{t} \text{ Sampling position}$$

a_i data symbols, ± 1



Square-Root Raised Cosine Pulses $\alpha = 1/2$
N = 3 Butterworth BT = 0.5

Heuristically speaking, to minimize the variance,

$$\overline{2\left[V(\hat{t}) - a_i \bar{V} \right] \dot{V}(\hat{t})} = 0$$

is desired.

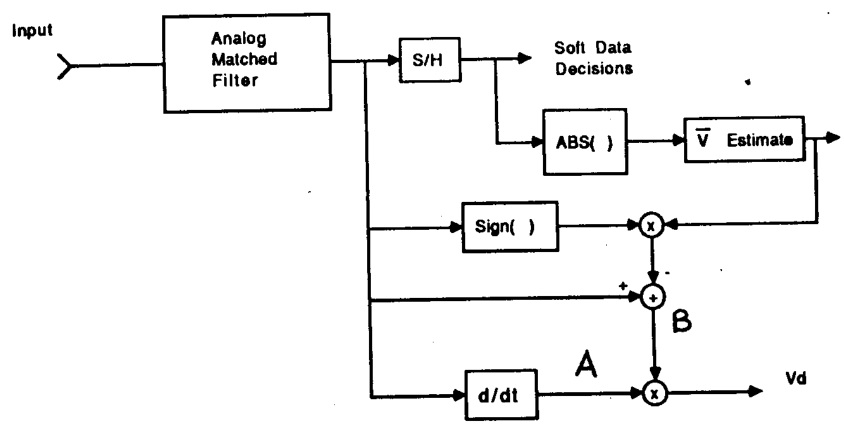
The filtering/smoothing leads to a natural inclusion of phase-locked loops. Note: Use of PLL's for synchronization is linked to sub-optimal estimators See [1], [4], [8] The preceding heuristic result describes the required structure for the MMSE phase detector.

In synchronizers employing phase-locked loops, selection of the phase detector is the single most important consideration which must be made. Improper selection results in

- possible complete inoperation
- high self-noise [2]
- false locking points
- inadequate robustness for noise, channel distortion, rate jitter, etc.
- in general, poor performance

MMSE Example Square-Root Raised Cosine Pulses

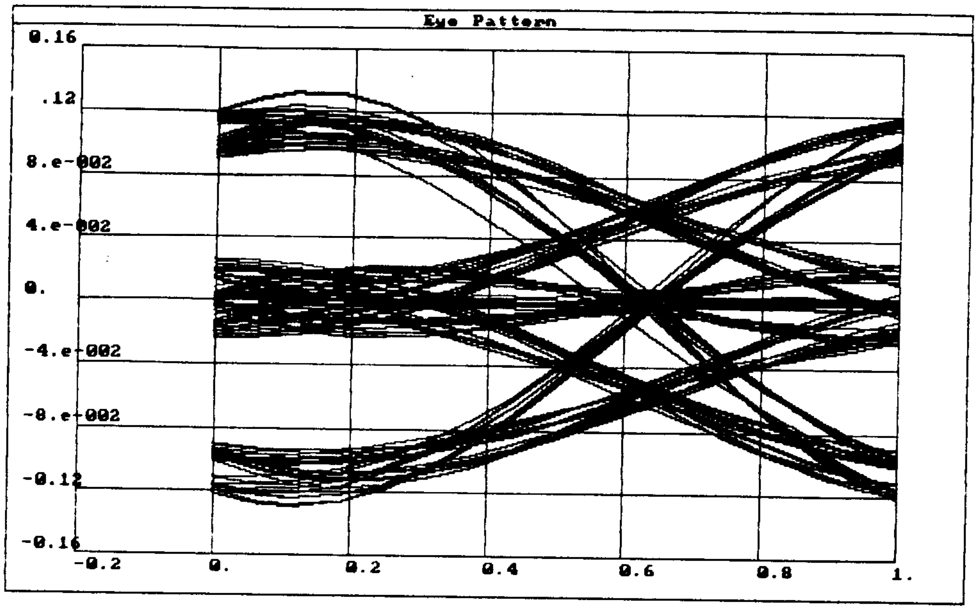
MMSE Phase Detector



MMSE Phase Detector: Internal Signals

Square-Root Raised Cosine Pulses
$\alpha = 1/2$

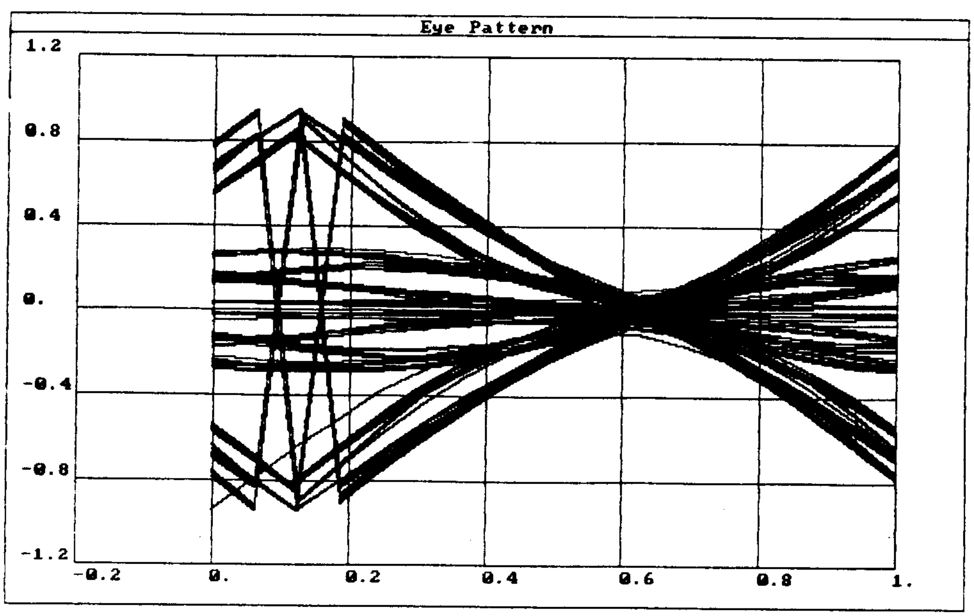
N= 3 Butterworth
BT = 0.5



Differentiator output

AT no point in the eye pattern is the differentiator output always zero.

'A'

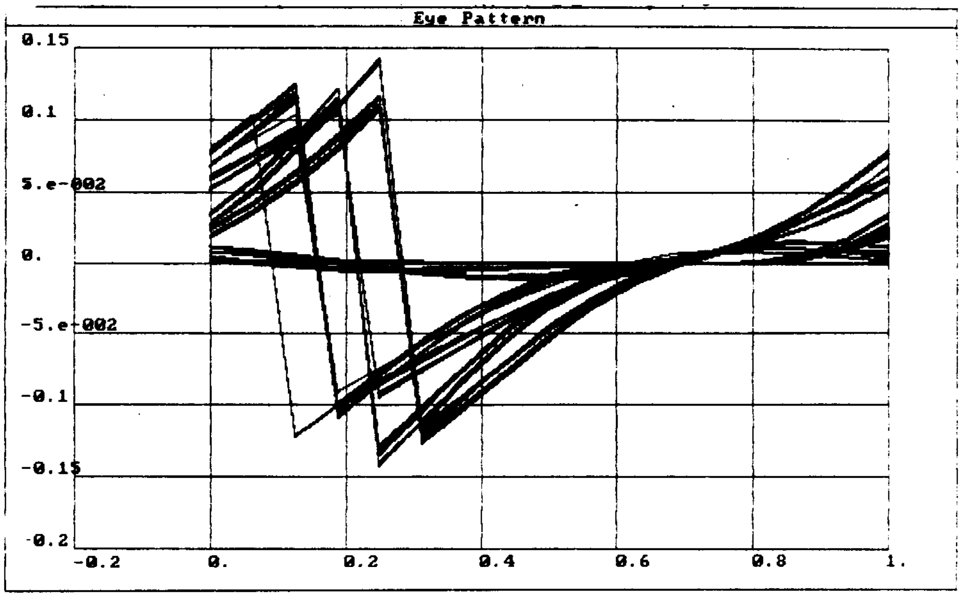


Summer Output

As an even signal, it alone is also unsuitable for the phase detector function.

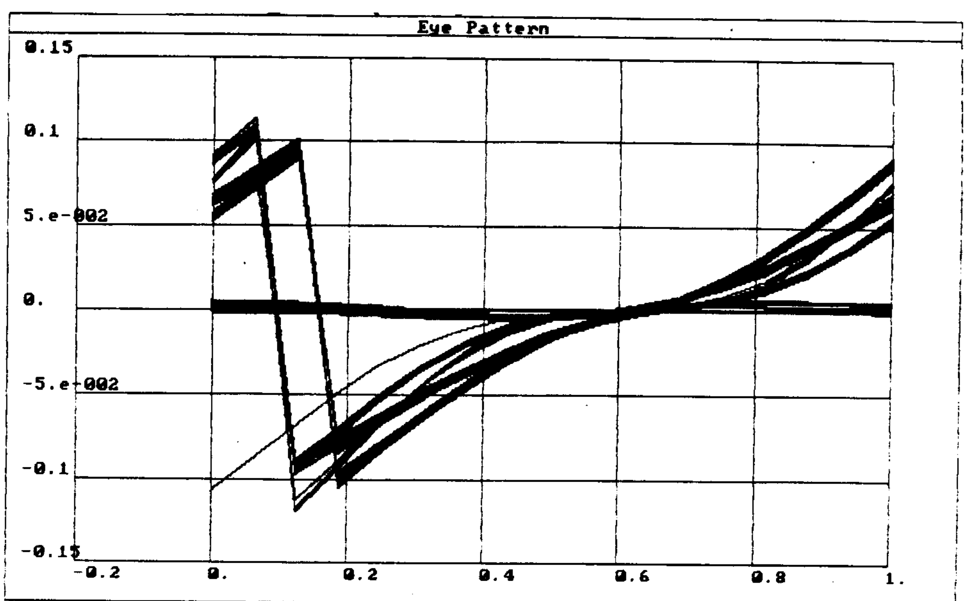
'B'

MMSE Phase Detector Output :
'A' * 'B' Gives Phase Detector Characteristic 'S' Curve



'S' Curve

N= 3 Butterworth
BT = 0.5

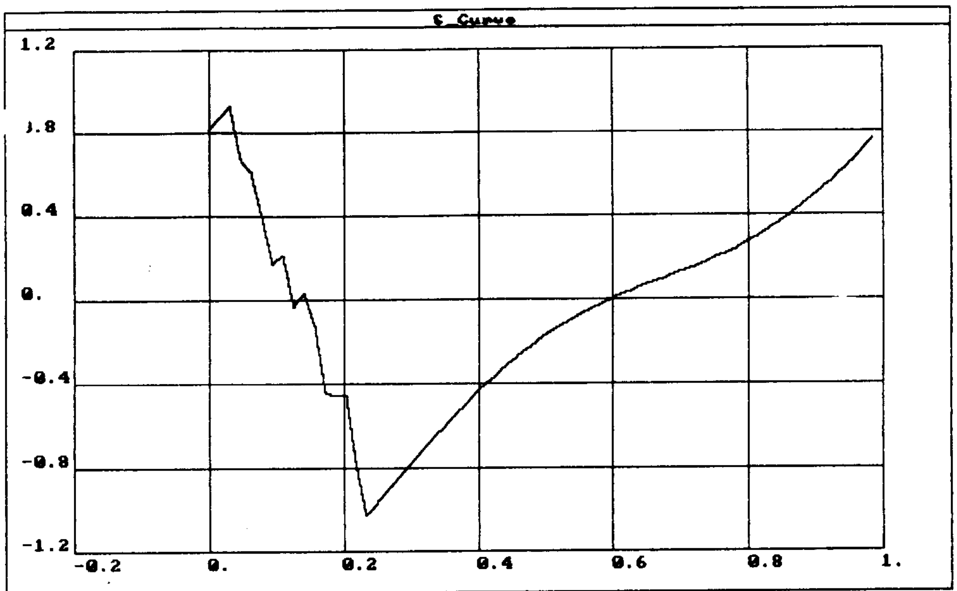


'S' Curve

Bessel Matched Filter

- Althoug the Bessel filter results in a lower- variance S- curve, the Butterworth is more optimal as a matched filter approximation.

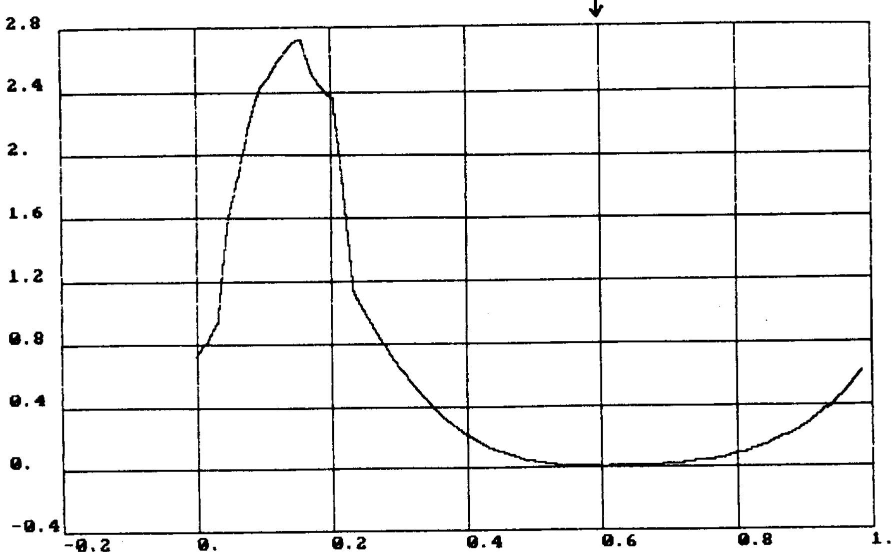
The true phase detector S curve is an average of the signal trajectories possible at the phase detector output across $\pm \pi$ rad.



Normalized S- Curve

$\frac{E_b}{N_0} \rightarrow \infty$

↑ Track Point ↓

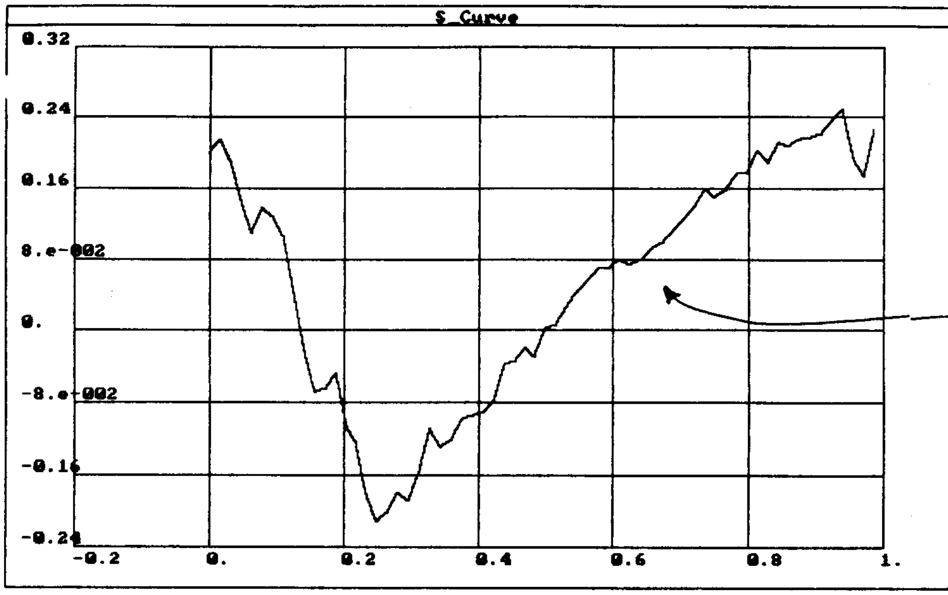


Phase Detector Output Noise Variance as a Function of Sampling Point

Note: Variance ~ 0 at proper sampling point.

- Note that noise variance is a function of tracking error.

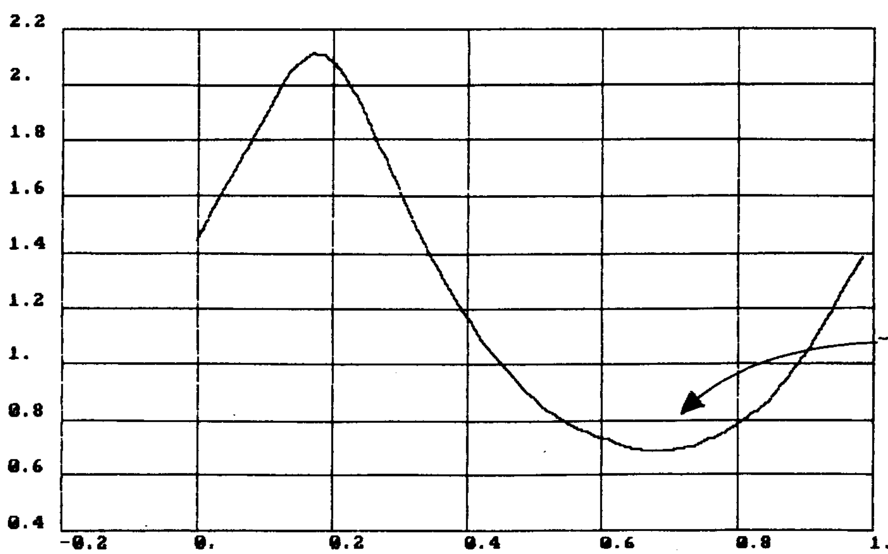
The phase detector S-curve and tracking variance degrade markedly at poor E_b/N_o.



S- Curve

$\frac{E_b}{N_o} = 3\,dB$

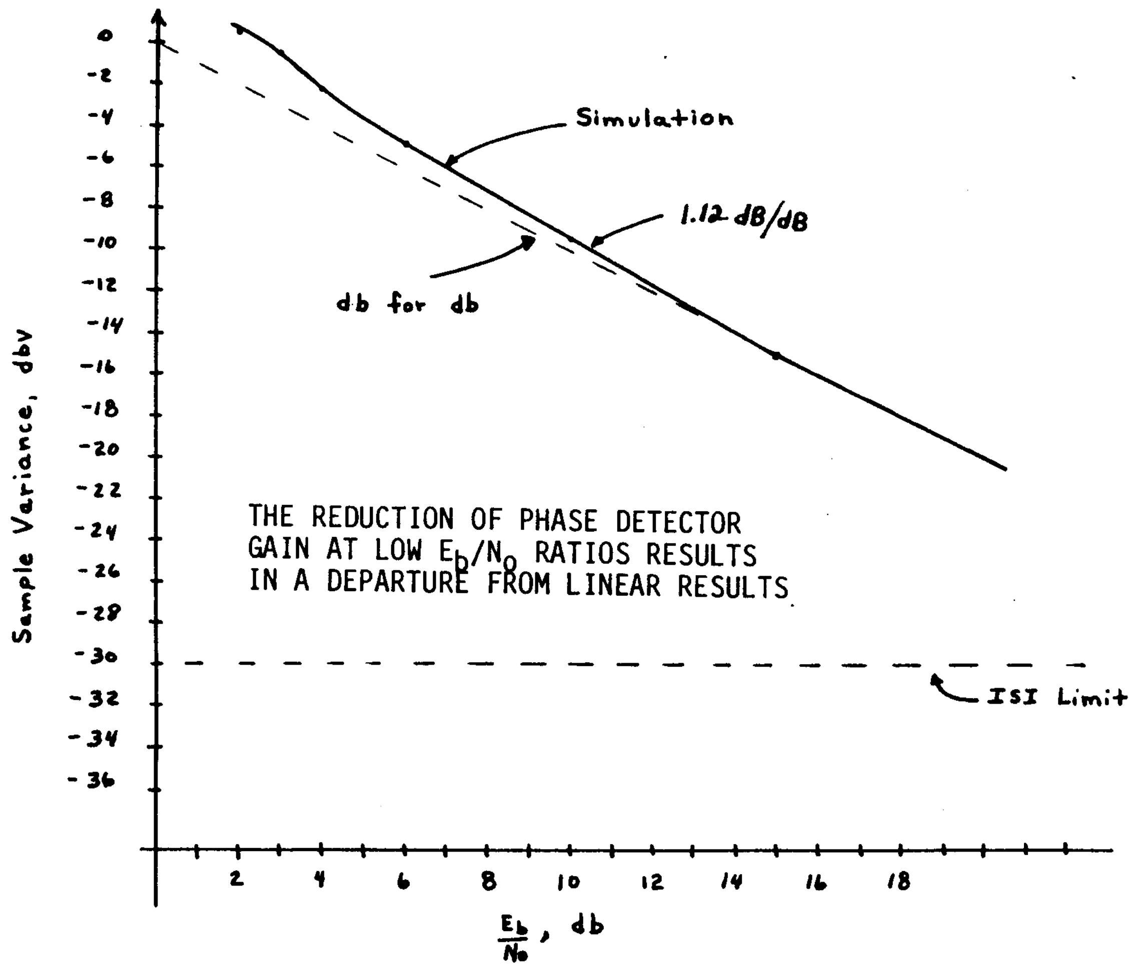
Note the appearance of a D.C. offset



Phase Detector Output Noise Variance

Track Variance Now Substantial

PHASE DETECTOR ERROR VARIANCE VS. E_b/N_o



THE REDUCTION OF PHASE DETECTOR GAIN AT LOW E_b/N_o RATIOS RESULTS IN A DEPARTURE FROM LINEAR RESULTS

M/A-COM Government Systems Division

GOI BIT SYNCHRONIZER DESIGN

- **The theoretical complexity of the design problem mandates a combination of analytical and simulation tools be used**

- **For example, the power spectral density out of the phase detector is <u>approximately</u>**

$$S(F) \approx 2\,T\,R_d(0)\,\mathrm{sinc}^2(\pi f T)\left[1/2 + \sum_{m=1}^{\infty} \frac{R_d(m)}{R_d(0)} \cos(2\pi f m T)\right]$$

where

Statistical Expectation

$$R_d(m) = \boxed{E}\left\{ \dot{X}_m X_m \dot{X} X - \dot{X}_m X_m \dot{X} L - \dot{X}_m L_m \dot{X} X + \dot{X}_m L_m \dot{X} L + \dot{X}_m N_m \dot{X} N + \dot{X}_m N_m \dot{N} X - \dot{X}_m N_m \dot{N} L + \dot{N}_m X_m \dot{X} N + \dot{N}_m X_m \dot{N} X - \dot{N}_m X_m \dot{N} L - \dot{N}_m L_m \dot{X} N - \dot{N}_m L_m \dot{N} X + \dot{N}_m L_m \dot{N} L + \dot{N}_m N_m \dot{N} N \right\}$$

34

24

The first expectation term is

$$\overline{\dot{X}_m X_m \dot{X} X} = \sum_i \sum_k \dot{\tilde{g}}(\hat{t} - mT - iT)\,\tilde{g}(\hat{t} - mT - iT)\,\dot{\tilde{g}}(\hat{t} - kT)\,\tilde{g}(\hat{t} - kT) \;+$$

$$\sum_i \sum_j \dot{\tilde{g}}(\hat{t} - mT - iT)\,\tilde{g}(\hat{t} - mT - jT)\,\dot{\tilde{g}}(\hat{t} - iT)\,\tilde{g}(\hat{t} - jT) \;+$$

$$\sum_i \sum_j \dot{\tilde{g}}(\hat{t} - mT - iT)\,\tilde{g}(\hat{t} - mT - jT)\,\dot{\tilde{g}}(\hat{t} - jT)\,\tilde{g}(\hat{t} - iT)$$

- **This result assumes an open data-eye and ideal $\overline{V}$ value**

$g(t)$ Square-Root Raised Cosine Pulse

$\tilde{g}(t)$ Output of matched filter, acting upon $g(t)$

Aside :

The need for a *low-variance* phase detector output is primarily accute where maximum phase-locked loop bandwidth is required e.g. for fast acquisition and/or high frequency jitter tolerance.

PLL Parameters

Barring complicated system requirements, the design may be completed as follows: (1st order)

1) The slope of the computed S-curve is the phase detector gain, Volts/radian (K_d)

2) From the matched filter analysis of static tracking error effects upon BER, a peak allowable tracking error is selected, θ_{PK}, rad.

3) From the S-curve variance calculations, the effective phase detector output power spectral density is calculated (assumed flat) N_P, V^2/Hz

4) The maximum permissible PLL noise bandwidth is calculated using Martin's criteria [See Gardner]

$$\lambda_1 \frac{\sqrt{N_P B_n}}{K_d} + \theta_{Stress} \leqq \theta_{PK}$$

loop stress due to FM, etc.

tracking noise

Confidence criteria, Normally taken as 3.

The noise bandwidth (single-sided) for a Classic Type II PLL is

$$B_n = \frac{\omega_n}{2}\left[\zeta + \frac{1}{4\zeta}\right]$$

Actual circuit parameters are realized via

$$\omega_n = \sqrt{\frac{K_d K_V}{\tau_1}}$$

$$\zeta = \frac{1}{2}\omega_n \tau_2$$

Further considerations for capture range, etc. must normally be given as well.

Simulating the System

Owing to the synchronizer complexity, it is prudent to confirm the design by simulation prior to actually constructing hardware.

Simulation Tips

- A state variable discription/approach is recommended.

- Be cautious of round-off errors and instabilities introduced by your selected method of integration. Note that backward Euler integration is much preferred over forward.

  In general, implicit methods such as Adams-Moulton give the most accurate & fast results.

- Be certain that the integration time step is much smaller than any underlying system dynamics (else experience "ringing" integration with higher order formulas)

- Confirm the statistics of the selected Gaussian noise model. Understand how the sampling nature of the simulation effects things.

- Before drawing conclusions, employ statistical bounds such as the Cramer-Rao bound to ensure the confidence criteria you are trying to meet (e.g. for ± 0.25 dB accuracy in E_b/N_0 assessment, how many symbols must be simulated?)

- For difficult simulation tasks such as very low BER (e.g. 10^{-9}) avoid brute force techniques in favor of mixed approaches

  e.g. low BER assessment

  The matched filter output samples are a mixture of Gaussian noise, intersymbol interference, and clocking error effects.

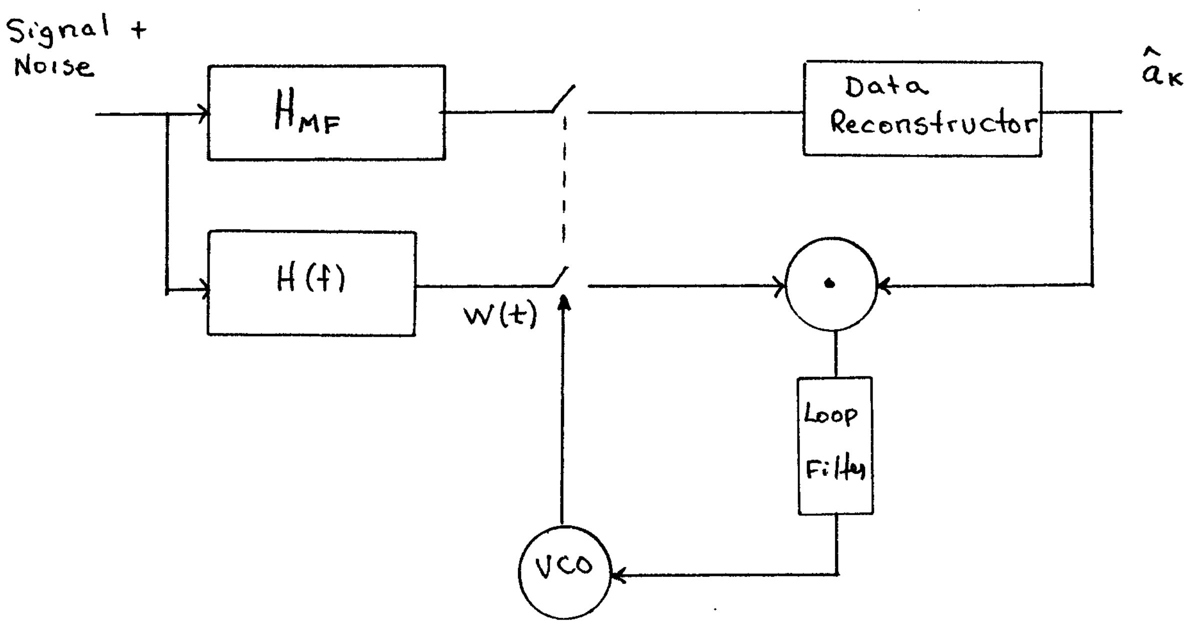
  The underlying probability distribution function can be found by accumulating moments of all the sample values and using properties of characteristic functions.

  Given the pdf, the BER may be found.

Modified Maximum-Likelihood Synchronizer

Serious reader referred to [11]

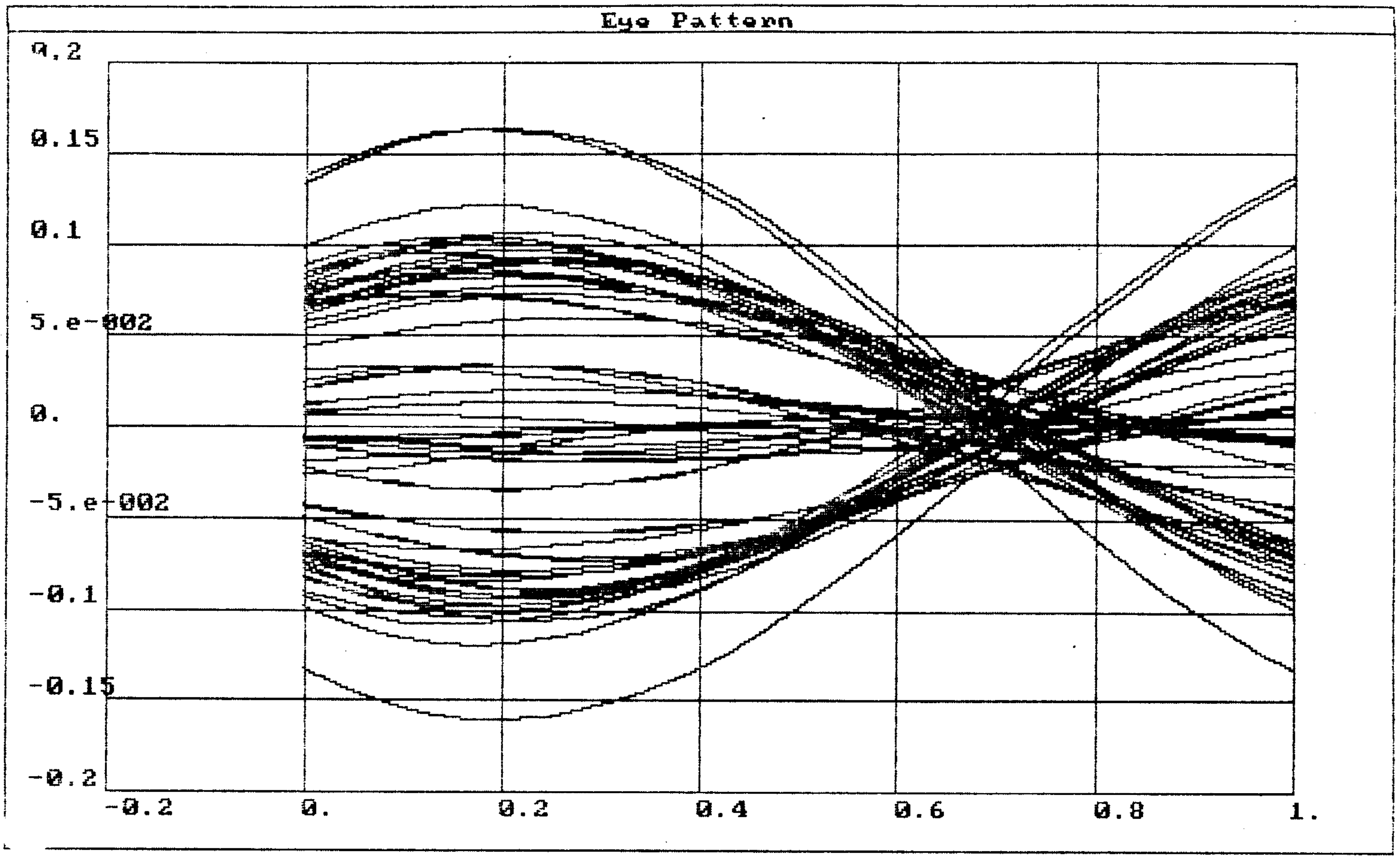
This method seeks to find a filter $H(f)$ which produces a recovered timing wave with no intersymbol interference.



By using methods of the calculation of variations, the recovered timing wave $W(t)$ may be minimized wrt. AWGN and ISI by selecting

$$H(f) = H_{MF}(f)\left[j2\pi f - \sum_m \frac{\dot{r}(mT)}{r(0)} e^{-j2\pi f T m} \right]$$

where $\quad r(t) = \tilde{g}(t) \quad$ ie. filtered pulse shape



Timing Filter Output

2 Taps

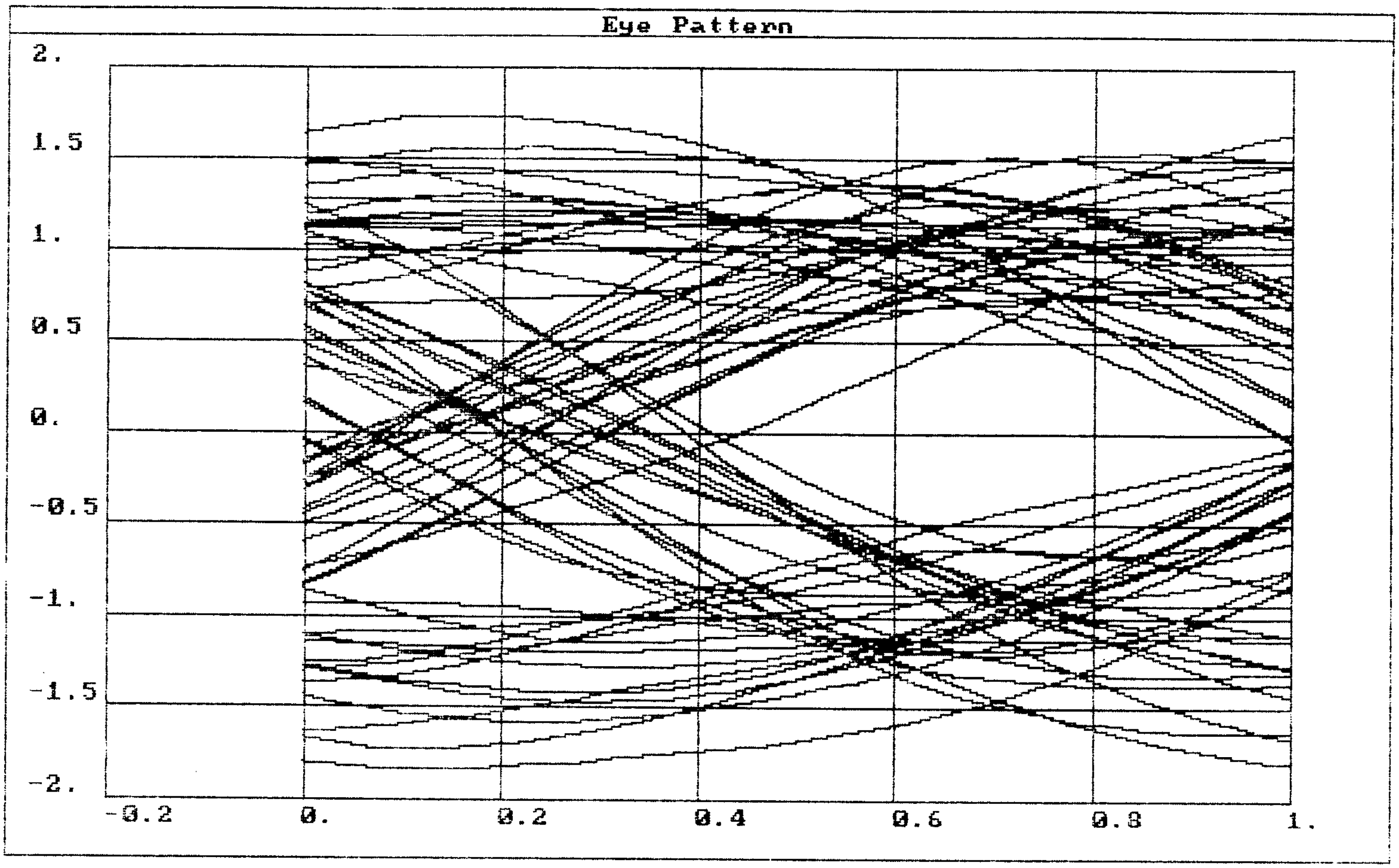
$$H(f) = H_{MF}(f)\left[j2\pi f - \sum_{\substack{m=1 \\ =-1 \\ \text{only}}} \frac{\dot{r}(mT)}{r(0)} e^{-j2\pi f mT} \right]$$

N=3 Butterworth

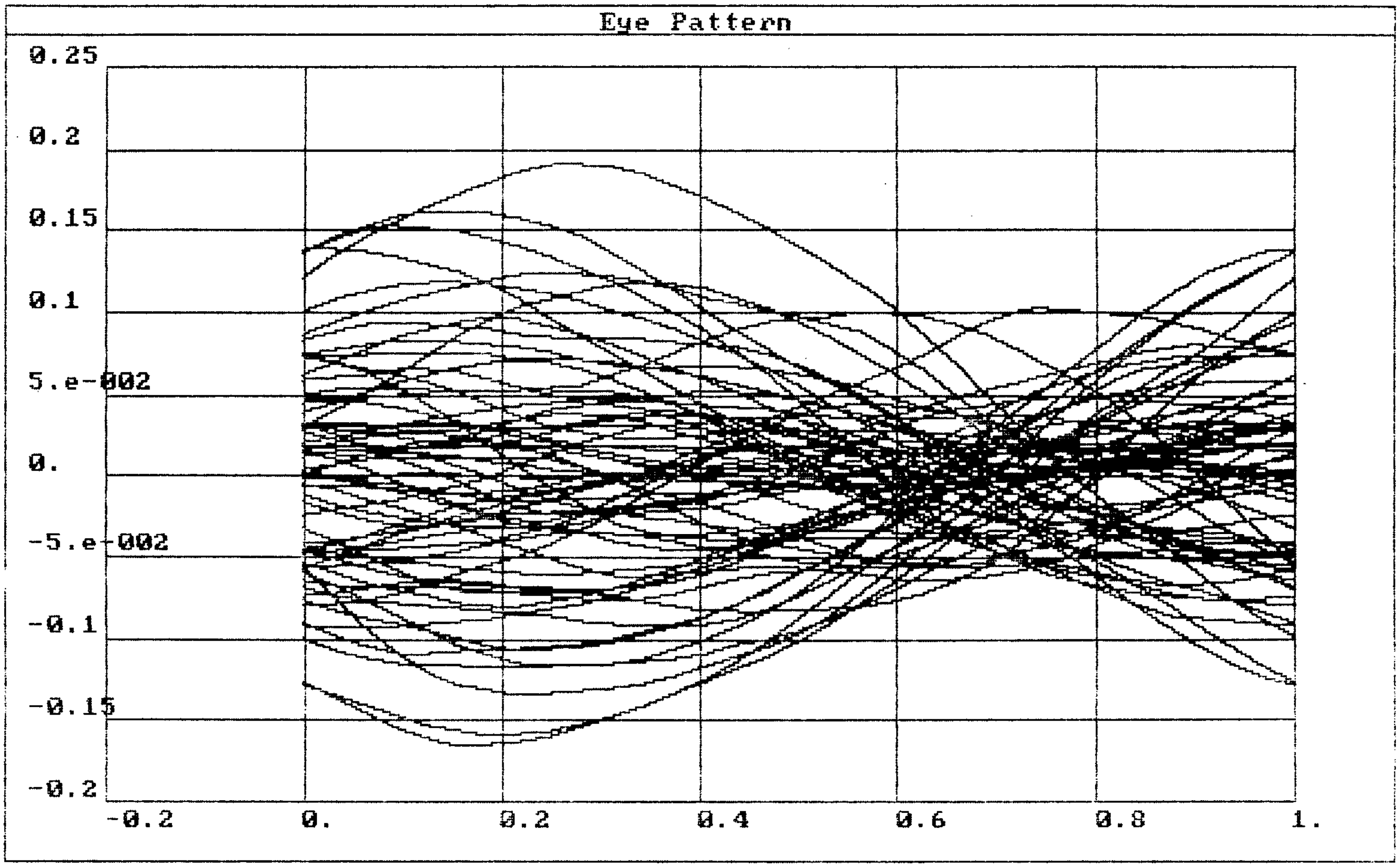
Approximated with $1 - e^{-s\Delta}$

$\dot{r}(\pm T)$ taken as roughly $1/2$

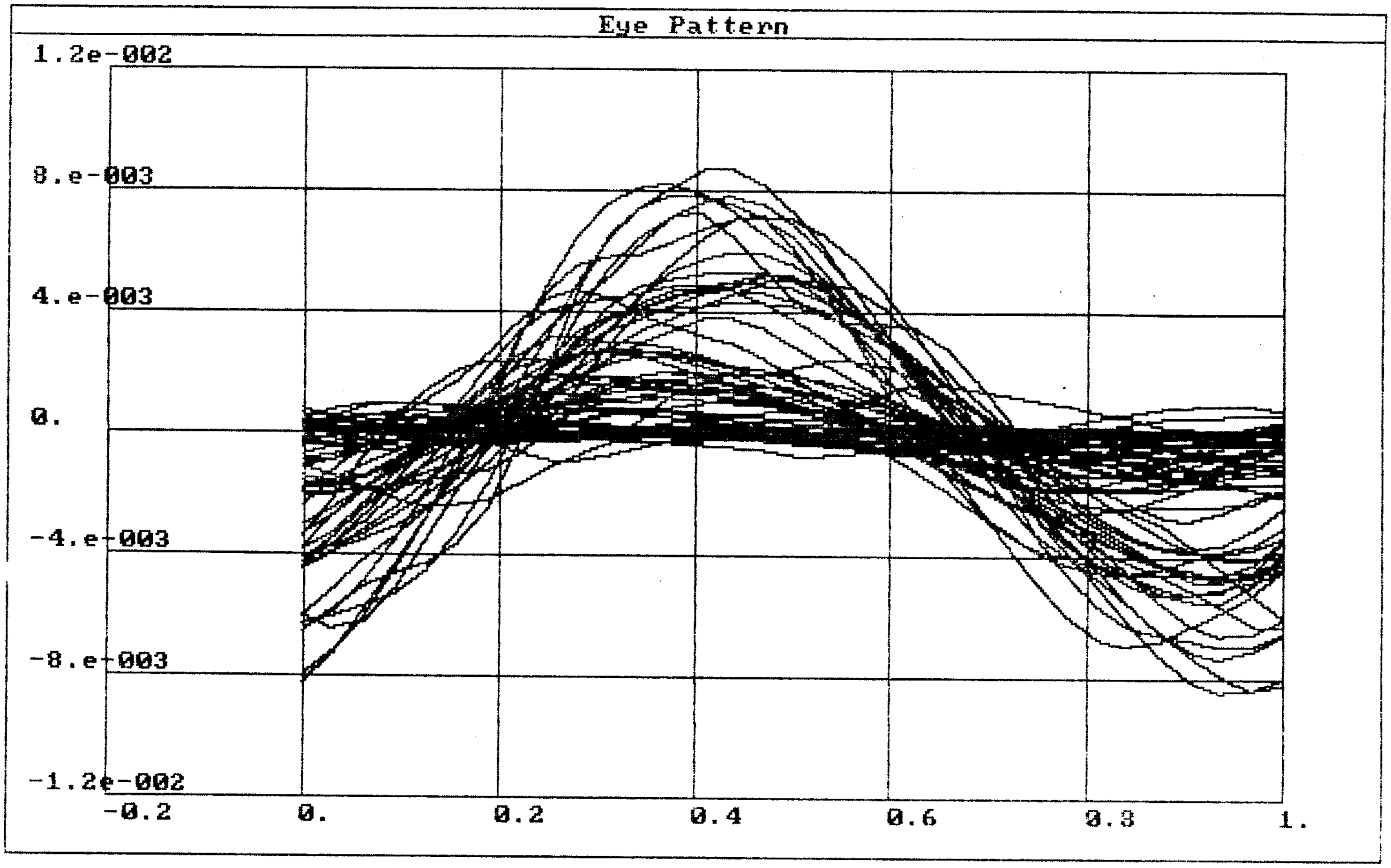
No Noise



$E_b/N_0 = 10$ dB Matched Filter Eye Pattern



Eb/No = 10 dB   Timing Filter Output



$E_b/N_0 = 15\,\text{dB}$

Timing Filter thru X^2 & pseudo-differentiator

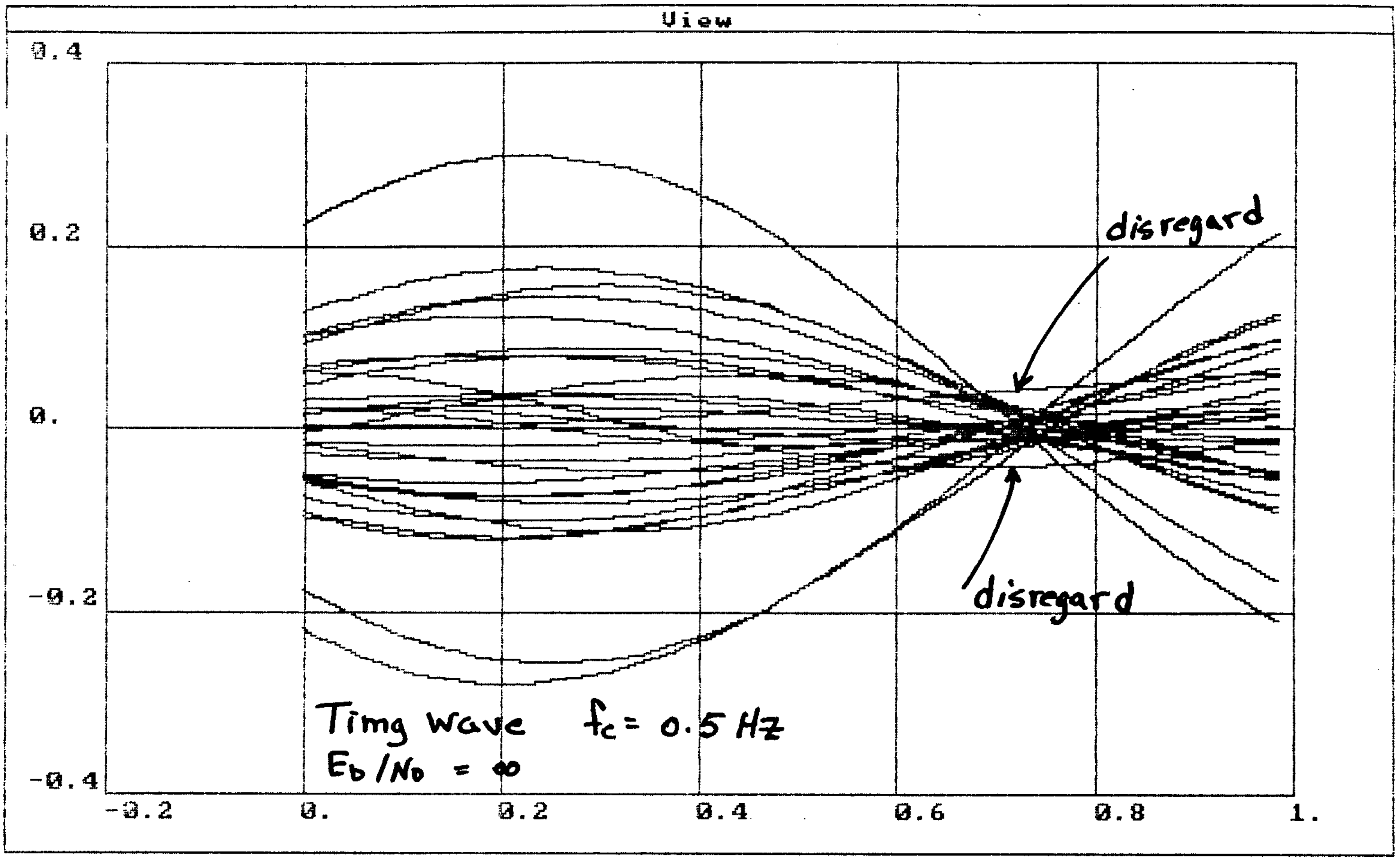
```
Matrix Entered was:

   0.99500   0.07030   0.00511  -0.00108   0.00000
  -0.07167   0.99500   0.07030   0.00511  -0.00108
  -0.00169  -0.07167   0.99500   0.07030   0.00511
   0.00951  -0.00169  -0.07167   0.99500   0.07030
   0.00000   0.00951  -0.00169  -0.07167   0.99500
LU Factored Matrix Follows :

    0.9950    0.0703    0.0051   -0.0011    0.0000
   -0.0720    1.0001    0.0707    0.0050   -0.0011
   -0.0017   -0.0715    1.0001    0.0707    0.0050
    0.0096   -0.0024   -0.0716    1.0001    0.0707
    0.0000    0.0095   -0.0024   -0.0715    1.0001
Now, enter source vector to finally solve for solutions
Enter components of source vector, each followed by a return
-0.007019
0.070590
-0.001381
-0.078427
0.019935
Solutions :
      -0.01212       0.06985       0.00913      -0.07890       0.01370
```

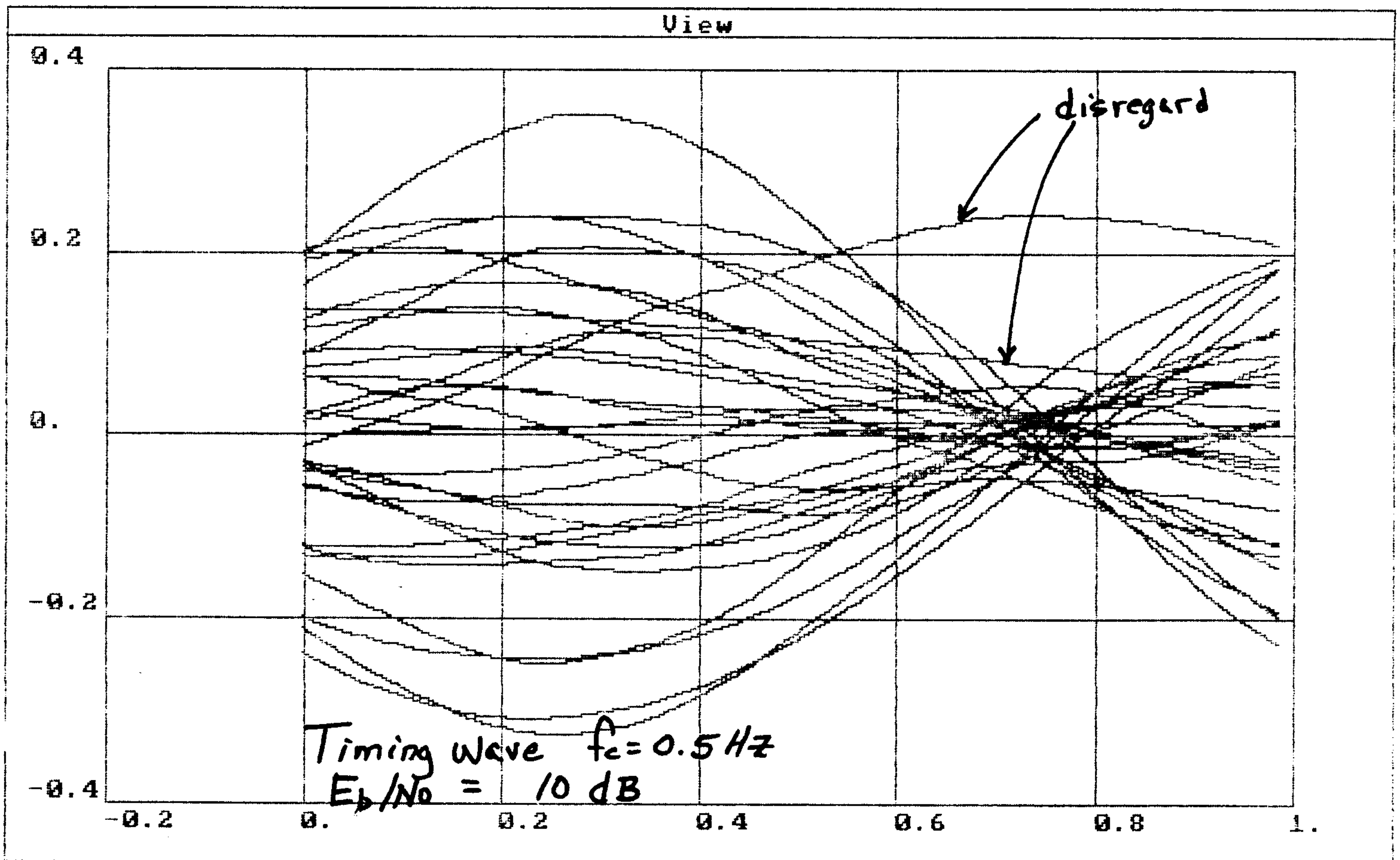
Computed tap values

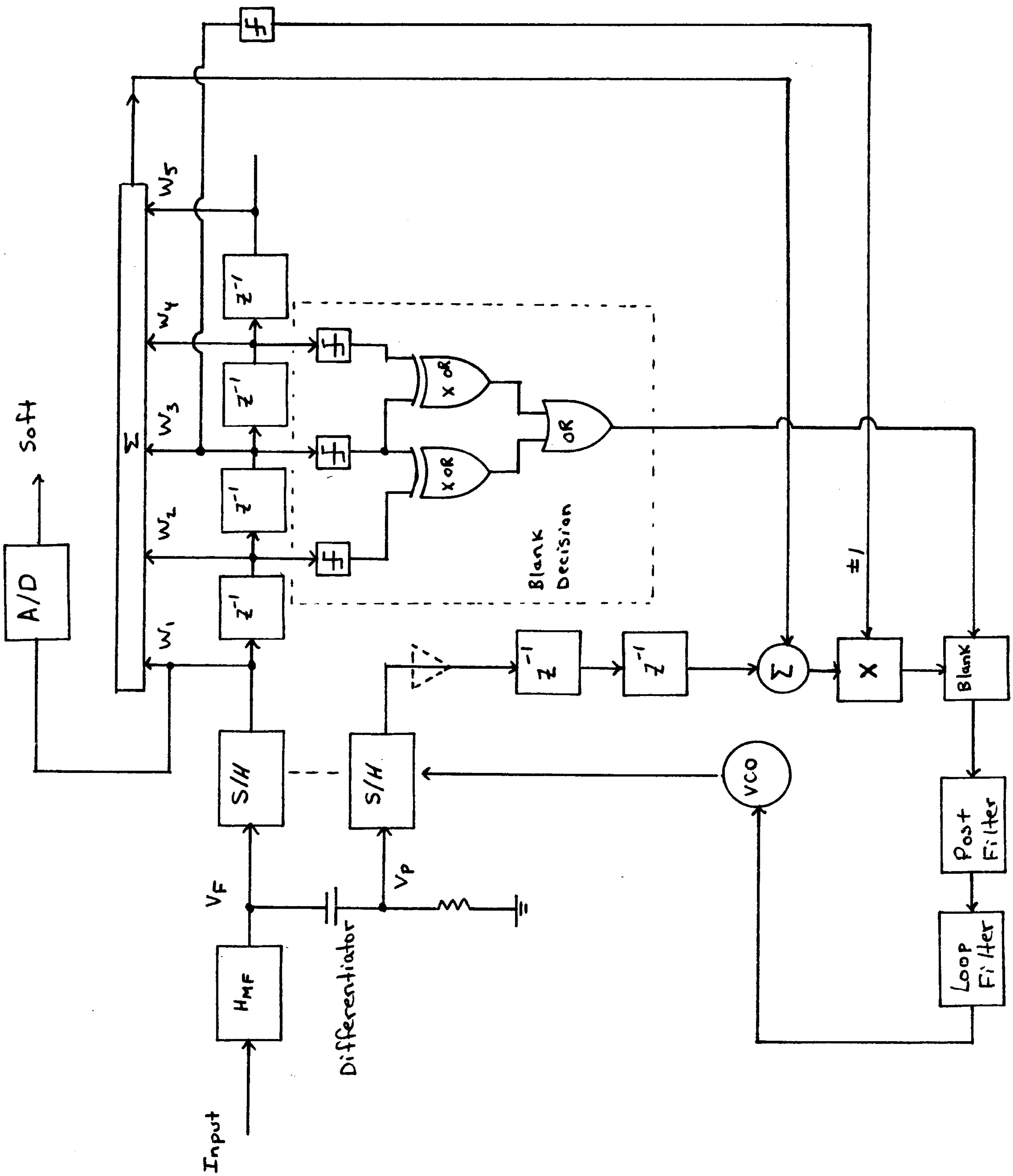
	$\tilde{g}$	$\dot{\tilde{g}}$ (scaled)
-3T	-0.00108	-0.002409
-2T	0.005114	-0.007019
-T	0.070304	0.070590
0	0.994996	-0.001381
T	-0.071673	-0.078427
2T	-0.001688	0.019935
3T	0.009515	-0.002418

Input to Sim 2 pgm

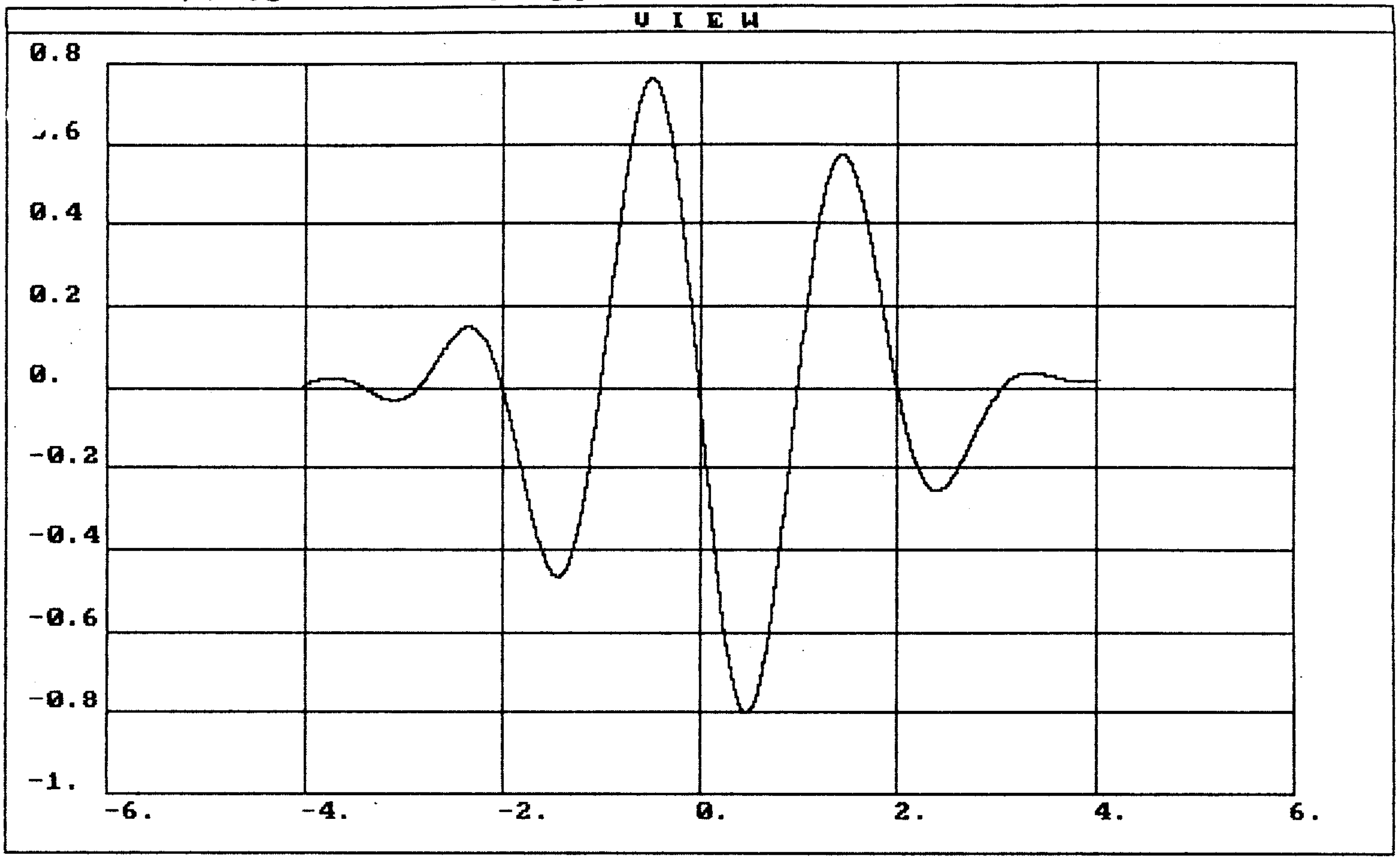
1.0
-0.01370
0.07890 (0.075)
-0.00913
-0.06985
0.01212


View
0.4
0.2
0.
-0.2
-0.4
-0.2
0.
0.2
0.4
0.6
0.8
1.
disregard
disregard
Timg wave $f_c = 0.5$ Hz
$E_b/N_0 = \infty$

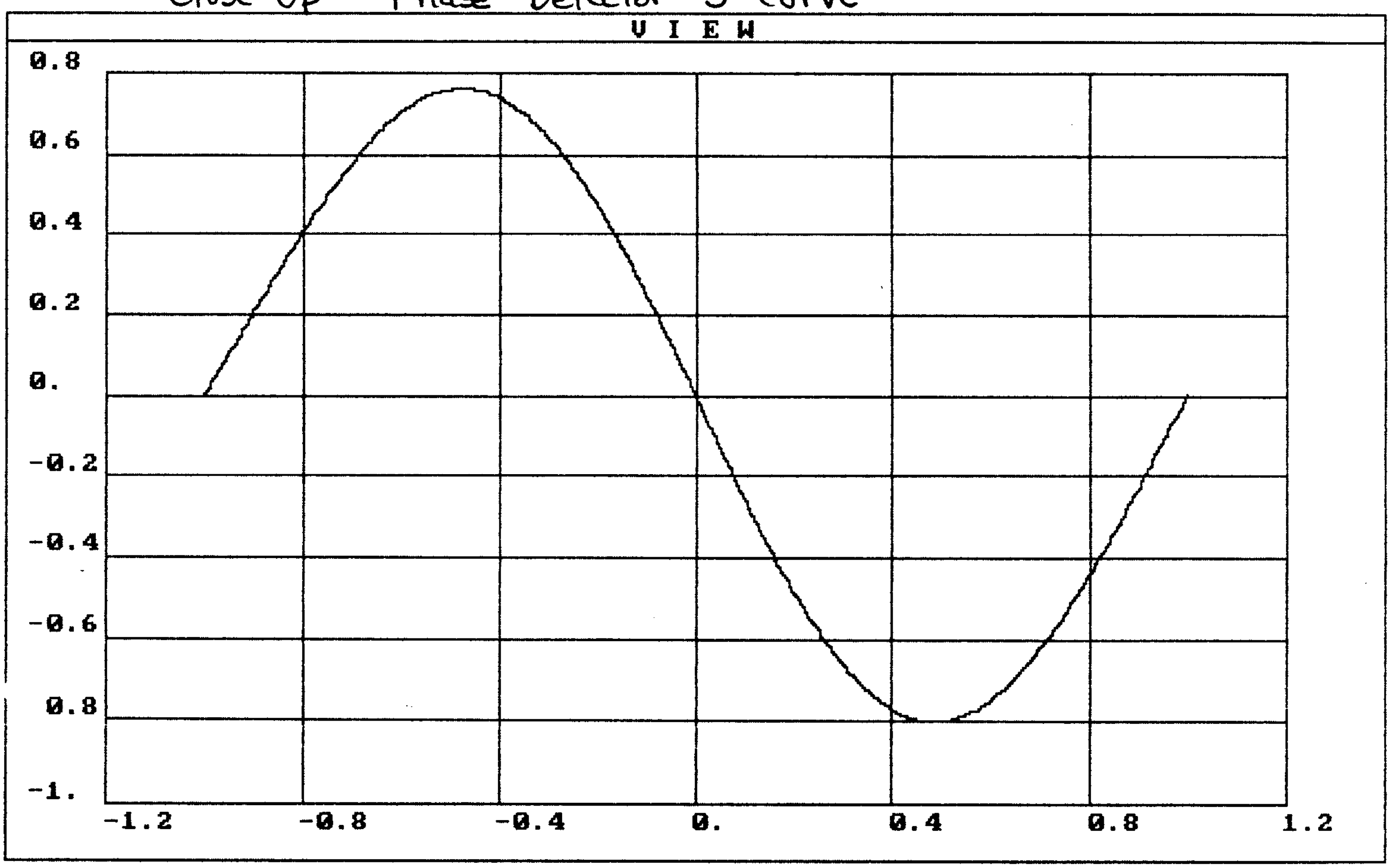

View
0.4
0.2
0.
-0.2
-0.4
-0.2
0.
0.2
0.4
0.6
0.8
1.
disregard
Timing wave $f_c = 0.5$ Hz
E_b/N_0 = 10 dB


Input
H_{MF}
Differentiator
V_F
V_P
S/H
S/H
VCO
A/D
Soft
Σ
W_1
W_2
W_3
W_4
W_5
z^{-1}
XOR
XOR
OR
Blank Decision
±1
Σ
X
Blank
Post Filter
Loop Filter

Phase Detector S- Curve



Close-Up Phase Detector S-Curve



- Analysis of the MML approach is greatly simplified compared to the MMSE approach because it is much more linear in nature.

- The MML approach relies heavily upon the employed pulse shape

- For higher data rates, the necessity of a high-speed tapped delay line exclude its use at present in an all-analog implementation. (intermediate rates)

In conclusion:

High performance bit synchronization at low E_b/N_0 is technically difficult and multi-disciplined making hasty assessments ill-advised.

The same detailed analysis <u>must</u> permeate the actual hardware design.

Be keenly aware of the virtues of hybrid designs which employ a mixture of analog and digital techniques.

References

1] L.E. Franks, "Carrier and Bit Synchronization in Data Communications- A Tutorial Review", IEEE COM-28, Aug. 1980

2] F.M. Gardner, "Self-Noise in Synchronizers" IEEE COM-28 Aug. 1980

3] W.A. Gardner, L.E. Franks, "Characterization of Cyclo-Stationary Random Signal Processes", IEEE IT-21 Jan. 1975

4] M.H. Meyers, L.E. Franks, "Joint Carrier Phase and Symbol Timing Recovery for PAM Systems" IEEE COM-28 Aug. 1980

5] L.E. Franks, J.P. Bubrouski, "Statistical Properties of Timing Jitter in a PAM Timing Recovery Scheme", IEEE COM-22 July, 1974

6] B.R. Saltzberg, "Timing Recovery for Synchronous Binary Data Transmission", BSTJ March, 1967

7] D.L. Duttweiler, "The Jitter Performance of Phase-Locked Loops Extracting Timing from Baseband Data Waveforms", BSTJ Jan. 1976

8] A.L. Mc Bride, A.P. Sage, "Optimum Estimation of Bit Synchronization", IEEE AES-5 May, 1969

9] C.R. Hogge, "A Self-Correcting Clock Recovery Circuit" IEEE ED-32 Dec. 1985

10] W.J. Hurd, T.O. Anderson, "Digital Transition Tracking Symbol Synchronizer for Low SNR Coded Systems" IEEE COM-18 April, 1970

11] Moeneclaey, " A Comparison of Two Types of Symbol Synchronizers for which Self-Noise is Absent" , IEEE COM-31 Mar. 1983

12] Moeneclaey, " The Optimum Closed-Loop Transfer Function of a Phase-Locked Loop Used for Synchronization Purposes" IEEE COM-31 April 1983

13] Moeneclaey, " The Influence of Four Types of Symbol Synchronizers on the Error Probability of a PAM Receiver" IEEE COM-32 Nov. 1984

14] Moeneclaey, " Two Maximum-Likelihood Symbol Synchronizers with Superior Tracking Performance" IEEE COM-32 Nov. 1984

15] E.Y. Ho, Y.S. Yeh, " A New Approach for Evaluating the Error Probability in the Presence of Intersymbol Interference and Additive Gaussian Noise", BSTJ Nov. 1970

16] C. Helstrom, " Calculating Error Probabilities for Intersymbol and Cochannel Interference", IEEE COM-34 May, 1986