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"Design Tools & Caveats for Frequency Synthesizer Design"

Introduction

Take a seasoned RF/microwave designer who has a command of basic control theory along with an insight into analog and digital electronics, include an understanding of communication systems concepts, and you have a frequency synthesizer designer. Perhaps in no other area of what is traditionally called RF/microwave design is "top-level-down" system design as important because so many design parameters are hopelessly interwoven. All too frequently in synthesizer design, substantial topology changes must be made in the final design, or a "golden filter" must be invented late in the prototyping effort in order to hopefully reach the final design goals; and these are the more fortunate instances.

Most of the recent synthesizer trade literature deals with either direct digital synthesis (DDS) or indirect synthesis which is more commonly known as synthesis by phase-lock. In the greater view of frequency synthesizer design, these are only two modicums in the complete picture.

The Total Picture

Frequency synthesizer designs are driven by performance specifications which typically originate from a system designer. Because the synthesizer is often the most costly analog/RF item in modern digital radios, it is prudent to involve the synthesizer designer and radio frequency plan designer early in the development. Without this interaction, TBDs (to be determined) often go through a metamorphosis, appearing later as very difficult requirements (e.g. -95 dBc spurs, 0.2 usec swithing time) which may not in truth be required, or which with proper system reallocations, could be eased.

Different frequency plan architectures which in the end accomplish the same final objective may in fact result in monumental differences in synthesizer complexity and cost. The tendency to make the synthesizer "one block" in the overall block diagram should be resisted strongly because this is almost always a dramatic understatement of the problem solution.

Other systems level parameters such as supply voltages, choice of reference frequencies, control interfaces, etc. should also be addressed by the synthesizer designer early in the design effort. In general, since interfaces by definition involve other areas or modules in the system, the synthesizer designer should freeze good design concepts into these areas as early as possible.

Design Tools

A minimum of four basic analysis tools are required in my estimation to adequately address the complex synthesizer design task:

i) Mixer spur analysis program
ii) System phase noise analysis program
iii) Phase-locked loop transient analysis/stability analysis
iv) Filter performance analysis tool

The mixer spurious analysis tool is necessary because multiple frequencies will be combined using mixers in more complex designs. Diligent effort must be applied to guarantee that these spurs do not cause spurious synthesizer outputs. Although the overall synthesizer phase noise performance can be calculated using a spreadsheet, I prefer the use of a customized program for that purpose which automatically has embedded models for phase-locked loops, digital dividers, etc. If indirect synthesis is to be used within the synthesizer, the designer must be cognizant of the achievable trades between switching speed, sampling spur levels, and phase noise. Initial estimates of what is achievable can be obtained from the third tool. Finally, any complex synthesizer requires filters. The fourth tool allows the designer to quickly assess achievable filter characteristics assuming finite component Q. These tools must be used iteratively to hone a final synthesizer frequency plan from which the more detailed design may be launched.

Phase-locked Loop Stability and Transient Analysis

The information presented herein will only attempt to address narrow aspects of the third design tool area as each of the other areas is suitable for a separate stand-alone discussion themselves. Most of the results presented have not been published to the best of my knowledge. The article will conclude with some well deserved caveats for synthesizer designers.

Frequency domain and time domain analyses are required to fully characterize a phase-locked loop design. Stability issues are most clearly seen using frequency domain analysis whereas switching speed is evaluated from a time domain analysis. The output phase noise performance of the synthesizer may be computed by using elements of the frequency domain analysis.

Typically, one of four mathematical descriptions of the linearized control loop is employed:

i) Laplace transforms
ii) Z transforms
iii) Simultaneous differential equations
iv) Simultaneous finite difference equations

Strictly speaking, methods i) and iii) are only valid for continuous systems and methods ii) and iv) are only valid for sampled control systems. As the ratio of loop bandwidth to reference frequency decreases, all four descriptions converge to the same generalized result. Since most synthesis applications make use of digital phase detectors and/or dividers, the sampled control system description is the primary focus of the following discussion.

Z-transform Problem Formulation

A number of articles have addressed the usage of Z transforms to describe sampled control systems [4],[5],[7],[12],[15]. In general, the Laplace transform description of the open-loop gain is transformed into its "equivalent" Z-transform by first expanding the Laplace transform into partial fractions and then converting each term into its "equivalent" Z-transform. The word "equivalent" here is used in a non-rigorous sense. Some precautions in making this transformation must be observed as discussed in [4]. If a time delay is part of the open-loop gain function, this may be accomodated by using modified-Z transforms [4].

The time domain response is obtained by inversion of the Z-transform much as done with Laplace transforms. Inversion of the Z-transform may be done by the method of residues (which first involves solving for all of the denominator roots) or by simple repeated long-hand division which is of course much more simple. Stability analysis involves computing the root locations of the system characteristic function and determining if any lie outside the unit circle.

The Z-transform system description unfortunately suffers from numerical instabilities as the order of the system being analyzed increases due to finite computer numerical precision. The problem is particularly acute unless all denominator factors of (Z-1) are factored out of the denominator polynomial and handled separately. These numerical problems generally arise for system orders greater than roughly 5 or 6 but can vary significantly. For higher-order systems, implicit problem formulations which are discussed later provide higher quality, numerically stable solutions.

Specific Solutions

In the early stages of synthesizer design, design guidelines are much more helpful than are long and tedious precise results. The detailed analysis is simply deferred until a plausible design solution appears near.

The six basic phase-locked loop cases which are considered address most of the initial design situations which may result. The six basic configurations are shown in Table I.

Table I: Basic Phase-locked Loop Cases

	Loop Type	Phase Detector Type	Delays	Sampling Efficiency
1.	I	Sample/Hold	No	No
2.	I	Sample/Hold	Yes	Yes
3.	II	Sample/Hold	No	No
4.	II	Sample/Hold	Yes	Yes
5.	II	Phase/Freq. Hi-Z	Yes	N/A
6.	II	Phase/Freq. Lo-Z	Yes	N/A

Three phase detector types are included in Table I; the sample-and-hold phase detector, the phase/frequency detector with high-impedance output, and the phase/frequency detector with low-impedance output. Each of these phase detectors is described in more detail in Figure 1. Some of the design configurations allow inclusion of non-zero loop time delays or finite sampling efficiency (sample/hold types only) as noted in Table I.

The initial design cases given in Table I have been purposely kept simple in order to streamline initial design estimates. They impose a minimum number of design unknowns upon the designer's efforts yet yield very good results. The inclusion of time delay in the modeling equations is particularly valuable because it allows the presence of additional filters (which are typically used to further reduce sampling spurs) to be largely accounted for by simple inclusion of their low frequency group delay in this term.

The design equations for the first four configurations are collectively shown in Figure 2. A number of common variables which are used throughout are defined below.

Common Variables

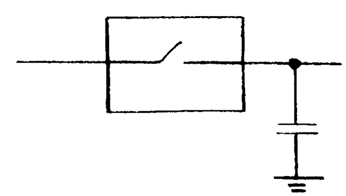
Kd	Phase detector gain, volts/radian
Kv	VCO gain, radian/second/volt
N	Feedback divider ratio
T	Reference period, seconds
K	Combined gain term equal to Kd Kv T/N
Ws	Reference frequency, radians/second (2 pi / T)
^f	Step change in synthesizer output frequency, Hz
0e	VCO output phase error, radians,

Although closed-form solutions may be found for the final two configurations, the complexity of the solutions masks any directly visible insight into the problem and these solutions are therefore not presented here. Owing to the necessary phase detector approximations used in the final two configurations, it suffices to select the post-detection filter time constants such that zero-order sample-hold behavior is closely emulated and the analysis conducted as for configuration 4 [15].

The equations presented in Figure 2 are valid only for linear phase-locked loop operation. Gain margin is presented only for the ideal type I and II cases because phase margin more accurately describes the decrease in system stability given the

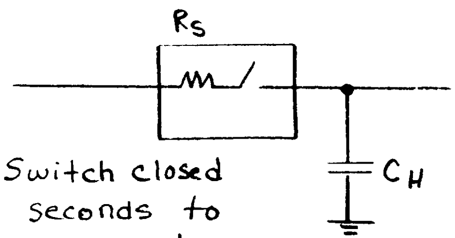
Figure 1 Phase Detector Types

a. Ideal Sample-Hold



$$H(s) = \frac{1-e^{-sT}}{s}$$

b. Inefficient Sample-Hold
[12], p. 126



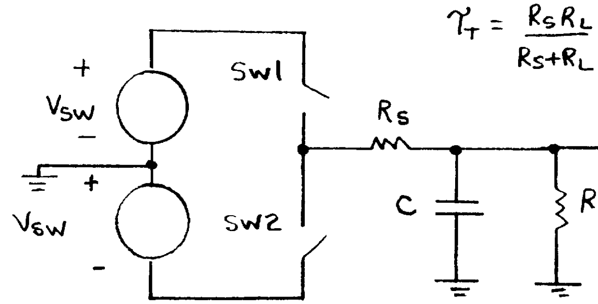
Switch closed τ_S seconds to take sample

$$\tau_c = R_S C_H$$

$$H(s) = \frac{1-e^{-sT}}{s} \frac{e^{sT}(1-A)}{e^{sT}-A}$$

$$A = e^{-\tau_S/\tau_c}$$

c. Phase/Frequency Detector
in ϕ-det. mode
Tri-state output
[6]

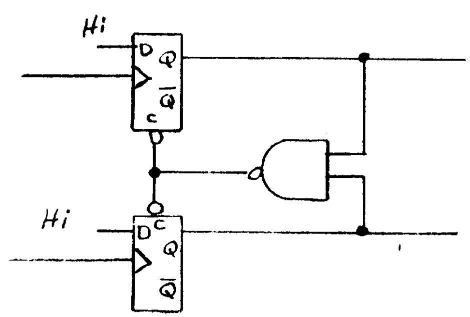


$$\tau_T = \frac{R_S R_L}{R_S+R_L} C \gg T \qquad \tau_1 = R_L C$$

$$H(s) \sim \frac{K_d}{s\tau_T + \frac{\tau_T}{\tau_1}} \frac{1}{1-e^{-sT} e^{-T/\tau_1}}$$

$$K_d = \frac{V_{SW} R_1}{2\pi (R_1+R_3)}$$

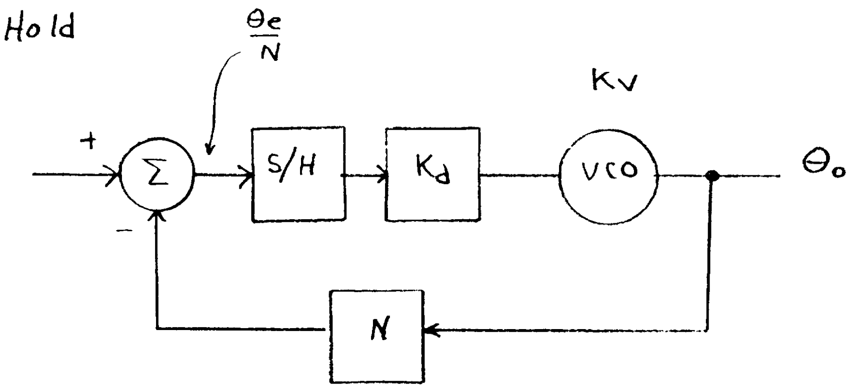
d. Phase/Frequency Detector
in ϕ-det. mode
Low-Impedance Output



$$H(s) = K_d$$

$$K_d = \frac{V_{High}}{2\pi}$$

Figure 2.1 Ideal Type I Sample-Hold



$$G_{OL}(s) = \frac{K_d}{N}\,\frac{1-e^{-sT}}{s}\,\frac{K_v}{s}$$

$$G_{OL}(z) = \frac{K}{z-1}$$

$$\theta_e(nT) = \frac{2\pi\Delta f T}{K}\left[1-(1-K)^n\right] \text{ Rad.}$$

$$\text{Gain Margin} = -20\log\left[\pi\,\frac{\omega_n}{\omega_s}\right] \text{ dB}$$

$$\omega_n = \frac{K_d K_v}{N}$$

$$\text{Phase Margin} = \operatorname{Tan}^{-1}\left[\sqrt{\frac{4}{K^2}-1}\right]$$

Phase Noise

$S_v(\omega) = \widetilde{\theta^2_{VCO}(\omega)}$ VCO Self-noise

$S_{RN}(\omega) = \widetilde{\theta^2_{RN}(\omega)}$ Reference Noise

$S_o(\omega) = \widetilde{\theta^2_o(\omega)}$ Output Noise

Units Rad^2/Hz

$\sim$ denote statistical average

Notes

1) Phase lock achieved in one sample for $K=1$

Gain Margin = 6 dB

Phase Margin = 60°

2) Reference and VCO power spectral density transfer functions

Ref: $$\frac{S_o(\omega)}{S_{RN}(\omega)} = \frac{16K^2N^2\sin^4(\omega T/2)}{(\omega T)^4\left(K^2+2-2K+2(K-1)\cos\omega T\right)}$$

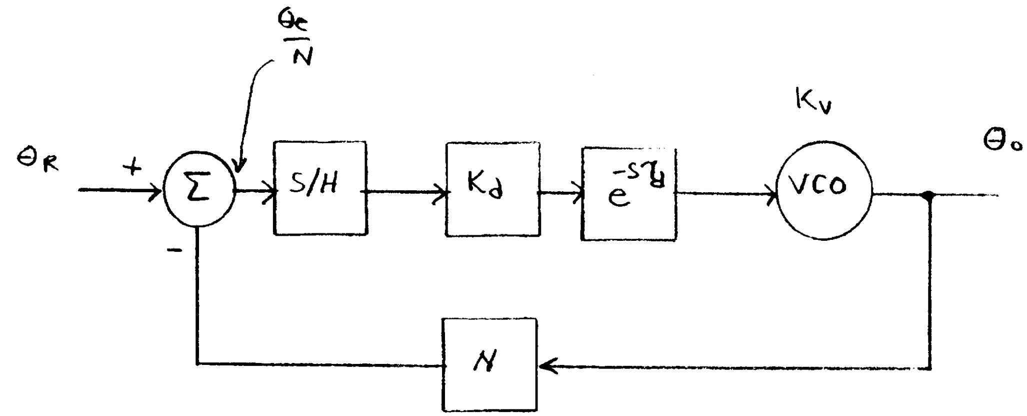
$$= N^2\left[\frac{\sin(\omega T/2)}{(\omega T/2)}\right]^4 \quad \text{for } K \equiv 1$$

VCO: $$\frac{S_o(\omega)}{S_{VCO}(\omega)} = \frac{4\sin^2(\omega T/2)}{K^2+2-2K+2(K-1)\cos\omega T}$$

$$= 4\sin^2\left(\frac{\omega T}{2}\right) \quad \text{for } K \equiv 1$$

Figure 2.2 Non-ideal Type I Sample-Hold

$$G_{OL}(s) = \frac{K_d}{N} \underbrace{\frac{1-e^{-sT}}{s} \frac{e^{sT}(1-A)}{e^{sT}-A}}_{\text{Inefficient Sample-hold}} \underbrace{e^{-s\tau_d}}_{\text{Time Delay}} \frac{K_v}{s}$$



$$G_{OL}(z) = K(1-A) \frac{mz+(1-m)}{(z-A)(z-1)}$$

$$m = 1 - \frac{\tau_d}{T} \; ; \quad 0 < m \leq 1$$

$$\theta_e(z) = \frac{2\pi \Delta f T z \, (z-A)}{z^3 + \alpha z^2 + \beta z + \gamma}$$

$$\alpha = K(1-A)m - 2 - A$$

$$\beta = 1 + 2A + K(1-A)(1-2m)$$

$$\gamma = -A - K(1-A)(1-m)$$

$$\text{Phase Margin} = 180^\circ - \tan^{-1}\left[my,\, 1+mx-m\right] - \tan^{-1}\left[y,\, x-A\right] - \tan^{-1}\left[y,\, x-1\right]$$

where $x = \text{Real Part}[z]$

$y = \text{Imag Part}[z] = \sqrt{1-x^2}$

and x satisfies

$$4Ax^2 - x\left[2+2A^2+4A+L^2 m(1-m)\right] + \left[2+2A^2 - L^2\left(m^2+(1-m)^2\right)\right] = 0$$

$$L^2 = K^2(1-A)^2$$

Figure 2.3 Ideal Type II Sample-Hold

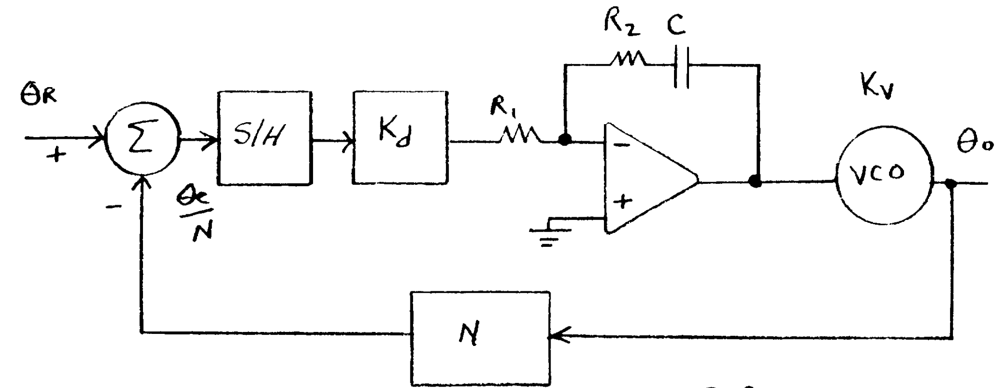
$$G_{OL}(S) = \frac{K_d}{N}\,\frac{1-e^{-ST}}{S}\,\frac{1+S\tau_2}{S\tau_1}\,\frac{K_V}{S}$$

$$G_{OL}(z) = \frac{K}{\tau_1}\,\frac{z\left(\frac{T}{2}+\tau_2\right) + \left(\frac{T}{2}-\tau_2\right)}{(z-1)^2}$$

$$\theta_e(z) = \frac{2\pi\Delta f T z}{z^2 + z\left(\frac{aK}{\tau_1}-2\right) + \left(1+\frac{Kb}{\tau_1}\right)}$$

where $a = \frac{T}{2} + \tau_2$

$b = \frac{T}{2} - \tau_2$



$\tau_1 = R_1C$

$\tau_2 = R_2C$

$$\text{Gain Margin} = -20\log\left[2\pi\zeta\frac{\omega_n}{\omega_s}\right]$$

where $\zeta = \frac{1}{2}\omega_n\tau_2$

$$\omega_n = \left(\frac{K_d K_V}{N\tau_1}\right)^{1/2}$$

$$\omega_s = \frac{2\pi}{T}$$

$$\text{Phase Margin} = 180^\circ + \text{Tan}^{-1}\left[ay, ax+y\right] - 2\,\text{Tan}^{-1}\left[y, x-1\right]$$

where $x = 1 + \frac{ab}{4}\left(\frac{K}{\tau_1}\right)^2 - \frac{KT}{4\tau_1}\sqrt{\left(\frac{Kab}{\tau_1}\right)^2+4}$

$y = \sqrt{1-x^2}$

Notes:

1) Dead beat response possible for

$\zeta = 0.75$

$\omega_n = \frac{1}{T}$

2) For dead-beat response case, Gain Margin is only

$$GM = -20\log\left[\frac{3}{4}\right] = 2.499\ dB$$

Figure 2.4   Non-ideal Type II Sample-Hold

$$G_{OL}(s) = \frac{K_d}{N} \; \frac{1-e^{-sT}}{s} \; \frac{e^{sT}(1-A)}{e^{sT}-A} \; \frac{1+s\tau_2}{s\tau_1} \; e^{-s\tau_d} \; \frac{K_v}{s}$$

$$G_{OL}(z) = \frac{K}{\tau_1}(1-A)\frac{1}{z-1}\;\frac{\alpha z^2+\beta z+\gamma}{(z-1)^2}$$

where

$$\alpha = T\frac{m^2}{2} + \tau_2 m$$

$$\beta = \frac{T}{2}\left(2m-2m^2+1\right)+\tau_2-2\tau_2 m$$

$$\gamma = \frac{T}{2}(m-1)^2-\tau_2+\tau_2 m$$

$$m = 1-\frac{\tau_d}{T} \; ; \quad 0 < m \le 1$$

$$\theta_e(z) = \frac{2\pi\Delta f T z (z-A)}{z^3+d_2 z^2+d_1 z+d_0}$$

where

$$d_2 = -2-A+\frac{K}{\tau_1}(1-A)\alpha$$

$$d_1 = 1+2A+\frac{K}{\tau_1}(1-A)\beta$$

$$d_0 = -A+\frac{K}{\tau_1}(1-A)\gamma$$

inclusion of inefficient sampling and internal time delays.

Closed-form solutions may also be valuable where loop performance must be evaluated many times such as in a Monte-Carlo analysis used to investigate design value tolerances. This type of assessment provides some initial insight into achievable performance over production quantities. The results of a typical Monte-Carlo analysis of a type II phase-locked loop are shown in Figure 3.

In general, closed-form solutions for higher-order systems are at best tedious and very prone to numerical instabilities due to finite arithmetic precision. Implicit methods provide a powerful macroscopic analysis tool for more complicated systems.

Macroscopic Phase-Locked Loop Analysis

Macroscopic modeling of phase-locked loop behavior is useful because it allows a designer to consider only primary block diagram level details during the design phase rather than be immediately plunged into device-level details. Further details may be added to the model once a final solution is near.

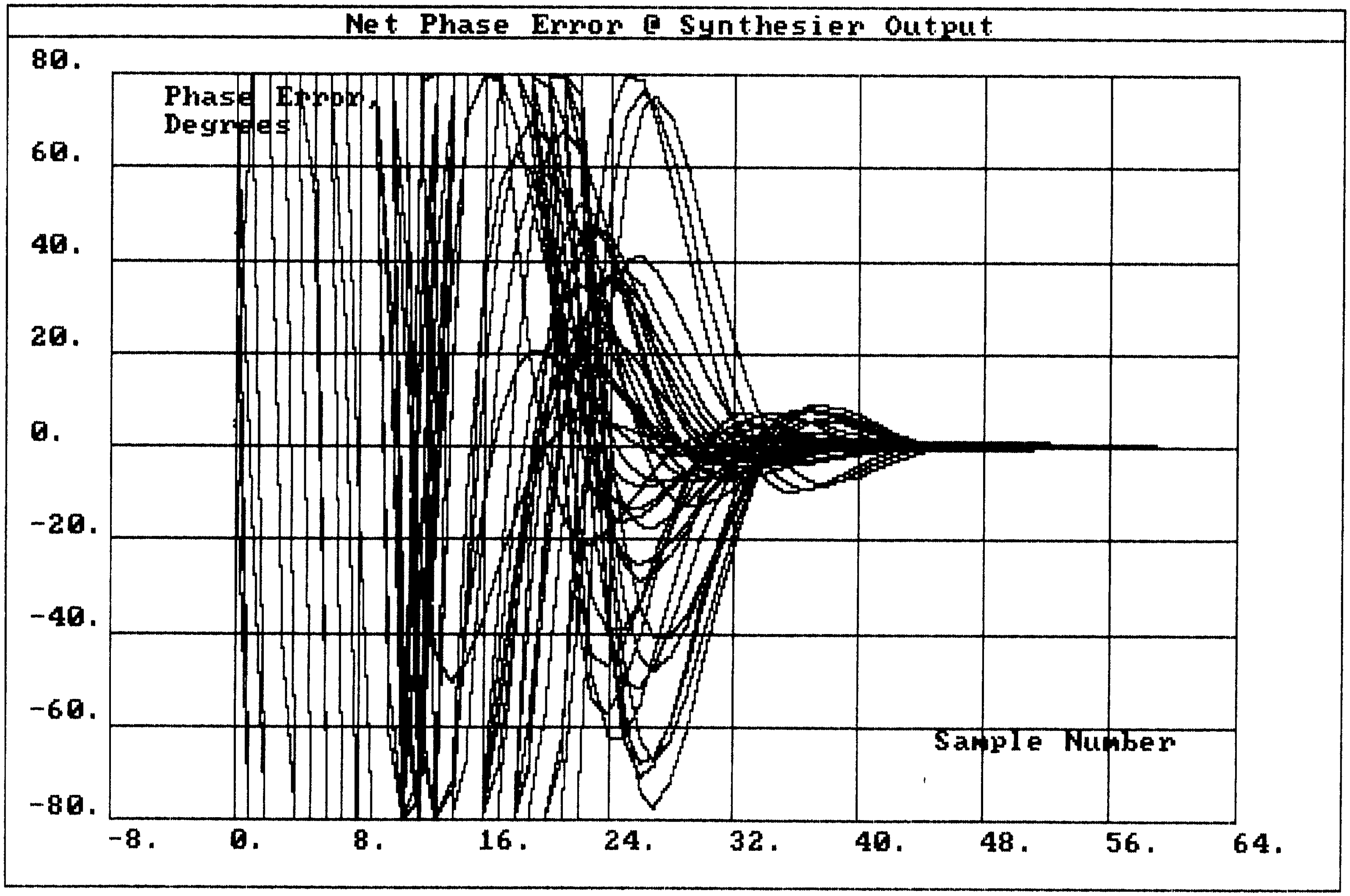
In order to make the analysis tool as flexible as possible, a nodal description of the network should be used and a library of standard circuit elements provided. With little loss of generality, an admittance description of the network may be used to completely describe the phase-locked loop as will be discussed shortly. Exploitation of what are called companion models for the basic block elements allows an implicit network equation formulation to be used (which is much easier to formulate than is explicit and also has many desirable numerical accuracy benefits [16]).

Companion models for the basic block diagram elements are shown in Figure 4. As is readily seen, the companion model formulation evolves about the numerical integration formula selected which in this case is the backward Euler formula. Although higher-order integration formulas such as the variable time step second-order Gear formula may look attractive, microscopic device details would have to be included in order to prevent the numerical algorithms from "ringing" in actual use. Since the iteration time step would have to be correspondingly small to accomodate the finite device slew-rates, the network simulation would be much more time consuming. Digital device slew rates are considered microscopic (compared to op-amp slew rates which are important macroscopic quantities) for the purposes of this discussion.

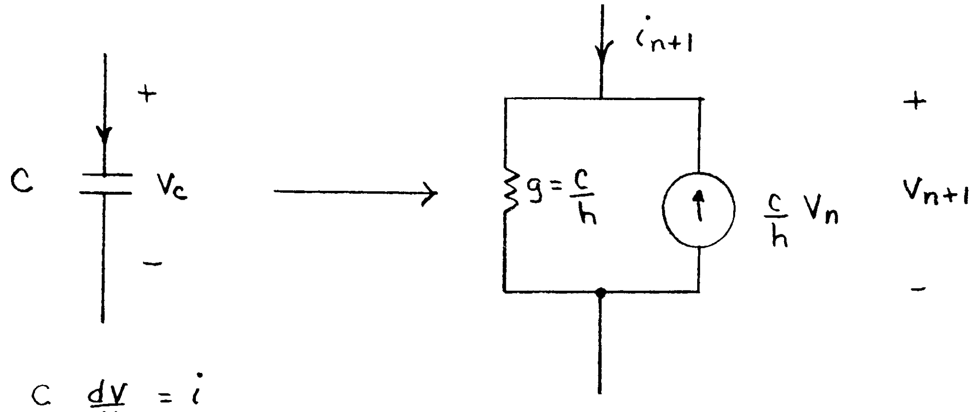
A number of desirable block diagram elements such as a voltage-controlled oscillator and ideal op-amp have been omitted from Figure 4 because they may be readily constructed from the basic elements presented. Other phase detector types such as the sample-and-hold variety can also be added.

The iterative computations which must be performed are quite straight forward. Once a circuit diagram for a given phase-locked loop has been created and entered in a nodal fashion, each component is replaced with its respective companion model. The

Figure 3. Type II Monte-Carlo Analysis



Capacitor

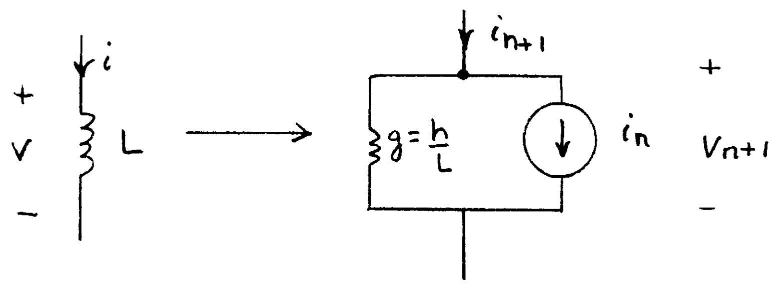


$$C \frac{dV}{dt} = i$$

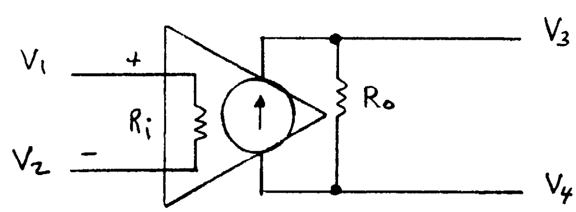
$$i_{n+1} = C V'_{n+1} \approx C \frac{V_{n+1} - V_n}{h} = \underbrace{\frac{C}{h} V_{n+1}}_{g} \underbrace{- \frac{C}{h} V_n}_{\text{source}}$$

$$h = t_{n+1} - t_n$$

Inductor



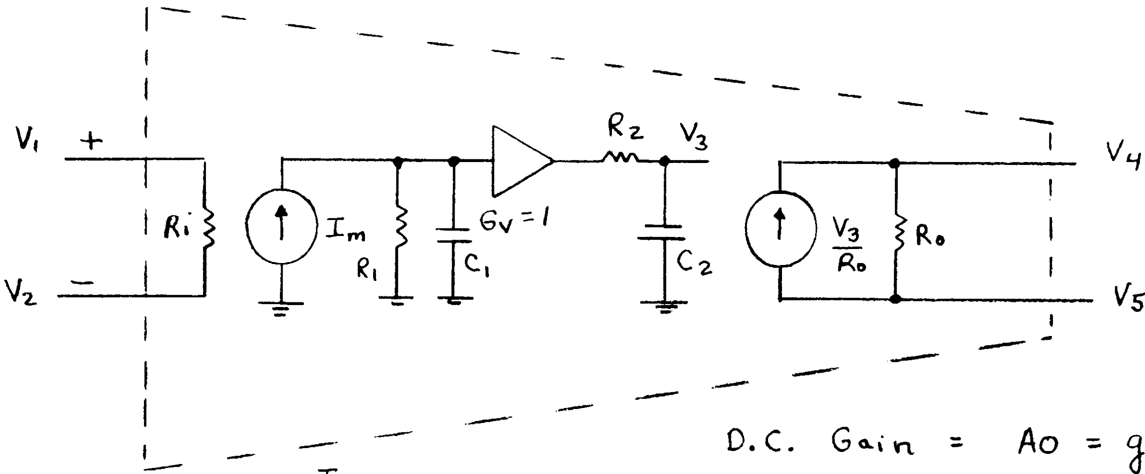
Voltage Follower

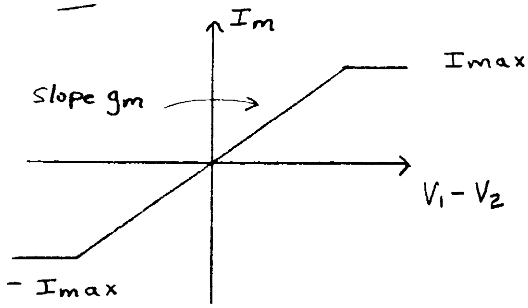


$\frac{AO}{R_o}(V_1 - V_2)$ where AO = D.C. Voltage Gain

Figure 4 Basic Companion Models

Op-Amp





D.C. Gain = $A_0 = g_m R_1$

Slew Rate $S = \frac{I_{max}}{C_1}$

Dominant Pole $W_1 = \frac{1}{R_1 C_1}$

$I_{max} = \frac{S}{R_1 W_1}$

Ideal Phase/Frequency Detector

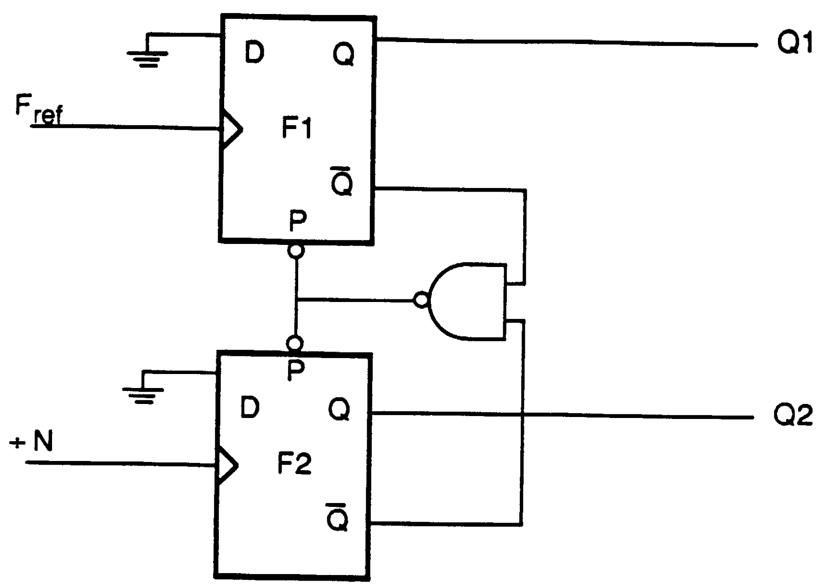


Figure 4 Continued

network node voltages and currents are then iteratively calculated as described in equation (1).

$$[Y] \; [V(t_{n+1})] = [I(t_n)] \quad (1)$$

Constant Network Conductance Matrix — Nodal Voltages at tn+1 — Companion Model Sources at tn

Frequency domain analysis proceeds in a similar manner. The network nodal description is used to create a floating admittance matrix description of the network [17] which is iteratively reduced to an equivalent two-by-two matrix from which the open-loop gain at a particular frequency is easily calculated. Given the open-loop gain at each frequency of interest, the closed-loop gain including sampling effects and transfer functions for VCO-related phase noise and reference-related phase noise may be calculated using the basic relationships derived in [4] and [5].

Design Example

The design example which will be presented employs a 2 MHz reference frequency and a low output impedance phase/frequency detector. An output third-order elliptic filter is included to further reduce sampling spurs at multiples of 2 MHz. The macroscopic model excluding VCO and feedback divider is shown in Figure 5. An OP-27 op-amp is used in the lead-lag filter with its respective finite slew-rate and rail-to-rail output voltage compliance range. The computed transient responses for two different loop parameter choices and slightly different post-detection filters are shown in Figures 6 and 7. The nonlinear double cycle-slip in Figure 6 is clearly apparent, being caused by inadequate bandwidth for the frequency hop magnitude executed. The relevant closed-loop gain functions pertaining to the topology used in Figure 7 are provided in Figures 8 and 9. These figures are useful for determining the phase-locked loop output phase noise spectrum [4].

Design Feasibility Guidelines

Although many parameters enter into synthesizer design, it is possible to arrive at some design guidelines which aid in quick trade-offs between switching speed and reference spurs. Only one loop filter configuration will be addressed as shown in Figure 10. The post-detection filter is chosen such that it is a

Model for Simulation Purposes

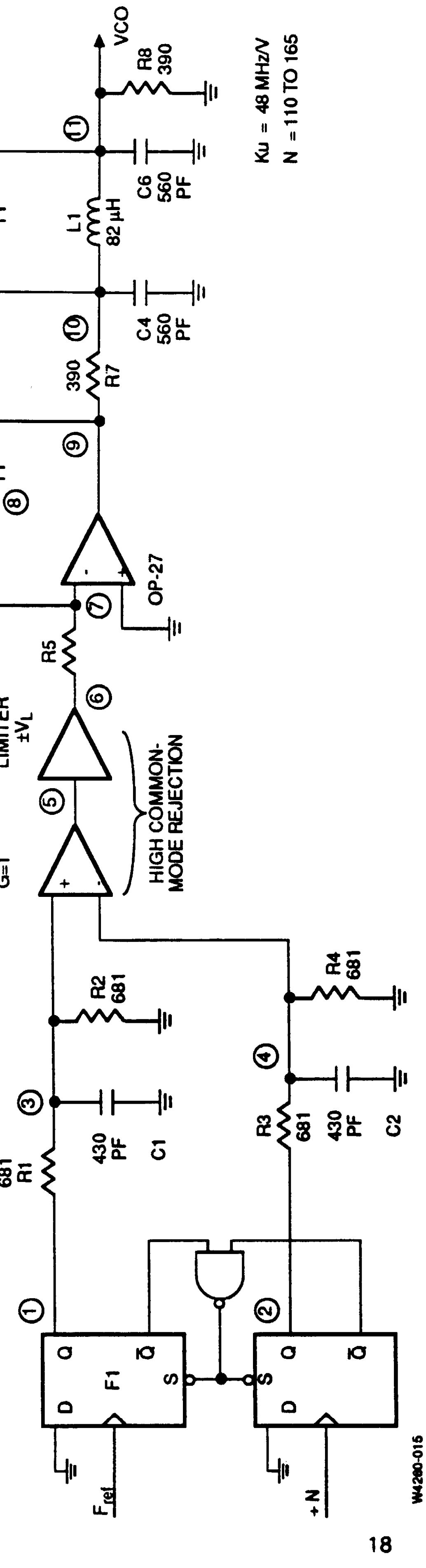


Figure 5 Design Example

Case III: N = 110 to 165

W_n = 88.4 KHz

ξ = 0.85

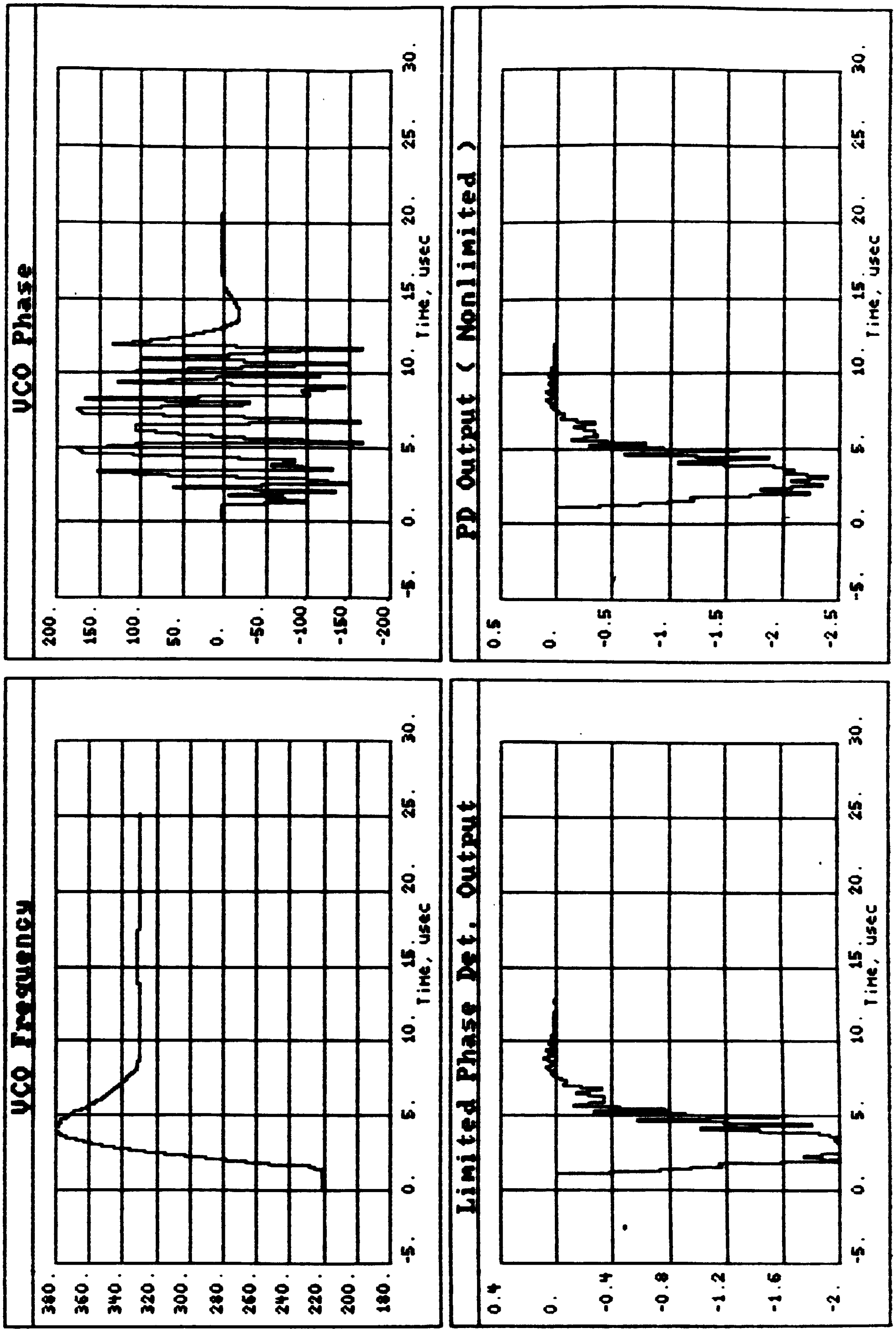


Figure 7

Case II: N = 110 to 165

W_n = 56.5 KHz

ξ = 0.688

Post-Det. Filter $\tau = T_{ref}/2$

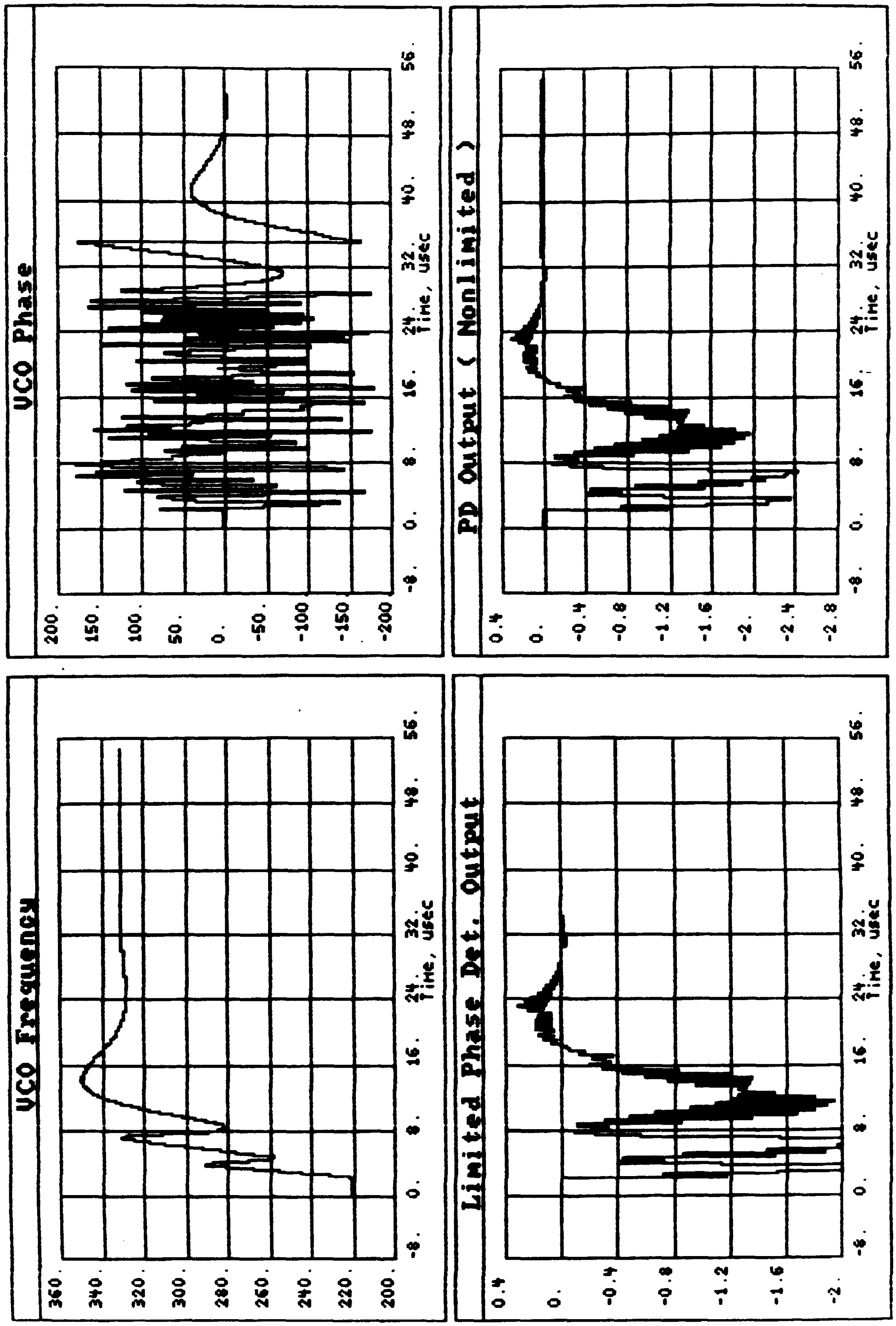


Figure 6

Figure 8

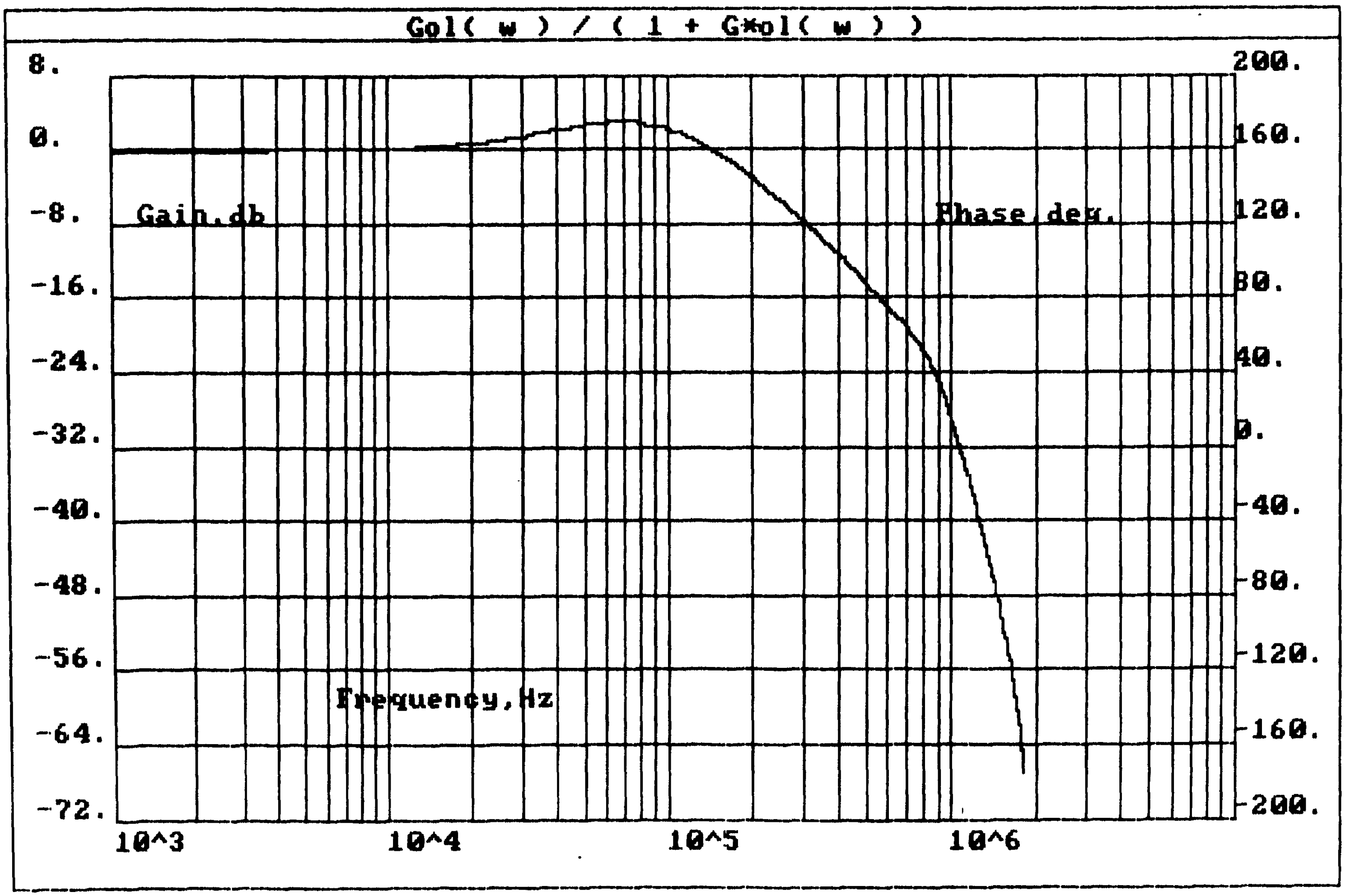
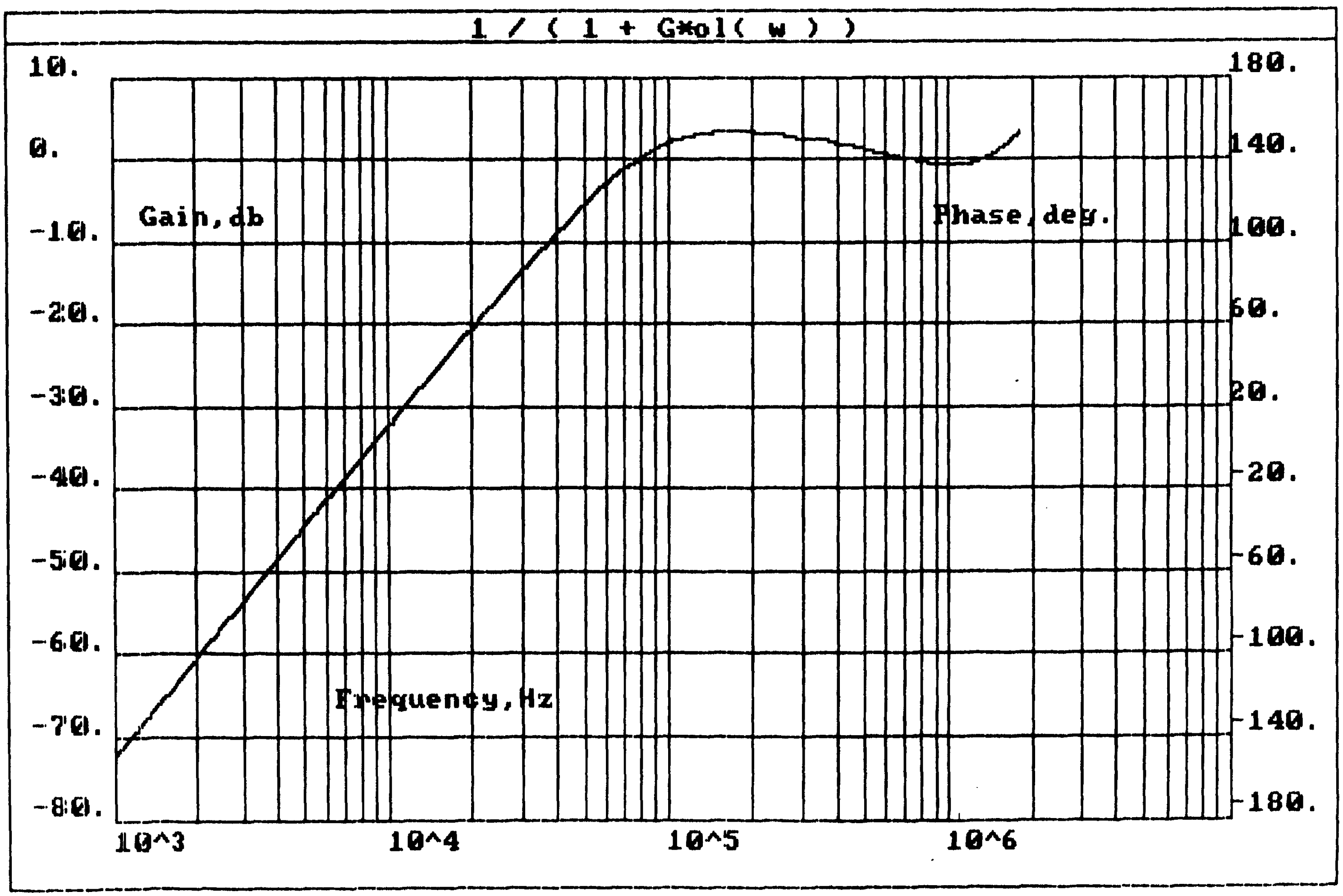

Gol(w) / (1 + G*ol(w))
8.
0.
-8.
-16.
-24.
-32.
-40.
-48.
-56.
-64.
-72.
Gain,db
Phase,deg.
200.
160.
120.
80.
40.
0.
-40.
-80.
-120.
-160.
-200.
Frequency,Hz
10^3
10^4
10^5
10^6

Figure 9



1 / (1 + G*ol(w))
10.
0.
-10.
-20.
-30.
-40.
-50.
-60.
-70.
-80.
180.
140.
100.
60.
20.
-20.
-60.
-100.
-140.
-180.
Gain, db
Phase, deg.
Frequency, Hz
10^3
10^4
10^5
10^6

first-order approximation to an ideal zero-order sample-hold as mentioned earlier. In very narrowband designs, more filtering is of course possible. The output filter is restricted to be an equally-terminated third-order elliptic lowpass filter. Clearly, the best spurious rejection occurs at the filter's finite transmission zero, but since this would in practice require precise tuning and temperature considerations, the stopband attenuation at 95 percent of the reference frequency is used for purposes of comparative evaluation. The frequency hop used in each simulation trial corresponds to one-half the maximum frequency hop range permissible as predicted from linear system theory. This precludes nonlinear cycle slipping behavior at the phase detector from appearing in the results. Finally, the damping factor is restricted to 0.75 throughout.

A compilation of simulation results is shown in Figures 11 and 12. These figures may be used to trade off switching speed for spurious performance. As demonstrated in Figure 11, some additional filtering within the loop can improve settling speed if appropriately selected. In general, settling speed remains approximately equal to that predicted by classical second-order system theory so long as the additional filtering does not reduce the phase margin below roughly 30 degrees.

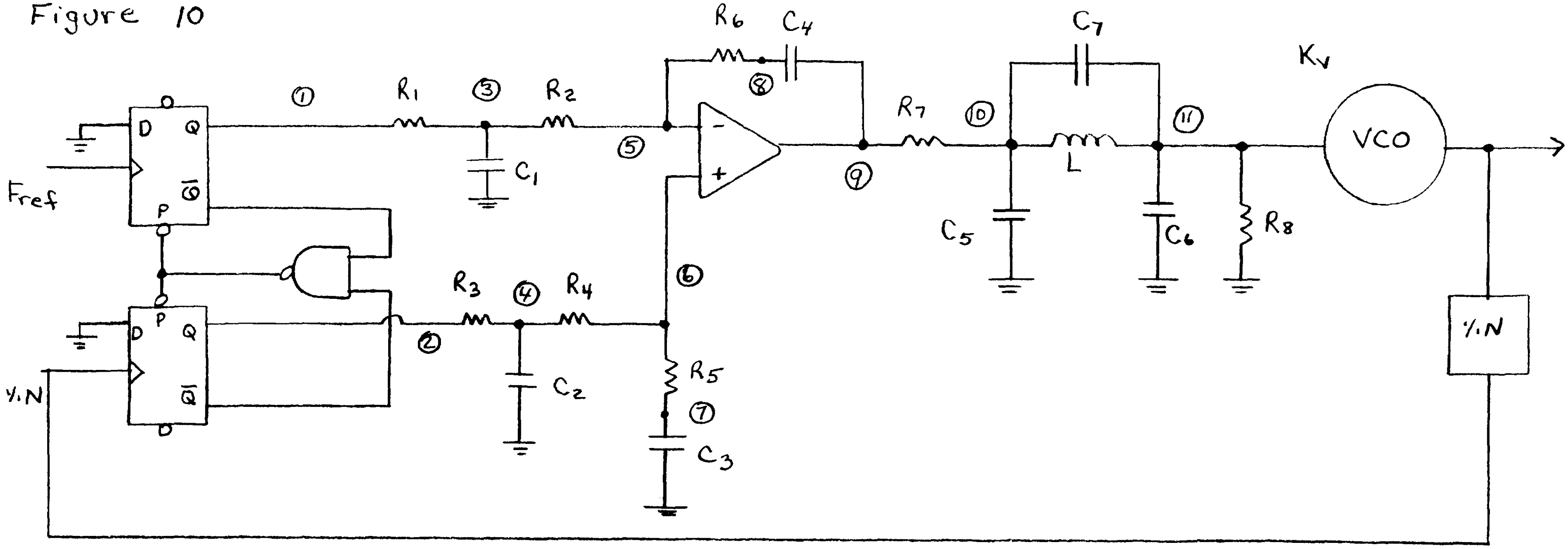
In instances where time does not permit a detailed calculation to be made, two additional guidelines may be helpful. Both guidelines apply to reference frequencies below 2 MHz where low-power Schottky devices are used for the phase detector electronics. For moderate synthesizer spur performance (e.g. -65 dBc), allocate a minimum of 30 to 35 sample periods to achieve phase-lock. If better spurious performance is required, a minimum of 50 sample periods should be allocated.

Only the attenuation of the reference spurs was considered in Figures 11 and 12 since the actual spurious performance level also depends upon the phase detector glitch energy occuring at the reference frequency. This is duty factor and device technology driven and must be ascertained by the designer.

Design Considerations

Although a number of fairly common synthesizer design problems are most appropriately addressed at the systems level, an adequate discussion is out of scope with the material presented thus far. Suffice it so say that i) an open dialog between systems designers and hardware designers should occur during the initial concept phase and ii) key systems requirements which dramatically drive the synthesizer design should be identified to the systems designer with possible hardware simplification trade-offs. These simple guidelines will help the design attain the maximum performance per dollar cost.

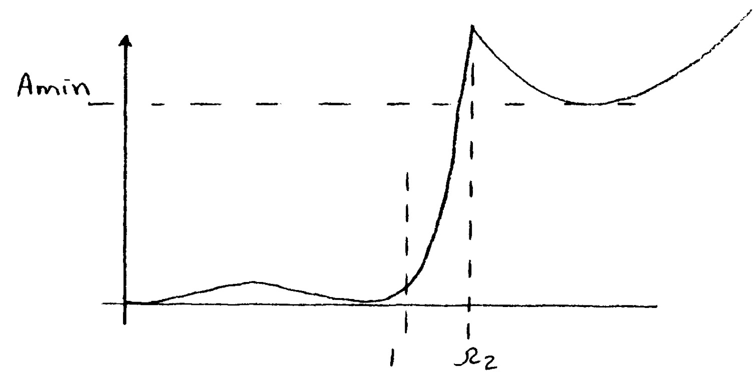
Figure 10



Elliptic Filters

CO3 20

θ	Amin	Ω_2
54°	10 dB	1.3498
38°	20 dB	1.8245
26°	30 dB	2.6003
18°	40 dB	3.7137
12°	50 dB	5.5386
8°	60 dB	8.2868



$R_7 = R_8 = 1K$

Fref = 1MHz

θ	$C_5 = C_6$	C_7	L
54°	162 pf	214 pf	118 μH
38°	281 pf	103 pf	246 μH
26°	449 pf	60.7 pf	418 μH
18°	674 pf	39.5 pf	641 μH
12°	1029 pf	25.6 pf	990 μH
8°	1556 pf	16.9 pf	1504 μH

Fref = 1 MHz

$\zeta = \frac{1}{2} \omega_n \tau_2 = 0.75$

$R_1 = R_2 = R_3 = R_4 = 1\text{ K}$

$C_1 = C_2 = \frac{T_{ref}}{2 R_1} = 500\text{ pf}$

$K_d = 0.8$ v/rad.

$\omega_n = \left(\frac{K_d K_V}{4 N \tau_1} \right)^{1/2}$

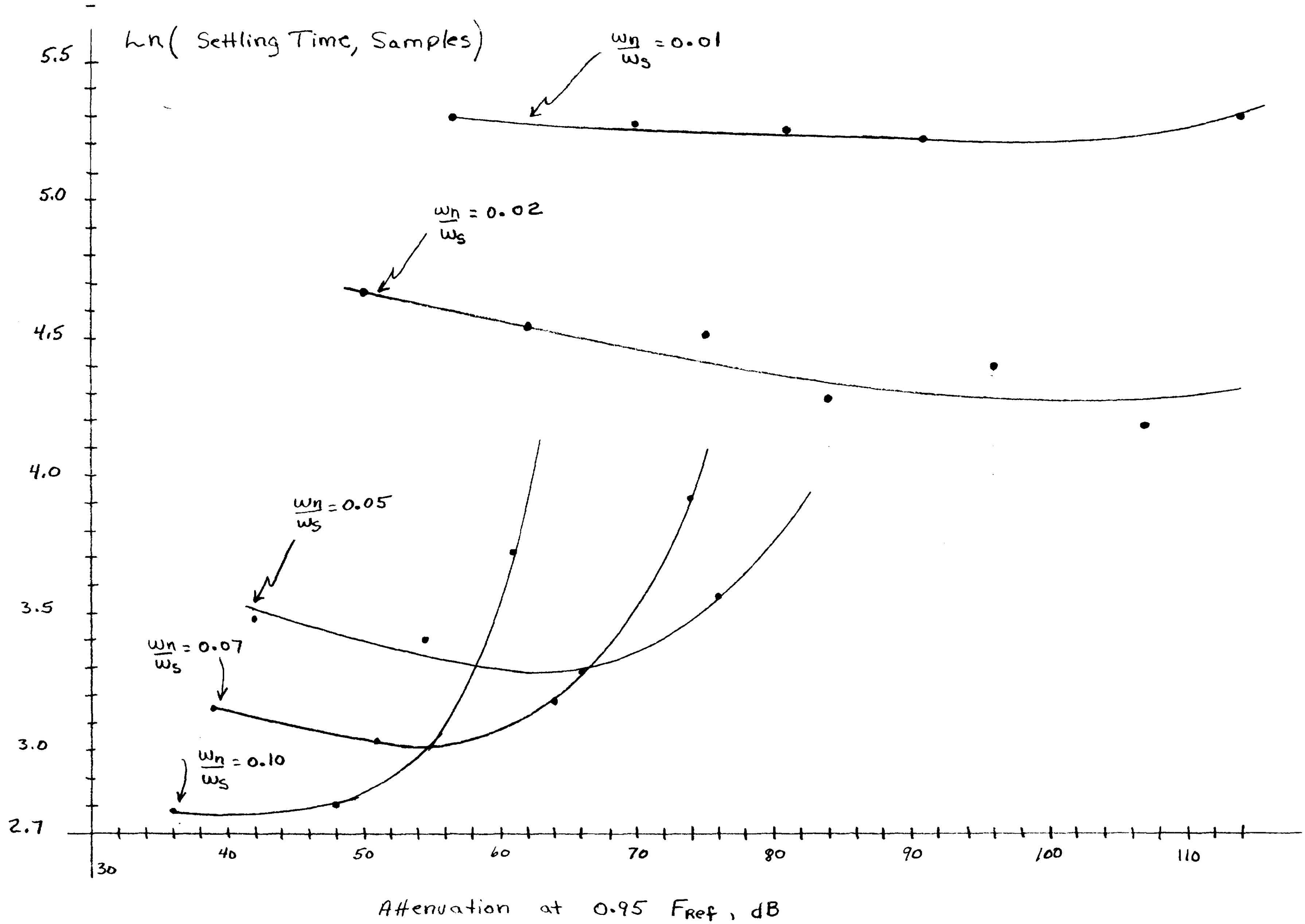
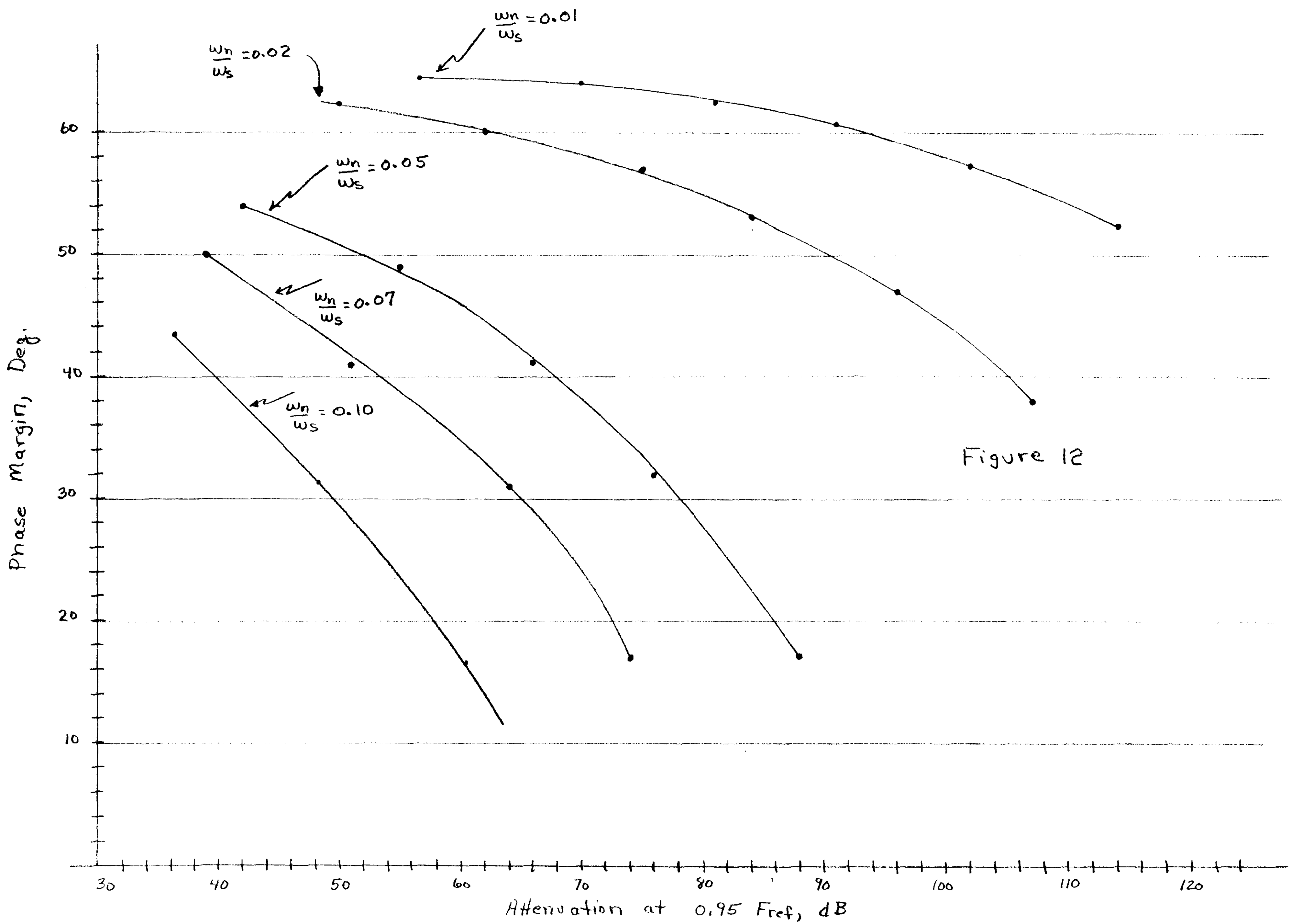

Ln(Settling Time, Samples)
5.5
5.0
4.5
4.0
3.5
3.0
2.7
$\frac{\omega_n}{\omega_s} = 0.01$
$\frac{\omega_n}{\omega_s} = 0.02$
$\frac{\omega_n}{\omega_s} = 0.05$
$\frac{\omega_n}{\omega_s} = 0.07$
$\frac{\omega_n}{\omega_s} = 0.10$
30
40
50
60
70
80
90
100
110
Attenuation at 0.95 F_{Ref}, dB

Figure 11



$\frac{\omega_n}{\omega_s} = 0.01$
$\frac{\omega_n}{\omega_s} = 0.02$
$\frac{\omega_n}{\omega_s} = 0.05$
$\frac{\omega_n}{\omega_s} = 0.07$
$\frac{\omega_n}{\omega_s} = 0.10$
Phase Margin, Deg.
60
50
40
30
20
10
30
40
50
60
70
80
90
100
110
120
Attenuation at 0.95 Fref, dB

Figure 12

Interfaces

As stated in the introductory comments, interfaces need to be properly frozen early in the design phase since these invariable affect other radio elements in addition to the synthesizer. Some key notes to consider in defining the synthesizer interface follow.

Any and all interface control signals to or from the synthesizer are possible sources of external contamination. Each input/output signal must be analyzed and adequate reverse isolation provided regardless whether the input is analog or digital. In some cases, separate voltage supply lines should be used for the buffering circuitry within the synthesizer. Contrary to popular assumption, digital gates do not have infinite reverse isolation. Differential inputs with hysteresis are strongly recommended.

The interface signal protocol should be designed such that the signal lines are in a static condition during the time periods where low synthesizer noise and spurs are required. Active interface signals otherwise require further isolation of control line inputs/outputs from sensitive circuit areas within the synthesizer.

Investigate the voltage regulation requirements prior to specifying voltage forms for the synthesizer design. The natural tendency is to specify an external 5 volt supply whenever TTL circuitry is involved for instance. Disastrous results can occur later when the designer concludes that an additional 60 dB of regulation is required at 100 Hz to prevent undesired spectral contamination from the power supply noise.

Use the highest reference frequency possible for transport to the synthesizer, dividing the supplied reference as required once within the synthesizer. This step reduces reference contamination problems outside the synthesizer by effectively 20 log(N). Passive crystal filtering of the reference within the synthesizer is often necessary and desirable.

Wherever possible, use system clocks, references, and channel spacings which are integer multiples of the lowest frequency in order to prevent undesired spurious outputs. For example, use of a 10 MHz reference in a phase-locked loop synthesizer which creates 3 MHz channel spacings invariably results in 1 MHz spurs due to sampling effects (e.g. 3* 3 MHz - 10 MHz gives 1 MHz).

Accept the axiom that no one is responsible for interface-induced interactions upon the synthesizer performance but you. Only the RF engineer typically has the insight to foresee problems at the system level such as those mentioned above. e.g. Load pulling is another common problem which arises when inadequate isolation is provided between voltage controlled oscillator outputs and the external world. A classical example is that of a QPSK modulator in which the I and Q modulation signals cause minute mixer VSWR changes which end up modulating a phase-locked loop's VCO. Since the I and Q signals have considerable low frequency content (sinc() function), the PLL attempts to track out any modulations falling within its own loop bandwidth.

Be involved with all grounding policies at the synthesizer system connector. Good grounding design is mandatory in modern digital radios which are generally bulging with single-ended high speed digital logic. Taking measures such as performing EMI power supply filtering within a separate cavity within the synthesizer is highly recommended.

Internal Design Issues

The synthesizer designer must be cognizant of synthesis techniques [11] and intimately familiar with all aspects of any electronic part chosen for the design. In the techniques area, a mixture of direct, indirect, and hybrid synthesis techniques should be used to realize the best performance versus size, power consumption and cost. The foregoing discussions should assist in performing trade-offs with indirect synthesis options. With direct-digital synthesis continuing its trend toward improved performance, this technology should be intelligently incorporated wherever possible (Figure 13). Examples of some of the more subtle design details which arise follow.

Very rarely are Type I phase-locked loops used in synthesizer design because they potentially display a long-term phase transient due to post-tuning drift type effects. With proper design, this is however a negligible problem for VCO frequencies below roughly 1.5 GHz. Even so, the settling speed of a properly designed Type I phase-locked loop (4 sample period settling being achievable) may be exploited and the output divided down with a highspeed digital divider if necessary to eliminate any significant post-tuning drift effects.

Digital devices are notorious for aliasing any high frequency noise components on their voltage supply lines down to baseband, thereby appearing within the closed-loop bandwidth of phase-locked loops. A design guideline which is virtually invariant with contamination frequency is that 20 mV peak-peak ripple on the supply line results in -57 dBc spurs for Schottky logic. Similar design guidelines exist for other device technologies.

Amplifiers′ susceptibility to power line induced spurious contamination is a function of output power level with respect to the amplifier′s compression point. Measurements must be invariably made to identify a component′s behavior with supply contamination. Data for a Watkins-Johnson T08 amplifier is presented in Figure 14.

Internal time constants within discrete circuitry, particularly for fast-hopping synthesizers, must be carefully chosen so as not to cause a "phase roll" due to very slight shifts in circuit operating points immediately after a frequency hop. Although the phase transient result is clearly visible, the voltage shifts required to create the problem are far to small to be detected using an oscilloscope.

Post-detection filters are generally used immediately following the phase/frequency detector in order to reduce the slew rates seen by the lead-lag filter. Nonetheless, slew rates

Figure 13

DDS Data —
Not available Yet

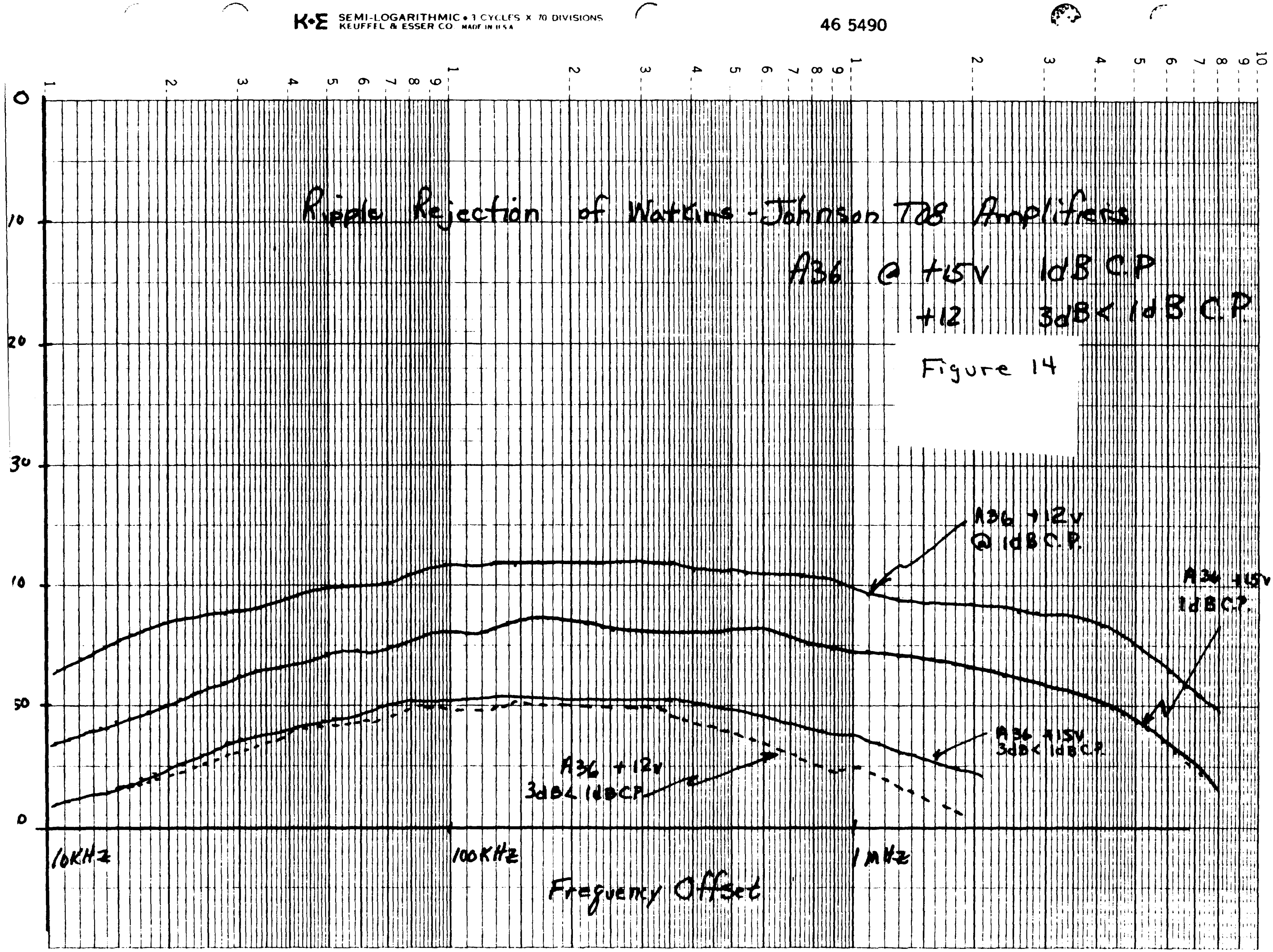

K•E SEMI-LOGARITHMIC • 3 CYCLES X 70 DIVISIONS
KEUFFEL & ESSER CO. MADE IN U.S.A.
46 5490
Ripple Rejection of Watkins-Johnson T08 Amplifiers
A36 @ +15V 1dB C.P
+12 3dB < 1dB C.P
A36 +12V @ 1dB C.P.
A36 +15V 1dB C.P.
A36 +15V 3dB < 1dB C.P.
A36 +12V 3dB < 1dB CP
0
10
20
30
10
50
0
10KHz
100KHz
1MHz
Frequency Offset

Figure 14

in excess of the op-amp's capabilities can still occur, resulting in higher phase noise levels than predicted. Design measures should be taken to avoid this occurrence.

Conclusion

A number of results have been presented which should be helpful in initial frequency synthesizer design. Details have also been presented describing a general phase-locked loop analysis tool for both frequency domain and time domain studies. Finally, a number of hardware design recommendations have been suggested which lead to improved synthesizer designs.

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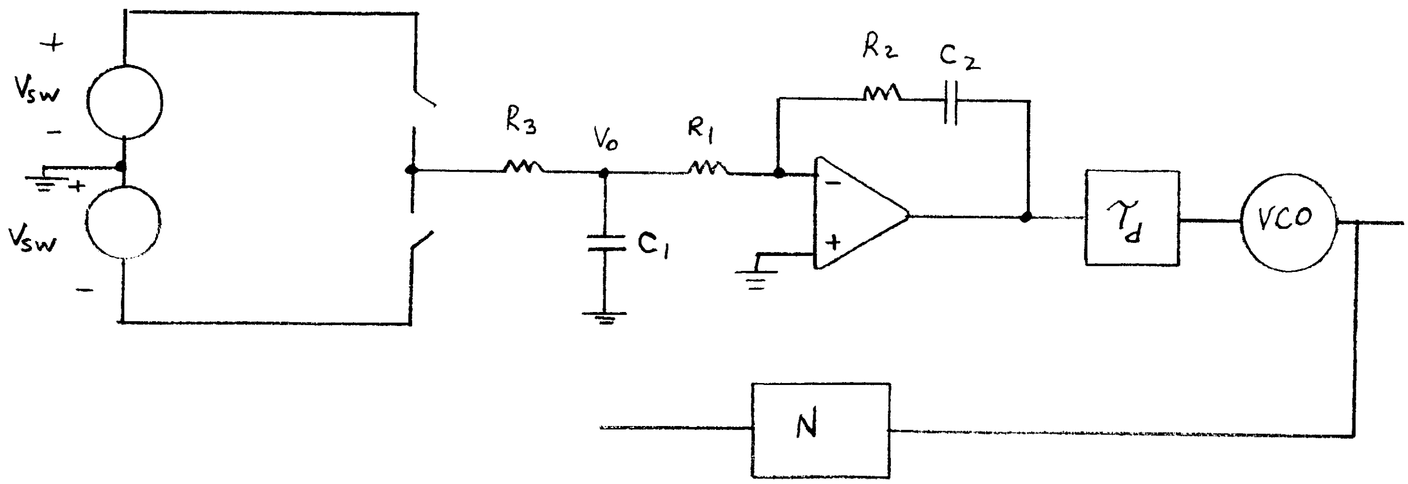
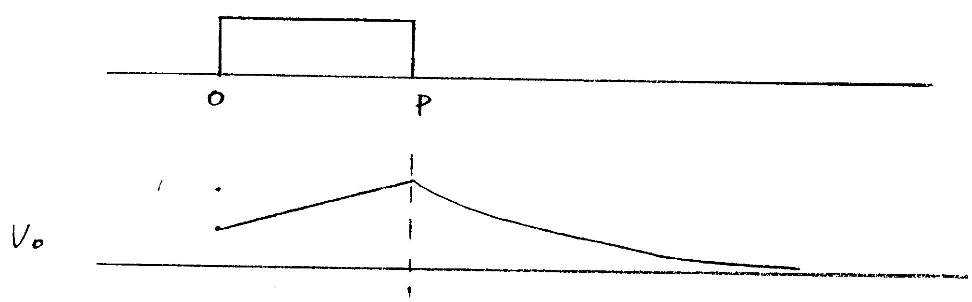
High Z Ø/f Detector



Ø detector operates as a tri-state switch

Say at $t=0$ V_o is initially V_{oo}



For $0 \le t \le P$:

$$V_o = V_{oo}\, e^{-t/\tau_T} + V_{sw} \frac{R_1}{R_1+R_3}\left(1 - e^{-t/\tau_T}\right) \qquad \tau_T = C_1 \frac{R_1 R_3}{R_1+R_3}$$

$$V_o(P) = V_{oo}\, e^{-P/\tau_T} + V_{sw} \frac{R_1}{R_1+R_3}\left(1 - e^{-P/\tau_T}\right)$$

For the remainder of the reference period, $T-P$, V_o decays exponentially with time constant $\tau_o = C_1 R_1$

For $p \ll \tau_T$

$$V_o(p) \approx V_{oo} + \frac{V_{sw} R_1}{R_1 + R_3} \frac{p}{\tau_T}$$

$$= V_{oo} + \frac{V_{sw} R_1}{R_1 + R_3} \frac{T}{2\pi \tau_T} \phi_e^*(0)$$

where $\phi_e^*(0)$ is the sampled phase error at $t = 0$.

For the remainder of the reference period,

$$V_o(t) = \left[V_{oo} + \frac{V_{sw} R_1}{R_1 + R_3} \frac{T}{2\pi \tau_T} \phi_e^*(0) \right] e^{-t/\tau_1}$$

where $\tau_1 = R_1 C_1$

In transform form,

$$V_o(s) = \frac{V_{oo}}{s + 1/\tau_1} + \frac{V_{sw} R_1}{R_1 + R_3} \frac{T}{2\pi \tau_T} \phi_e^*(0) \frac{1}{s + 1/\tau_1}$$

If we ignore the initial condition and note that $V_o(t)$ is the result of superimposing the effects of all previous phase error samples taken every T seconds,

$$V_o(s) = \frac{V_{sw} R_1}{R_1 + R_3} \frac{T}{2\pi \tau_T (s + 1/\tau_1)} \phi_e^*(s) \left[1 + e^{-sT} e^{-T/\tau_1} + e^{-2sT} e^{-2T/\tau_1} \cdots \right.$$

$$= \frac{V_{sw} R_1 \, T \, \phi_e^*(s)}{(R_1 + R_3)\, 2\pi \tau_T (s + 1/\tau_1)} \quad \frac{1}{1 - e^{-sT} e^{-T/\tau_1}}$$

Since may approximate

$$\phi_e^*(s) \approx \frac{1}{T} \phi_e(s)$$

and $K_d = \dfrac{V_{sw} R_1}{(R_1 + R_3)\; 2\pi}$

$$\therefore \quad V_o(s) = \frac{K_d \quad \phi_e(s)}{s\tau_T + \tau_T/\tau_1} \quad \frac{1}{1 - e^{-sT} e^{-T/\tau_1}}$$

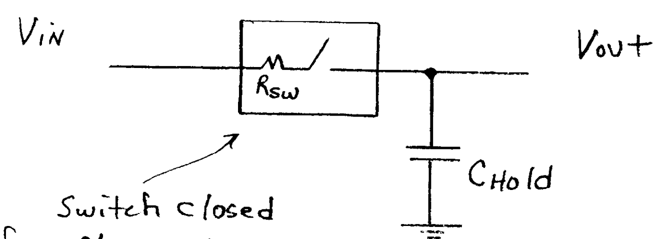
Ideal Sample-Hold

$$\frac{V_o(s)}{V_i(s)} = \frac{1 - e^{-sT}}{s}$$

Inefficient sample-hold

$$\frac{V_o(s)}{V_i(s)} = \frac{1 - e^{-sT}}{s} \; \frac{e^{sT}(1-A)}{e^{sT} - A}$$

where $A = e^{-\tau_{closed}/\tau_{RC}}$



- Switch closed for τ_{closed} sec. to take sample
- $\tau_{RC} = R_{SW} \, C_{Hold}$

J. A. Crawford
May 6, 1989

Type I Sample-Hold Ideal

$$G_{OL}(s) = \frac{K_d}{N} \frac{1-e^{-sT}}{s} \frac{K_v}{s}$$

$$G_{OL}(z) = \frac{K_d K_v}{N} (1-z^{-1}) \mathcal{Z}\left\{ \frac{1}{s^2} \right\}$$

$$= \frac{K_d K_v}{N} \frac{z-1}{z} \frac{Tz}{(z-1)^2} = \frac{K_d K_v}{N} T \frac{1}{z-1} = \frac{K}{z-1}$$

where $K = \frac{K_d K_v}{N} T$

$$\theta_e(z) \Big|_{@VCO} = \frac{2\pi \Delta f T z}{(z-1)^2} \frac{1}{1+G_{OL}(z)}$$

Rad. @ VCO for $\frac{\Delta f}{N}$ Hz Change at reference

$$= \frac{2\pi \Delta f T z}{(z-1)^2} \frac{1}{1+\frac{K}{z-1}}$$

$$= \frac{2\pi \Delta f T z}{(z-1)} \frac{1}{(z-1+K)}$$

$$= \frac{2\pi \Delta f T z}{K} \left[\frac{1}{z-1} - \frac{1}{z-1+K} \right]$$

$$= \frac{2\pi \Delta f T}{K} \left[\frac{z}{z-1} - \frac{z}{z-1+K} \right]$$

$$\theta_e(nT) = \frac{2\pi \Delta f T}{K} \left[1 - (1-K)^n \right] \quad \text{Radians}$$

Gain Margin @ $\omega \ni \angle G_{OL} \equiv 180°$. This occurs at $\omega = \frac{\pi}{T}$ where $z \equiv -1$.

$$GM = -20 \log\left[\left| G_{OL} \right|_{\omega=\frac{\pi}{T}} \right] = -20 \log\left[\frac{K}{2} \right]$$

$$= -20 \log\left[\pi \frac{\omega_n}{\omega_s} \right] \quad \text{where } \omega_n = \frac{K_d K_v}{N},\ \omega_s = \frac{2\pi}{T}$$

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Noise

Let VCO self-noise be $S_V(\omega)$ $rad.^2/Hz$

Proved at other times,

$$S_o(\omega) = S_V(\omega) \left| \frac{1}{1+G_{OL}(z)} \right|^2$$

$$\frac{S_o(\omega)}{S_V(\omega)} = \left| \frac{z-1}{z-1+K} \right|^2 = \frac{\left[\cos(\omega T)-1\right]^2 + \sin^2(\omega T)}{\left[\cos(\omega T)-1+K\right]^2 + \sin^2(\omega T)}$$

$$= \frac{\cos^2(\omega T) - 2\cos(\omega T)+1 + \sin^2(\omega T)}{\cos^2(\omega T) + 2(K-1)\cos(\omega T) + (K-1)^2 + \sin^2(\omega T)}$$

$$= \frac{2-2\cos\omega T}{1+ 2(K-1)\cos(\omega T) + K^2 - 2K+1}$$

$$= \frac{4\sin^2(\omega T/2)}{K^2-2K+2 + 2(K-1)\cos(\omega T)}$$

$$= 4\sin^2\left(\frac{\omega T}{2}\right) \quad \text{for } K \equiv 1 \text{ case}$$

For reference noise — Sampled reference noise $\approx \frac{1}{T}\theta_{RN}(\omega)$

$$\theta_o(\omega) = \theta^*_{RN}(\omega) \frac{G_{OL}(\omega)}{1+G_{OL}(z)}$$

$$\frac{S_o(\omega)}{S_{RN}(\omega)} = \frac{1}{T^2} \frac{N^2K^2}{T^2\omega^4} 4\sin^2\left(\frac{\omega T}{2}\right) \left| \frac{1}{1+G_{OL}(z)} \right|^2$$

$$= N^2K^2 \left[\frac{\sin(\omega T/2)}{(\omega T/2)}\right]^4 \frac{1}{K^2-2K+2+2(K-1)\cos(\omega T)}$$

$$= N^2 \left[\frac{\sin(\omega T/2)}{(\omega T/2)}\right]^4 \quad \text{for } K \equiv 1 \text{ case}$$

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Phase Margin

$$G_{OL}(z) = \frac{K}{z-1}$$

pt. @ unity gain : $1 = \dfrac{K^2}{|z-1|^2}$

$$K^2 = |z-1|^2 = (z-1)(z^*-1)$$

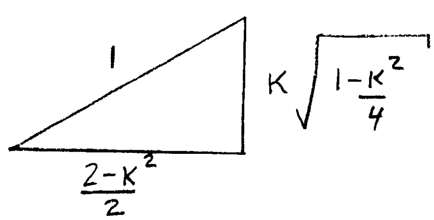
$$= 1 - (z+z^*) + 1 \qquad \text{Let } 2\alpha = z + z^* \text{ (Real)}$$

$$= 2 - 2\alpha$$

$$\therefore \quad \alpha = \frac{2-K^2}{2} = \cos\theta_u$$

where unity gain occurs at $z = e^{j\theta_u}$

$\angle G_{OL}(z = e^{j\theta_u})$:



$$\angle G_{OL} = +\tan^{-1}\left[\frac{\sin\theta_u}{|\cos\theta_u - 1|}\right] - \pi$$

always neg. inside

$$= +\tan^{-1}\left[K\sqrt{1-\frac{K^2}{4}}\;\frac{1}{\left|1-\frac{K^2}{2}-1\right|}\right] - \pi$$

$$= +\tan^{-1}\left[\frac{2}{K}\sqrt{1-\frac{K^2}{4}}\right] - \pi$$

$$= +\tan^{-1}\left[\sqrt{\frac{4}{K^2}-1}\right] - \pi$$

$$\phi_{margin} = \tan^{-1}\left[\sqrt{\frac{4}{K^2}-1}\right]$$

Case I   Ideal Type I Sample - Hold Phase Detector

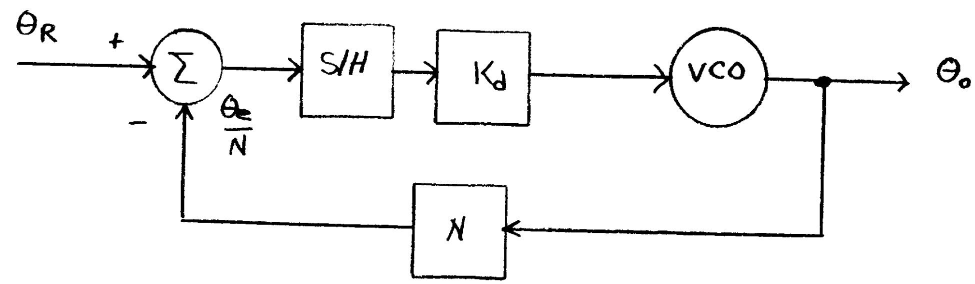
$$G_{OL}(s) = \frac{K_d}{N}\,\frac{1-e^{-sT}}{s}\,\frac{K_v}{s}$$

$$G_{OL}(z) = \frac{K}{z-1}$$

$$\theta_e(nT) = \frac{2\pi\Delta f T}{K}\left[1-(1-K)^n\right]$$

$$\text{Gain Margin} = -20\log\left[\pi\,\frac{\omega_n}{\omega_s}\right]\ \text{dB}$$

$$\omega_n = \frac{K_d K_v}{N}$$



Let $S_v(\omega) = \widetilde{\theta^2_{VCO}(\omega)}$ VCO self-noise

$S_{RN}(\omega) = \widetilde{\theta^2_{RN}(\omega)}$ Reference noise

$S_o(\omega) = \widetilde{\theta^2_{ON}(\omega)}$ Output noise

Units all rad^2/Hz

~ denotes statistical av.

ϕ_{margin}

$$\phi_{margin} = \tan^{-1}\left[\sqrt{\frac{4}{K^2}-1}\right]$$

Notes

1) Phase - lock achieved in one sample for K = 1

Gain Margin = 6 dB

2) Reference and VCO power spectral density transfer functions

Ref: $$\frac{S_o(\omega)}{S_{RN}(\omega)} = \frac{16K^2N^2\sin^4(\omega T/2)}{(\omega T)^4\left(K^2+2-2K+2(K-1)\cos(\omega T)\right)}$$

$$= N^2\left[\frac{\sin(\omega T/2)}{(\omega T/2)}\right]^4 \quad \text{for } K \equiv 1$$

VCO: $$\frac{S_o(\omega)}{S_{vco}(\omega)} = \frac{4\sin^2(\omega T/2)}{K^2+2-2K+2(K-1)\cos(\omega T)}$$

$$= 4\sin^2\left(\frac{\omega T}{2}\right) \quad \text{for } K \equiv 1$$

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Type I Sample-Hold Non-ideal

$$G_{OL}(s) = \frac{K_d}{N}\,\frac{1-e^{-sT}}{s}\,\frac{e^{sT}(1-A)}{e^{sT}-A}\,e^{-s\tau_d}\,\frac{K_v}{s}$$

$$A = e^{-\tau_{sw}/\tau_{RC}}$$

$\frac{e^{sT}(1-A)}{e^{sT}-A}$ ↑ ineff. sampling

$e^{-s\tau_d}$ ↑ loop time delay due to added filters, etc.

$$= \frac{K_d K_v}{N}(1-A)\,\frac{e^{sT}-1}{e^{sT}-A}\,\mathcal{Z}\left\{\frac{e^{-s\tau_d}}{s^2}\right\}$$

$$G_{OL}(z) = \frac{K_d K_v}{N}(1-A)\,\frac{z-1}{z-A}\left\{\frac{mT}{z-1}+\frac{T}{(z-1)^2}\right\} \qquad \text{where } m = 1-\frac{\tau_d}{T}$$

$$= \frac{K_d K_v}{N}(1-A)\,\frac{z-1}{z-A}\,\frac{mT(z-1)+T}{(z-1)^2}$$

$$= \frac{K_d K_v T}{N}(1-A)\,\frac{mz+(1-m)}{(z-A)(z-1)}$$

$$= K(1-A)\,\frac{mz+(1-m)}{(z-A)(z-1)} \qquad \text{where } K = \frac{K_d K_v}{N}T$$

$$\theta_e(z)\Big|_{@VCO} = \frac{2\pi\Delta f T z}{(z-1)^2}\;\frac{1}{1+K(1-A)\frac{mz+(1-m)}{(z-A)(z-1)}}$$

$$= \frac{2\pi\Delta f T z}{z-1}\;\frac{z-A}{(z-1)(z-A)+K(1-A)\big(mz+(1-m)\big)}$$

$$= \frac{2\pi\Delta f T z\,(z-A)}{(z-1)\left[z^2+z\big(-1-A+Km(1-A)\big)+A+K(1-A)(1-m)\right]}$$

$$= \frac{2\pi\Delta f T z\,(z-A)}{z^3+\alpha z^2+\beta z+\gamma}$$

$$\alpha = -1-1-A+Km(1-A) = K(1-A)m-2-A$$

$$\beta = 1+A-Km(1-A)+A+K(1-A)(1-m) = 1+2A+K(1-A)(1-2m)$$

$$\gamma = -A-K(1-A)(1-m)$$

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Phase Margin

$$G_{OL}(z) = K(1-A)\,\frac{mz+(1-m)}{(z-A)(z-1)}$$

Unity Gain Point

$$K^2(1-A)^2 = \left|\frac{(z-A)(z-1)}{mz+(1-m)}\right|^2 = L^2 \qquad 2\alpha = z+z^*$$

$$L^2 = \frac{(z-A)(z^*-A)(z-1)(z^*-1)}{(mz+1-m)(mz^*+1-m)}$$

$$= \frac{(1+A^2-2A\alpha)(2-2\alpha)}{m^2+(1-m)^2+m(1-m)2\alpha}$$

$$4A\alpha^2 - \alpha\left[2+2A^2+4A+2L^2m(1-m)\right] + \left[2+2A^2-L^2\left(m^2+(1-m)^2\right)\right] = 0$$

$$\alpha = \text{Real Part}\left[z \ni |G_{OL}(z)| = \text{Unity}\right]$$

Let $\beta = \sin\left[\cos^{-1}\alpha\right]$

$$\theta_{margin} = \pi - \angle G_{OL}(z=\alpha+j\beta)$$

$$= 180^\circ + \tan^{-1}\left[m\beta,\ 1+m\alpha-m\right] - \tan^{-1}\left[\beta,\ \alpha-A\right] - \tan^{-1}\left[\beta,\ \alpha-1\right]$$

J. A. Crawford

Type II Ideal Sample - Hold

$$G_{OL}(s) = \frac{K_d}{N} \frac{1-e^{-sT}}{s} \frac{1+s\tau_2}{s\tau_1} \frac{K_v}{s}$$

$$= \frac{K_d K_v}{N \tau_1} \frac{1-e^{-sT}}{s} \frac{1+s\tau_2}{s^2}$$

$$G_{OL}(z) = \frac{K_d K_v}{N \tau_1} (1-z^{-1}) \mathcal{Z}\left\{ \frac{1+s\tau_2}{s^3} \right\}$$

$$= \frac{K_d K_v}{N\tau_1} \frac{z-1}{z} \left\{ \frac{1}{2} \frac{T^2 z(z+1)}{(z-1)^3} + \tau_2 \frac{Tz}{(z-1)^2} \right\}$$

$$= \frac{K_d K_v}{N} T \frac{1}{\tau_1} \frac{z-1}{z} \frac{\frac{1}{2} T z(z+1) + \tau_2 z(z-1)}{(z-1)^3}$$

$$= \frac{K}{\tau_1} \frac{\frac{T}{2}(z+1) + \tau_2(z-1)}{(z-1)^2}$$

$$= \frac{K}{\tau_1} \frac{z\left(\frac{T}{2}+\tau_2\right) + \left(\frac{T}{2}-\tau_2\right)}{(z-1)^2}$$

Let $a = \frac{T}{2} + \tau_2$

$b = \frac{T}{2} - \tau_2$

$$\theta_e(z) = \frac{2\pi\Delta f T z}{(z-1)^2} \frac{1}{1 + \frac{K}{\tau_1} \frac{za+b}{(z-1)^2}}$$

$$= 2\pi \Delta f T z \frac{1}{(z-1)^2 + \frac{K}{\tau_1}(az+b)}$$

$$= \frac{2\pi\Delta f T z}{z^2 + z\left(\frac{aK}{\tau_1} - 2\right) + \left(1 + \frac{Kb}{\tau_1}\right)}$$

Dead-beat response possible if

$$\frac{aK}{\tau_1} = 2 \qquad \frac{Kb}{\tau_1} = -1$$

or $\frac{aK}{2} = -Kb$

or $\frac{a}{2} = -b \implies \boxed{\tau_2 = \frac{3}{2} T} \implies K = \frac{2\tau_1}{a}$

$$K = \frac{2\tau_1}{a} = \frac{2\tau_1}{\frac{T}{2} + \tau_2}$$

$$= \frac{2\tau_1}{2T} = \frac{\tau_1}{T}$$

$$K = \frac{K_d K_v}{N} T = \frac{\tau_1}{T} \Rightarrow \frac{K_d K_v}{N\tau_1} = \frac{1}{T^2} = \omega_n^2$$

$$\boxed{\omega_n = \frac{1}{T}}$$

Dead beat Response for

$$\tau_2 = \frac{3}{2} T$$

$$\omega_n = \frac{1}{T} \quad R/sec$$

$$\xi = \frac{1}{2}\omega_n \tau_2 = \frac{1}{2}\,\frac{1}{T}\,\frac{3}{2}T = \frac{3}{4}$$

$$\text{Gain Margin} = -20\log\left[\frac{K}{\tau_1}\left|\frac{-\left(\frac{T}{2}+\tau_2\right)+\left(\frac{T}{2}-\tau_2\right)}{4}\right|\right]$$

$$= -20\log\left[\frac{K}{\tau_1}\,\frac{\tau_2}{2}\right] = -20\log\left[\frac{K_d K_v}{N} T \frac{1}{\tau_1}\,\frac{\tau_2}{2}\right]$$

$$= -20\log\left[\frac{K_d K_v}{N\tau_1}\, T\, \frac{\xi}{\omega_n}\right]$$

$$= -20\log\left[\omega_n^2\,\frac{2\pi}{\omega_s}\,\frac{\xi}{\omega_n}\right] = -20\log\left[2\pi\xi\,\frac{\omega_n}{\omega_s}\right]$$

where $\omega_n = \left(\frac{K_d K_v}{N\tau_1}\right)^{1/2}$

$\omega_s = \frac{2\pi}{T}$

J.A. Crawford

Ideal Type II S/H

$$\left| \frac{K}{\Upsilon_1} \frac{Za+b}{(Z-1)^2} \right| = 1$$

$$\frac{K^2}{\Upsilon_1^2} = L^2 = \frac{\left[(Z-1)(Z^*-1) \right]^2}{(aZ+b)(aZ^*+b)} = \frac{(2-2\alpha)^2}{a^2+b^2+2ab\alpha}$$

$$\alpha^2 - \alpha\left(2 + \tfrac{1}{2}abL^2\right) - L^2\frac{a^2+b^2}{4} + 1 = 0$$

Solving the quadratic

$$\alpha = 1 + \frac{ab}{4}L^2 - \frac{1}{4}\sqrt{L^4a^2b^2 + L^2(a+b)^2 4}$$

But $a+b = T$

$$\alpha = 1 + \frac{ab}{4}L^2 - \frac{1}{4}\sqrt{L^4a^2b^2 + 4L^2T^2}$$

$$\text{Ømargin} = 180^\circ + \text{Tan}^{-1}\left[a\beta, a\alpha+b\right] - 2\,\text{Tan}^{-1}\left[\beta, \alpha-1\right]$$

$$\alpha = \text{Real}\left[Z\right]$$

$$\alpha = 1 + \frac{ab}{4}\left(\frac{K}{\Upsilon_1}\right)^2 - \frac{KT}{4\Upsilon_1}\sqrt{\left(\frac{K}{\Upsilon_1}ab\right)^2 + 4}$$

Type II Sample-Hold, Delay, Inefficient

$$G_{OL}(s) = \frac{K_d}{N} \frac{1-e^{-sT}}{s} \frac{e^{sT}(1-A)}{e^{sT}-A} \frac{1+s\tau_2}{s\tau_1} e^{-s\tau_d} \frac{K_v}{s}$$

$$= \frac{K_d K_v}{N\tau_1} \frac{e^{sT}-1}{e^{sT}-A} (1-A) \frac{1+s\tau_2}{s^3} e^{-s\tau_d}$$

$$G_{OL}(z) = \frac{K_d K_v}{N\tau_1} \frac{z-1}{z-A} (1-A)\, \mathcal{Z}_m \left\{ \frac{1+s\tau_2}{s^3} \right\} \qquad m = 1 - \frac{\tau_d}{T}$$

$$= \frac{K_d K_v}{N\tau_1} (1-A) \frac{z-1}{z-A} \left\{ \frac{T^2}{2} \frac{m^2 z^2 + (2m-2m^2+1)z + (m-1)^2}{(z-1)^3} + \frac{\tau_2 T}{(z-1)^2} + \frac{\tau_2 m T}{z-1} \right\}$$

$$= \frac{K}{\tau_1} (1-A) \frac{1}{z-A} \left\{ \frac{\frac{T}{2}\left[m^2 z^2 + (2m-2m^2+1)z + (m-1)^2 \right] + \tau_2 (z-1) + \tau_2 m (z-1)^2}{(z-1)^2} \right\}$$

$$= \frac{K}{\tau_1} (1-A) \frac{1}{z-A} \frac{\alpha z^2 + \beta z + \gamma}{(z-1)^2}$$

where

$$\alpha = T\frac{m^2}{2} + \tau_2 m$$

$$\beta = \frac{T}{2}(2m - 2m^2 + 1) + \tau_2 - 2\tau_2 m$$

$$\gamma = \frac{T}{2}(m-1)^2 - \tau_2 + \tau_2 m$$

$$\theta_e(z) = \frac{2\pi \Delta f T z}{(z-1)^2} \frac{1}{1 + \frac{K}{\tau_1}\frac{(1-A)}{(z-A)} \frac{\alpha z^2 + \beta z + \gamma}{(z-1)^2}}$$

$$= \frac{2\pi \Delta f T z (z-A)}{(z-1)^2 (z-A) + \frac{K}{\tau_1}(1-A)\left[\alpha z^2 + \beta z + \gamma \right]}$$

$$\theta_e(z) = \frac{2\pi\,\Delta f\,T z\,(z-A)}{z^3 + d_2 z^2 + d_1 z + d_0}$$

where

$$d_2 = -2 - A + \frac{K}{\tau_1}(1-A)\alpha$$

$$d_1 = 1 + 2A + \frac{K}{\tau_1}(1-A)\beta$$

$$d_0 = -A + \frac{K}{\tau_1}(1-A)\gamma$$

$$\text{Gain Margin} = -20\log\left[\left|\frac{K}{\tau_1}\frac{(1-A)}{(-1-A)}\quad\frac{\alpha-\beta+\gamma}{4}\right|\right]$$

$$= -20\log\left[\frac{K}{\tau_1}\frac{\tau_2}{2}\right] - 20\log\left[\frac{1-A}{1+A}\right]$$

$$-20\log\left[\frac{\alpha-\beta+\gamma}{2\tau_2}\right]$$

$$\alpha-\beta+\gamma = T\left[\frac{m^2}{2} - m + m^2 - \frac{1}{2} + \frac{m^2}{2} - m + \frac{1}{2}\right]$$

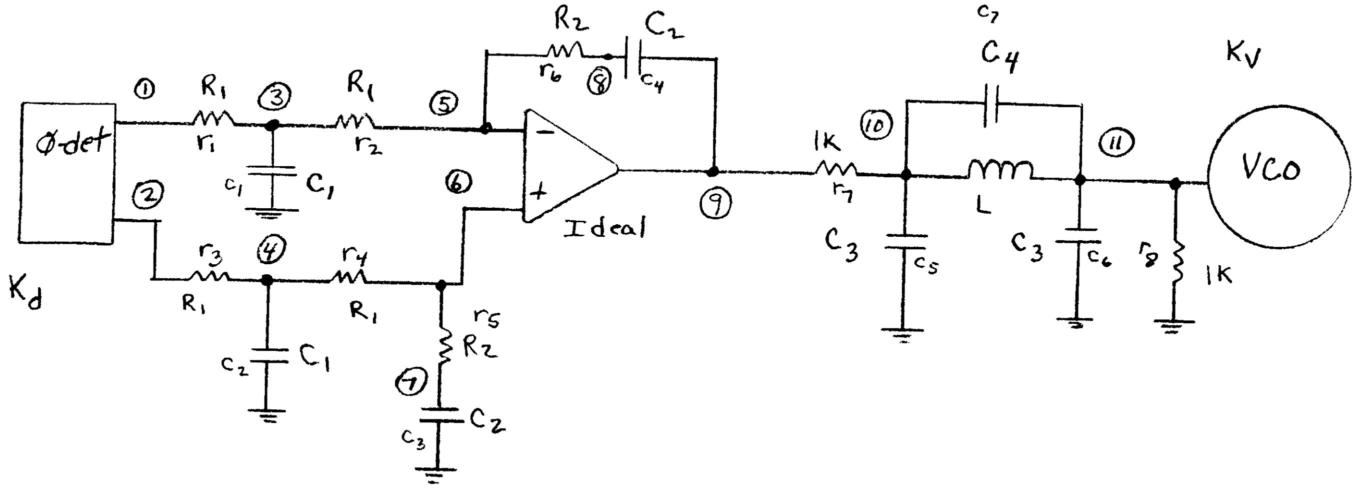
$$+\ \tau_2\left[m - 1 + 2m - 1 + m\right]$$

$$= T\left[2m^2 - 2m\right] + \tau_2\left[4m - 2\right]$$

$$\text{Gain Margin} = -20\log\left[2\pi\zeta\frac{\omega_n}{\omega_s}\right]$$

$$-20\log\left[\frac{1-A}{1+A}\right]$$

$$-20\log\left[\left|2m - 1 + \left(\frac{T}{\tau_2}\right)\left[m^2 - m\right]\right|\right]$$



$$\frac{1}{N}\ \frac{K_d}{2}\ \frac{1}{1+S\frac{\tau_1}{2}}\ \frac{1+S\tau_2}{S\tau_1}\ \frac{K_V}{S}\ \text{Elliptic} = G_{OL}(s)$$

Elliptic has embedded $\frac{1}{2}$ @ D.C.

Take $F_{ref} = 1\text{MHz}$

$K_d = 0.8\ \text{V/Rad}$

$K_V = 25\ \text{MHz}\ 2\pi/\text{V}$

N @ home $= 100$

Hop Δf :

$$\frac{\Delta f}{f_n} = \frac{\pi}{0.45} \cdot N_o = \frac{\pi\ 100}{0.45}$$

(half of possible ϕ-det range)

$$\Delta f = \frac{\pi \cdot 100}{0.45} f_N$$

⊛ or $N_{start} = N_o + \frac{\pi \cdot 100\ f_N}{0.45\ f_s}$

$$= 100 + 700\left(\frac{f_N}{f_s}\right)$$

⊛ $f_n = \left(\frac{K_d K_v}{4N\tau_1}\right)^{1/2} \frac{1}{2\pi}$

Keep K_d, N, τ_1 @ 0.8, 100, $\frac{T_s}{2}$ respectively & change K_v to change f_n

$$4\,\omega_n^2 \frac{N\tau_1}{K_d} = K_V = \omega_n^2 \frac{N}{K_d}\ \frac{4}{2f_s} = 2\pi\,\omega_n \frac{N}{2K_d}\left(\frac{f_n}{f_s}\right)4$$

⊛ $\zeta = \frac{1}{2}\omega_n \tau_2 = 0.75$

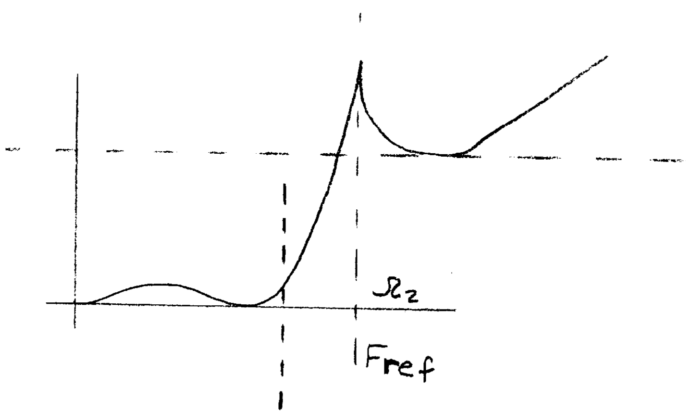
⊛ $C_1 = 500\ \text{pf}$
$R_1 = 1\text{K}$

@ $\zeta = 0.75$, $f_s = 10^6$, $N_o = 100$

$\frac{W_n}{W_s}$	T_2	K_v		N_{start} (max hop without cycle slip)	$C_2 = 1000pf$ R_2
0.01	23.87 μS	314	KHz/V	107	23.87 K
0.02	11.94 μS	1.257	MHz/V	114	11.94 K
0.05	4.77 μS	7.854	MHz/V	135	4.77 K
0.07	3.41 μS	15.4	MHz/V	149	3.41 K
0.10	2.39 μS	31.42	MHz/V	170	2.39 K
0.15	1.59 μS		MHz/V	205	1.59 K

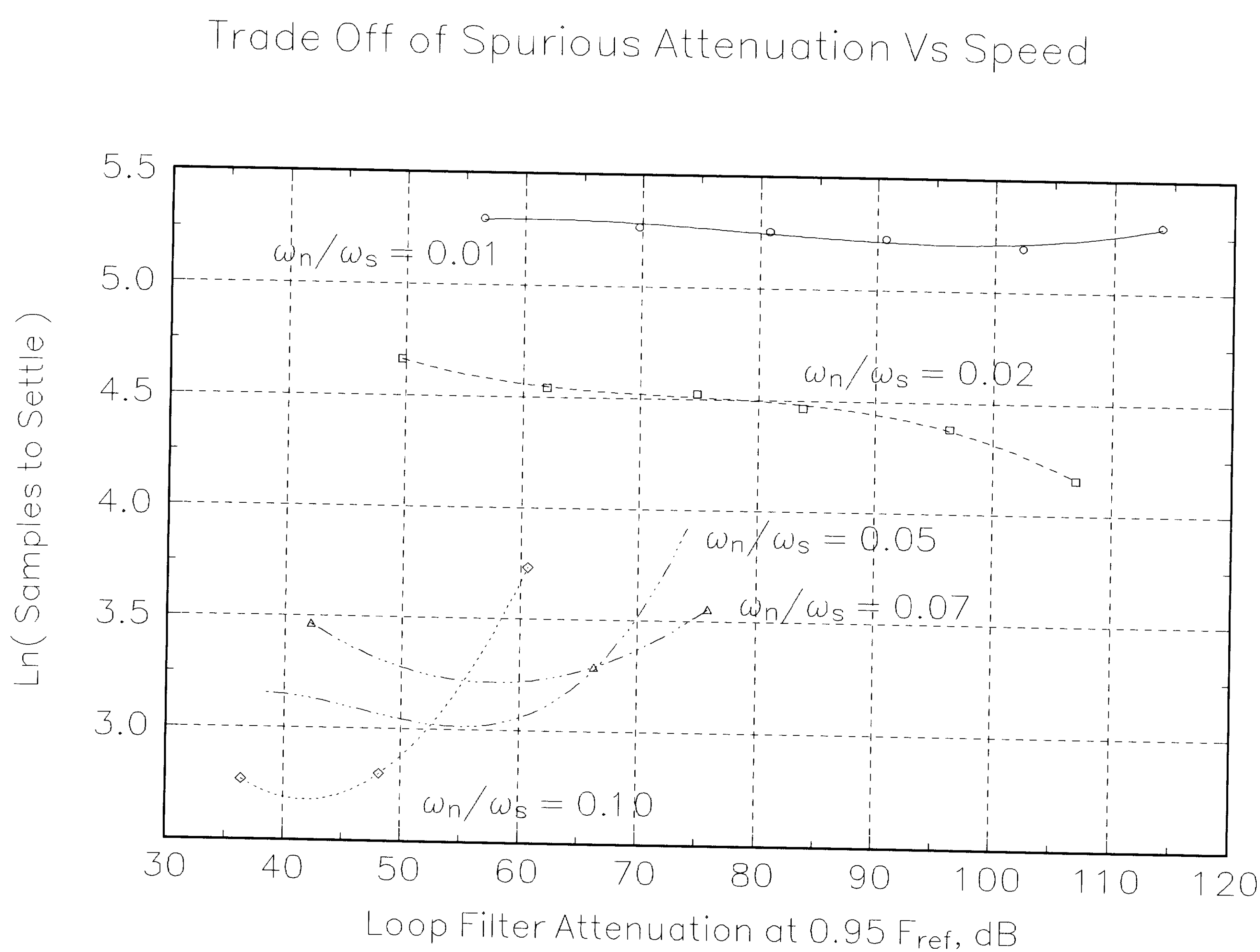
Elliptic Filters

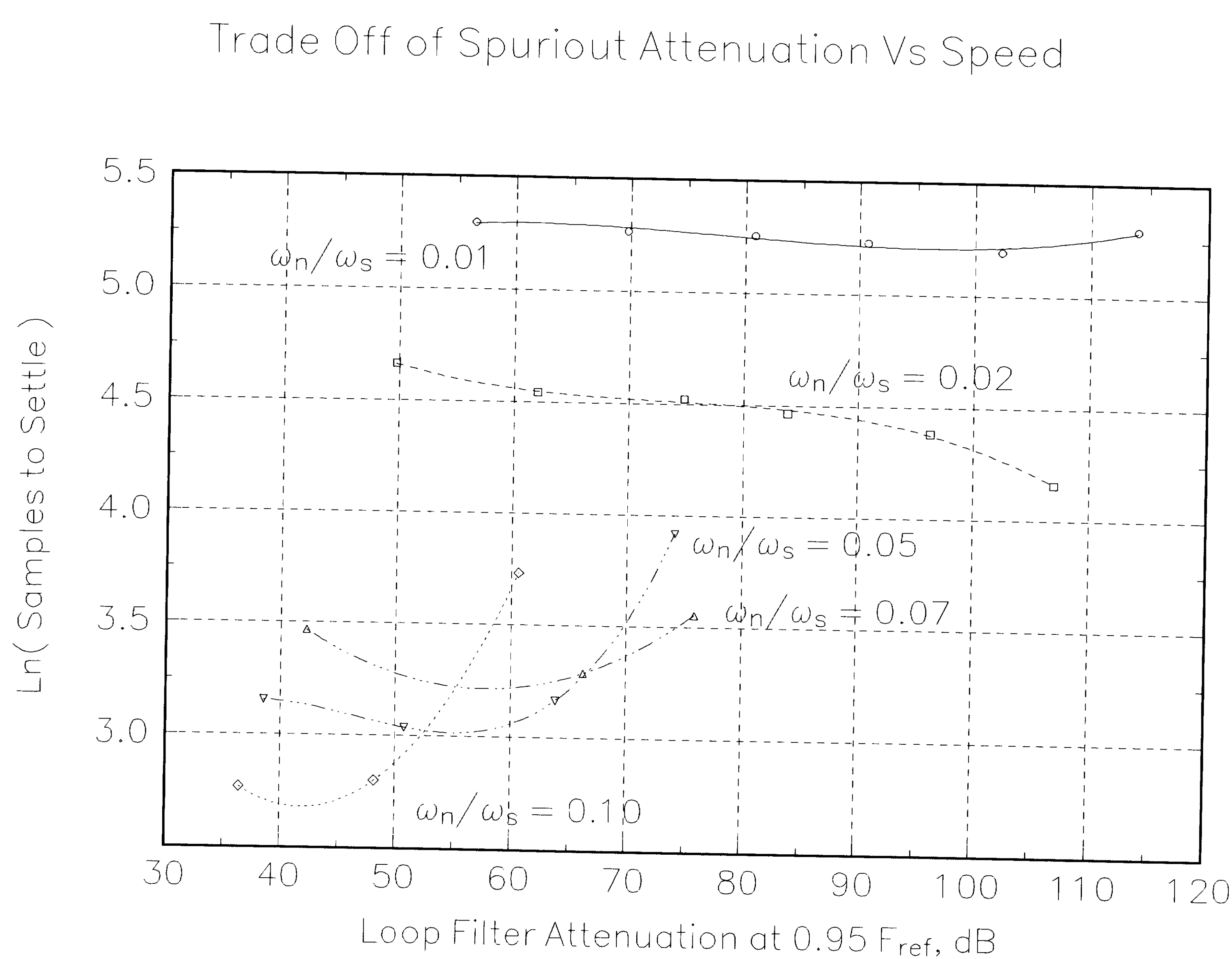
θ	Amin		Ω_2	C03 20
54°	10	dB	1.3498	
38°	20		1.8245	
26°	30		2.6003	
18°	40		3.7137	
12°	50		5.5386	
8°	60		8.2868	



Filters $R_L = R_S = 1K$

θ	C_3	C_4	L
54°	161.96 pf	213.9 pf	118.4 μH
38°	281.3 pf	103.1 pf	245.8 μ
26°	449.2 pf	60.7 pf	417.6 μ
18°	673.5 pf	39.54 pf	640.9 μ
12°	1029 pf	25.56 pf	990 μ
8°	1556 pf	16.89 pf	1504 μ

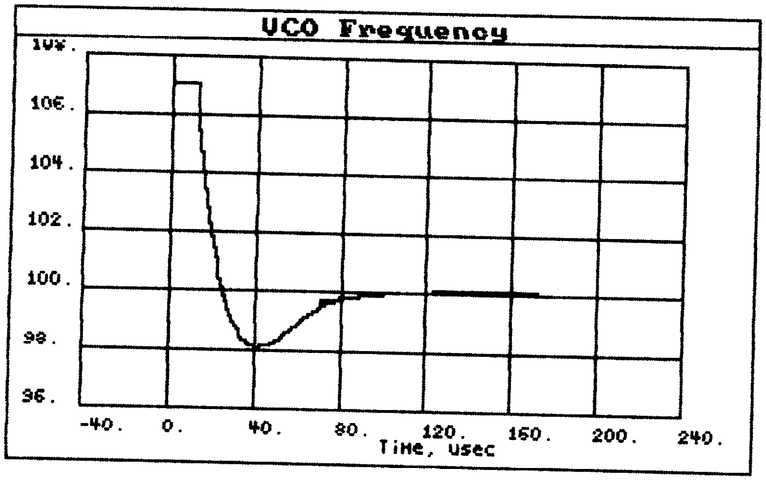

Trade Off of Spurious Attenuation Vs Speed
$\omega_n/\omega_s = 0.01$
$\omega_n/\omega_s = 0.02$
$\omega_n/\omega_s = 0.05$
$\omega_n/\omega_s = 0.07$
$\omega_n/\omega_s = 0.10$
5.5
5.0
4.5
4.0
3.5
3.0
Ln(Samples to Settle)
30
40
50
60
70
80
90
100
110
120
Loop Filter Attenuation at 0.95 F_{ref}, dB

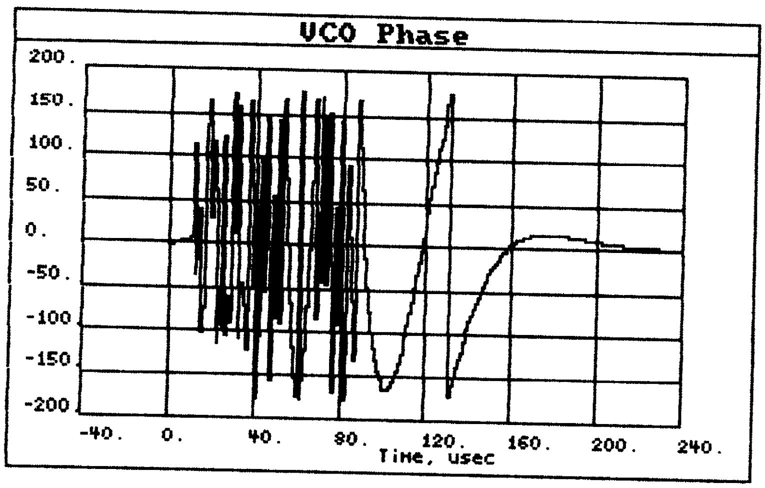

Trade Off of Spuriout Attenuation Vs Speed
5.5
5.0
4.5
4.0
3.5
3.0
Ln(Samples to Settle)
30
40
50
60
70
80
90
100
110
120
Loop Filter Attenuation at 0.95 F_{ref}, dB
$\omega_n/\omega_s = 0.01$
$\omega_n/\omega_s = 0.02$
$\omega_n/\omega_s = 0.05$
$\omega_n/\omega_s = 0.07$
$\omega_n/\omega_s = 0.10$

Results

	Elliptic	W_n/W_s	Gain Mar	Phase Mar	Atten @ 0.95 Fref	% Over-shoot	Settle to < 5°	
1	54°	0.01	33.8 dB	64.4°	56.5	27.4	200 μs	✓
2		0.02	28	62.2	49.7	25	106 μs	✓
3		0.05	19.4	53.9	42.2	30	32 μs	✓
4		0.07	9.5	50	38.5	40.8	23.4	✓
5		0.10	6.4	43.4	36.4	54	15.9	✓
6		0.15						
7	38°	0.01	29.6	63.8	69.7	23	194 μ	✓
8		0.02	23.4	60.0	62.0	24	94 μ	✓
9		0.05	15.1	48.6	54.5	31	30 μ	✓
10		0.07	11.6	41.3	50.8	41.4	20.8	✓
11		0.10	8.8	31.2	48.2	72	16.4	✓
12		0.15						
13	26°	0.01	25.4	62.3	80.8	23	192 μ	✓
14		0.02	19.7	57.1	74.8	24	92 μ	✓
15		0.05	11.2	41.2	66.3	38	26.8 μ	✓
16		0.07	8.0	30.8	63.9	57	23.7	✓
17		0.10	4.0	16.6	60.6	114	41.8	✓
18		0.15						
19	18°	0.01	22.5	60.4	90.7	22	187 μ	✓
20		0.02	16.5	53.2	83.8	26	87 μ	✓
21		0.05	7.75	31.6	75.9	56	35 μ	✓
22		0.07	4.4	17.3	74.1	92	50.3 μ	✓
23		0.10	—	—	—	—	—	
24		0.15	—	—	—	—	—	
25	12°	0.01	19.3	57.3	102.3	23.4	181 μ	✓
26		0.02	13.0	47.0	96.3	30	80 μ	✓
27		0.05	3.75	16.7	88	96	Unstable	
28		0.07	—	—	—	—	—	
29		0.10	—	—	—	—	—	
30		0.15	—	—	—	—	—	
31	8°	0.01	16.5	52.3	114	26	200 μ	✓
32		0.02	9.4	38.0	107	43	64 μ	✓
33		0.05	None	None	95.4	—	—	
34		0.07	—	—	—	—	—	
35		0.10	—	—	—	—	—	
36		0.15	—	—	—	—	—	

Run 1


VCO Frequency
108.
106.
104.
102.
100.
98.
96.
-40.
0.
40.
80.
120.
160.
200.
240.
Time, usec


VCO Phase
200.
150.
100.
50.
0.
-50.
-100
-150
-200
-40.
0.
40.
80.
120.
160.
200.
240.
Time, usec