Phase-Locked Loop Related Terminology & Definitions

References

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2. Crawford, J.A., Frequency Synthesizer Design Handbook, Artech House, 1994.
3. Egan, W.F., Phase-Lock Basics, 2nd ed., John Wiley & Sons, 1998.
4. Gardner, F.M., Phaselock Techniques, 2nd ed., John Wiley & Sons, 1979.
5. Robins, W.P., Phase Noise in Signal Sources, Peter Peregrinus LTD, 1982.

Term	Meaning	Reference
aliasing	Analog signals that are time-sampled at a rate less than the Nyquist sampling rate F_{Nyq} cannot be reconstructed perfectly because frequency components F_{sig} in excess of $F_{Nyq}/2$ are folded (aliased) back in the frequency domain to lie within the range $-F_{Nyq}/2$ to $F_{Nyq}/2$. This folding in the frequency domain is referred to as *aliasing*. The process is described mathematically by the Poisson Sum formula.	[1], Ch. 3, 7
Allan variance	A measure of frequency stability, it is calculated by taking half the mean of the squared difference between two successive measurements of normalized frequency.	[5], Sec. 9.4.2
beat note		[2], p. 388
charge-pump	Prevalent phase detector type in which the output takes the form of pulse-width modulated current pulses. The update rate corresponds to the PLL's reference frequency and the width of the pulses is proportional to the phase error.	[1], Sec. 6.8
closed-loop bandwidth	The –3 dB bandwidth of the transfer function between the VCO's output phase and the input reference phase.	[1], Sec. 6.2
continuous time system	Continuous and differentiable in the mathematical sense. Such systems are not necessarily linear and or time-invariant unless explicitly stated.	[1], Ch. 6
cycle-slipping	All PLLs can be thought of as modulo-2π control systems which attempt to track an input reference signal with minimum error. Normally, if the phase error exceeds the range of $(-\pi, \pi)$, the PLL cannot distinguish the difference leading to an entire cycle being erroneously added or subtracted. This is called cycle-slipping. It is possible to build phase detectors with an extended range [e.g., $(-3\pi, \pi 3)$] but these are rarely seen.	[1], Ch. 10
damping factor	Strictly speaking, only applicable to second-order systems. When the system's transfer function poles and zeros are plotted in the complex plane, the damping factor dictates the angle at which the complimentary poles appear in the left-half place. The quantity is directly related to system stability and phase margin.	[1], Sec. 6.3.2
damping, over	Damping factor value greater than unity. For a second-order system, the poles are both real.	[1], Sec. 6.3.2
damping, under	Damping factor value less unity. For a second-order system, the poles are both complex.	[1], Sec. 6.3.2
damping, critical	Damping factor equal to unity. . For a second-order system, a double real-pole results.	[1], Sec. 6.3.2

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dead zone	Normally meant to describe a phase detector's behavior near zero phase error where the detector's gain is either zero or markedly smaller than it is for larger phase errors.	[1], Sec. 8.7.3
delta-sigma	In PLL work, the delta-sigma concept is used for fractional-N frequency synthesis. The most common configurations used are the MASH and all-zero varieties.	[1], Ch. 8
digital phase locked loop	A PLL which is completely digital in nature, including the oscillator. Z-transforms are used to analyze these PLLs.	[1], Ch. 7
discrete-time system	Synonymous with digital, sampled systems. Analysis is performed using *z*-transforms.	[1], Ch. 7
equivalent noise bandwidth	The bandwidth of an ideal rectangular filter that would exhibit the same noise variance at its output when the input noise power spectral density is uniformly flat.	[3], Sec. 14.1
EVM	Error Vector Magnitude. A measure of signal constellation fidelity that is normally measured in %rms. It contains both AM and PM contributions.	[1], App. 5A
feedback divider	The digital divider normally present in the feedback path of a PLL used in frequency synthesis applications.	[1], Ch. 1
Fokker-Plank techniques	Differential equation methods that can be used to describe the evolution of a probability density function over time such as occurs in a PLL under low signal-to-noise ratio operating conditions.	[3], Sec. 18.1 [1], Ch. 1, 10
fractional-N PLL	Normally found in frequency synthesis applications, the traditional PLL is restricted to output integer-multiples of the applied reference signal. Fractional-N synthesis methods remove this restriction by using analog compensation methods and or digital methods that normally use delta-sigma modulation methods.	[1], Ch. 8 [2], Ch. 9
fractional spurs	Spurious sideband tones in a PLL-based frequency synthesizer output which have an offset frequency of $\chi\ F_{Ref}$ where χ is the fractional portion of the average feedback divide ratio, and F_{Ref} is the reference frequency provided to the PLL.	[1], Ch. 8 [2], Ch. 9
frequency locked loop	A control loop similar to a PLL except that the phase detector has been replaced by a frequency detector.	[2], Ch. 2
gain margin	A term from classical control theory that refers to the additional open-loop gain (dB) that can be added before instability sets in.	[1], Sec. 6.9.2
gain peaking	Directly related to the phase margin present in the PLL, this refers to the maximum closed-loop gain observed in the reference transfer function H_1.	
H_1	The reference port to VCO output port transfer function scaled by (1/*N*).	[1], Sec. 6.2
H_2	The VCO disturbance to PLL output port transfer function.	[1], Sec. 6.2
Haggai phase noise model	A linear model for an oscillator's phase noise spectrum that leads to a Lorentzian power spectral density for phase noise.	[1], Sec. 9.5.2
Haggai loop filter	A method adopted by Haggai for PLLs based on the much earlier work of Bode which can deliver constant phase margin even if the closed-loop bandwidth is changed by two orders of magnitude. Also referred to as a –9 dB/octave loop.	[1], Sec. 6.7
harmonic sampling	Also called sub-sampling. Normally entails sampling a bandpass signal of bandwidth B and center frequency F_o (>>B) with a rate that satisfies Nyquist with respect to bandwidth B. Mathematically described by Poisson Sum formula.	
hold-in range	The range of input frequencies over which a PLL can remain locked.	[3], Ch. 1

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image suppression	In the context of in-phase and quadrature-phase signal conversion, the amplitude and phase balance between the two conversion paths determine how well positive and negative frequencies can be resolved.	[1], App. 5A
injection locking	The entrapment of one oscillator by another when one or both oscillators are near the same frequency or one is near an integer subharmonic of the other.	[1], Ch. 1, Sec. 9.4.2
integrated phase noise	The total phase noise present in the frequency sidebands having frequency offsets spanning from F_L to F_H from the carrier, on both sides.	
Johnson noise	Also referred to as thermal noise. All nonzero resistances above absolute zero temperature exhibit thermal noise.	[1], Ch. 4
Kalman filter	A state-variable filter which updates its state information based upon a priori known characteristics of a system plus incomplete and noise data observations.	[1], Ch. 1
K_d	Phase detector gain, normally having units of A/rad or V/rad.	
K_v	VCO tuning sensitivity, normally having units of rad/s/V.	
lead-lag	A type of PLL loop filter that is seen in most type-2 PLLs. The lead-lag filter is crucial for phase margin. It normally has one pole and one zero associated with it.	[1], Ch. 1, 6
Leeson's phase noise model	The traditional linear model used to characterize oscillator phase noise.	[1], Ch. 9
load pulling	The frequency perturbations to an oscillator when it is subjected to a change in its load impedance.	[1], Sec. 9.4.1
loop order	Refers to the order of the characteristic equation associated with the open-loop gain transfer function. Loop order must be greater than or equal to the loop type.	[1], p. 3
loop SNR	The ratio of signal to noise within a PLL having a given equivalent noise bandwidth.	[3], Sec. 14.2
loop stress	In the case of a type-2 PLL, a leaky integrator or input frequency ramp can lead to a constant nonzero phase error at the phase detector of the PLL that is called loop stress.	
loop type	Refers to the number of ideal integrators in the open-loop gain transfer function.	[1], p. 3
Lorentzian power spectral density	A frequently used power spectral density that is encountered in PLL work with a shape equal to a first-order Butterworth filter having a flat noise spectral density applied at its input. A natural result of the Haggai oscillator model.	[1]
MASH	A type of Δ-Σ modulator known as Multi-stage Noise Shaping.	[1], Ch. 8
maximum a posteriori estimator	An estimation method closely related to maximum-likelihood but most applicable for the estimation of random parameters.	[1], Sec. 1.4.3
maximum likelihood estimator	An estimation method for deterministic parameters which maximizes the probability for a given set of observations.	[1], Sec. 1.4.2
mean-time to slip	The average time for an initially locked PLL to fall out of lock due to poor signal-to-noise ratio conditions.	[1], Ch. 10
minimum mean square estimator	A parameter estimation method that minimizes the squared error. Also called a minimum variance estimator.	[1], Sec. 1.4.1
natural frequency	A key design parameter for all PLLs with units rad/s. Equal to the magnitude of the left half-plane poles in the closed-loop transfer function for the classic type-2 PLL.	[1], p. 228-9
noise peaking	Amplification of the reference port phase noise in a PLL that occurs due to inadequate phase margin in the system.	[1], Ch. 2

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Term	Meaning	Reference
1/f noise	Noise that exhibits a 1/f power spectral density shape that is ubiquitous throughout nature	[1], App. 4B
phase detector figure of merit	A formula first suggested by National Semiconductor for predicting the noise pedestal performance of digital phase detectors, given by $\mathscr{L}_o = FM + 20\log_{10}(f_{\text{VCO}}) - 10\log_{10}(f_{\text{Ref}})$ dBc/Hz in which $\mathscr{L}_o$ is the observed noise level at the locked VCO output, and *FM* is the figure of merit for the phase detector.	[1], Sec. 4.7.4
phase detector, Tri-state	Classical charge-pump output phase detector formed using two flip-flops and one NAND gate.	[1], Sec. 6.8.2
phase jitter	Random variation of an RF signal's phase.	
phase margin	A measure of stability corresponding to the amount of additional phase that can be added to a closed-loop system (all other characteristics remaining unchanged) before the system is unstable.	[1], Sec. 6.9.2
phase noise, flicker FM	Noise having a power spectral density in the phase domain proportional to f^{-3}.	[1], Sec. 4.6.1
phase noise, flicker PM	Noise having a power spectral density in the phase domain proportional to f^{-1}.	[1], Sec. 4.6.1
phase noise, white PM	Noise having a flat power spectral density in the phase domain.	[1], Sec. 4.6.1
phase noise, random walk FM	Noise having a power spectral density in the phase domain proportional to f^{-4}.	[1], Sec. 4.6.1
phase plane analysis	An analysis method normally applied to second-order PLL systems in which the time variable is eliminated and the relationship between phase error and frequency error considered.	[4], Sec. 4.2
Poisson sum	A mathematical result that precisely expresses the relationship between time-sampled and continuous-time domains through *z*-transforms and Laplace transforms.	[1], Ch. 7
post-tuning drift	The slowly changing phase error behavior of some PLLs once lock has been obtained. This is normally the result of capacitor dielectric absorption or bias-point shift, and should not be confused with the phase-tail observed for large damping factor behavior.	[1], Sec. 9.4.4
power spectral density, one-sided	Frequency domain distribution of signal power, limited to positive frequencies.	[1], Sec. 4.3
power spectral density, two-sided	Frequency domain distribution of signal power. A symmetric spectrum, containing positive and negative frequencies. Most useful in mathematical analysis involving the Wiener-Khintchine theorem.	[1], Sec. 4.3
pull-in range	Most often applied to low signal-to-noise ratio applications, the frequency range of mistuning over which a PLL eventually acquires phase lock.	[3], Ch. 8
reference spurs	Unwanted discrete sideband tones that occur at $\pm F_{ref}$ Hz on either side of a PLL's VCO carrier output where F_{ref} is the reference frequency used.	[1], Sec. 4.5.1
residual FM	A measure of phase noise that is closely related to the phase noise power spectral density in the case of widesense stationary random processes.	[1], Sec. 4.6.1

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ring oscillator	A type of oscillator closely related to an RC phase-shift oscillator, composed of cascaded stages of RC and active stages, capable of large frequency tuning ranges but only modest phase noise performance.	[1], Sec. 9.2.2
S-curve	The long-term time-average of a phase-error metric's output versus tracking error that is most frequently encountered in bit synchronization work where random data transitions are involved. The slope of the S-curve at zero error is gain parameter for the phase-error metric.	[1], Sec. 10.5
settling time	The time required for a PLL to respond to a specified initial error in phase and or frequency, and achieve a specified measure of steady-state error in phase or frequency.	[1], Sec. 2.1 [3], Ch. 8
single sideband noise	The mean-square phase deviation in radians of noise relative to the carrier in a single sideband.	[1], Sec. 4.6 [3], Sec. 11.6.2
spurs	A generic term for the single frequency unwanted tone outputs seen at the VCO output in a PLL.	
sum loop	Used heavily by Hewett-Packard in its synthesizer products through the 1980s and 1990s. A single PLL which is normally used to frequency-sum a low-frequency source with a high-frequency source, effectively using the PLL to eliminate the unwanted positive or negative frequency mixing product.	
threshold	The input signal-to-noise ratio to a PLL frequency demodulator for below which the output SNR falls rapidly for decreasing input SNR. Although arbitrary, threshold has been sometimes defined as that input SNR for which the output SNR is 1 dB poorer than linear theory would predict.	[4], Sec. 9.3 [3], Sec. 17.6.3
Tikhonov probability density function	The phase error probability density function associated with a type-1 PLL analyzed using Fokker-Planck techniques; closely related to the Gaussian distribution for moderate loop SNRs.	[1], Ch. 1 [3], Ch. 18
time jitter	Random excursions in the zero-crossings of a periodic signal normally attributed to phase noise.	
unity-gain closed-loop bandwidth	The frequency at which the closed-loop gain for the reference path is zero dB.	[1], Ch. 6
unity-gain open-loop bandwidth	The frequency at which the open-loop gain exhibits unity gain (0 dB).	[1], Ch. 6
VCO	Voltage controlled oscillator	
VCO pulling	Frequency and or phase perturbations to a VCO's normal output signal due to load impedance changes.	[1], Sec. 9.4.1
VCO pushing	Frequency and or phase perturbations to a VCO's normal output signal due to small changes in its supply voltage.	[1], Sec. 9.4.3

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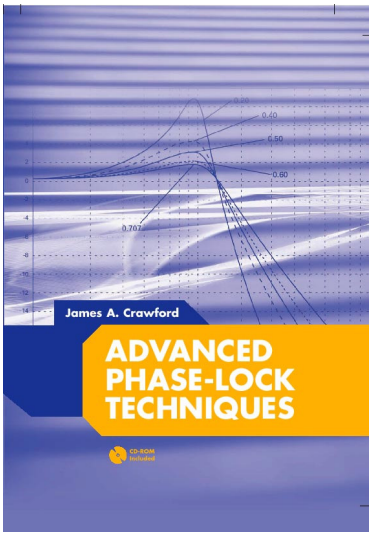

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James A. Crawford

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3	*Fundamental Limits* A detailed discussion of the many fundamental limits that PLL designers may have to be attentive to or else never achieve their lofty performance objectives, e.g., Paley-Wiener Criterion, Poisson Sum, Time-Bandwidth Product.	38
4	*Noise in PLL-Based Systems* An extensive look at noise, its sources, and its modeling in PLL systems. Includes special attention to 1/*f* noise, and the creation of custom noise sources that exhibit specific power spectral densities.	66
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