Part 2

Extending sampling to Type II phase-locked loops

The theory behind sampled control loops established in Part 1 of this series of articles may be extended to encompass the Type II PLL as well.

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TRUE sampling's benefits for PLL synthesizers were introduced last month in Part 1. The stability requirements and transient response of a Type I control-loop were examined by using Z-transforms. In this concluding article, similar expressions are derived for the more-popular Type II control loop, and the Z-transform analysis is extended to permit a detailed examination of the output phase-noise spectrum from a sampled PLL synthesizer.

The open-loop gain for the ideal Type II control loop is

$$G_{o1}(S) = \frac{K_d}{N}\,\frac{1-e^{-ST}}{S}\,\frac{1+S\,\tau_2}{S\,\tau_1}\,\frac{K_v}{S} \qquad (29)$$

where $\tau 1$ and $\tau 2$ are the ideal integrator time constants. This expression may be restated using Z-transforms in the same way as for Type I loops:

$$G_{o1}(Z) = \frac{K_d\,K_v}{N\,\tau_1}\,Z\left\{\frac{1+S\,\tau_2}{S^3}\right\} = \frac{K_d\,K_v\,T[(T/2+\tau_2)\,Z+(T/2-\tau_2)]}{N\,\tau_1\,(Z-1)^2} \qquad (30)$$

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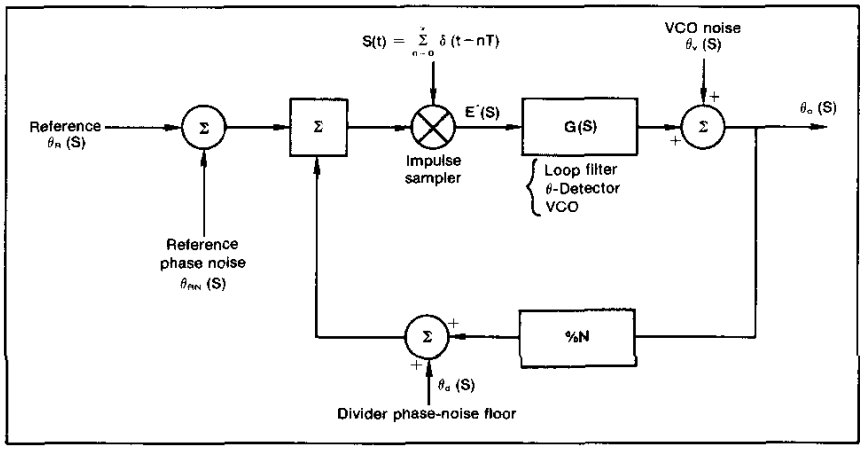

4. The sampled PLL is quite similar to the continuous type, *except for the inclusion of the impulse sampler and internal hold function.*

Using this equation, the loop response to a step change in input frequency, ΔF, may be found using the standard approach from Eq. 16. After substituting Eq. 30 into Eq. 16, the final error response is the result:

$$E(Z) = \frac{2\,Pi\,\Delta F\,T\,Z}{N}$$

$$\{Z^2+Z[K(T/2+\tau_2)/\tau_1-2]$$
$$+[1+K(T/2-\tau_2)/\tau_1]\}^{-1} \quad (31)$$

where

$$K = \frac{K_d\,K_v\,T}{N}$$

The Type II system will also phase-lock with a zero-beat response provided the conditions in Eqs. 32 and 33 are met:

$$K\,(T/2+\tau_2)/\tau_1 = 2 \quad (32)$$

$$K\,(T/2-\tau_2)/\tau_1 = -1 \quad (33)$$

Both of these conditions can be met by selecting the time constants in the ideal lead-lag filter as follows:

$$\tau_2 = 3/2\,T \quad (34)$$

$$\tau_1 = K_d\,K_v\,T^2/N \quad (35)$$

In terms of the more traditional quantities (natural frequency and damping factor), these optimum conditions for phase-lock dictate a natural frequency of $1/(2\pi T)$ Hz and a damping factor of 0.75. In the ideal case, if these relationships between loop parameters are met, the phase-error response will simply be a delta function.

$$E(Z) = \frac{2\,Pi\,\Delta F\,T}{N\,Z}$$

$$e(nT) = \frac{2\,Pi\,\Delta F\,T}{N}\,S\,(t-T)\ \text{Radians} \quad (36)$$

If these parameter choices for $\tau 2$ and $\tau 1$ are not met exactly, the error response will require more sample periods to settle to a prescribed degree of phase-lock. In this more general situation, the phase detector angular error as a function of time is

$$e(nT) = \frac{2\,Pi\,\Delta F\,T}{N\,(a-b)}\,[a^n-b^n]\ \text{Radians} \quad (37)$$

where

$$a = \frac{A+\sqrt{A^2-4B}}{2}$$

$$b = \frac{A-\sqrt{A^2-4B}}{2}$$

$$A = 2-K\,(T/2+\tau_2)/\tau_1$$

$$B = 1+K\,(T/2-\tau_2)/\tau_1$$

Both a and b are complex numbers that cause the time response to have the appearance of a damped sinusoid.

Synthesizer phase noise

Phase-noise performance of a candidate PLL synthesizer may be accurately predicted using basic control theory concepts. This is possible because the noise contributions are typically very small compared to the desired signal, and because the effects of each noise source can be considered separately. A basic PLL synthesizer structure is shown in Fig. 4, including the two most important noise sources generally considered. Other noise sources could be added as well. For instance, the loop filter exhibits 1/f noise caused by DC amplifiers. This source is generally ignored except in special cases, and the noise could be conveniently expressed in terms of an equivalent phase-noise term entering

the phase detector.

It is wise at this point to solve for the error function, E*(s):

$$E^*(S) = \left[\theta_R(S) - \theta_{RN}(S) - \frac{\theta_o(S)}{N} - \theta_D(S)\right]^* \quad (38)$$

The reference phase term may be ignored for the purpose of noise analysis. This slightly simplifies Eq. 38 as

$$E^*(S) = \theta^*_{RN}(S) - \theta^*_D(S) - \frac{E^*(S)G^*(S) + \theta^*_v(S)}{N}$$

$$= \frac{\theta^*_{RN}(S) - \theta^*_o(S) - \theta^*_v(S)/N}{1 + \frac{G^*(S)}{N}} \quad (39)$$

Each noise term can be considered to be uncorrelated with respect to the other noise sources. Therefore, each term may be considered independently and the resulting noise powers added together. The effect of reference noise on the output phase noise can be found from Eq. 39:

$$\theta_o(S)\Big|_{Ref} = \frac{\theta^*_{RN}(S)\ G(S)}{1 + \frac{G^*(S)}{N}} \quad (40)$$

In general, the phase detector cannot differentiate between feedback divider noise and reference-generated noise. The feedback contribution to the output phase noise is given by an analogous expression as Eq. 40. The VCO phase-noise contribution at first glance appears to be equally simple to compute. Beginning as before with the expression for E*(s), the resulting contribution to the output system phase noise is

$$\theta_o(S)\Big|_{vco} = \theta_v(s) - \frac{\theta^*_v(S)\ G(S)\ /N}{1 + \frac{G^*(S)}{N}}$$

$$= \frac{\theta_v(s) + [\theta_v(S)G^*(S) - \theta^*_v(S)\ G(S)]/N}{1 + \frac{G^*(S)}{N}} \quad (41)$$

The bracketed numerator quantity cannot be assumed to cancel to zero, although this is precisely what would occur in a continuous loop analysis. However, for small loop bandwidths as compared to the reference frequency, the bracketed quantity may be readily ignored. The same is true in cases where the VCO spectrum is exceptionally clean at frequency offsets greater than 0.5 F_{ref}. In most cases, the VCO phase-noise contribution at the output can be closely approximated by

$$\theta_o(s)\Big|_{vco} = \frac{\theta_v(s)}{1 + G^*(s)/N} \quad (42)$$

Equations 40 and 42 may be used to express concisely the power spectral density at the synthesizer output caused by the reference phase-noise source and the VCO's internally generated noise. The spectral density contribution from the reference and VCO noise powers may be calculated from Eq. 43 and 44:

$$\frac{S_o(\omega)}{S_{RN}(\omega)} = \frac{16\ K^2\ N^2\ \sin^4(\omega T/2)}{(\omega T)^4\ (K^2 + 2 - 2K + 2(K-1)\cos(\omega T)} \quad (43)$$

$$\frac{S_o(\omega)}{S_v(\omega)} = \frac{4\ \sin^2(\omega T/2)}{K^2 + 2 - 2K + 2(K-1)\cos(\omega T)} \quad (44)$$

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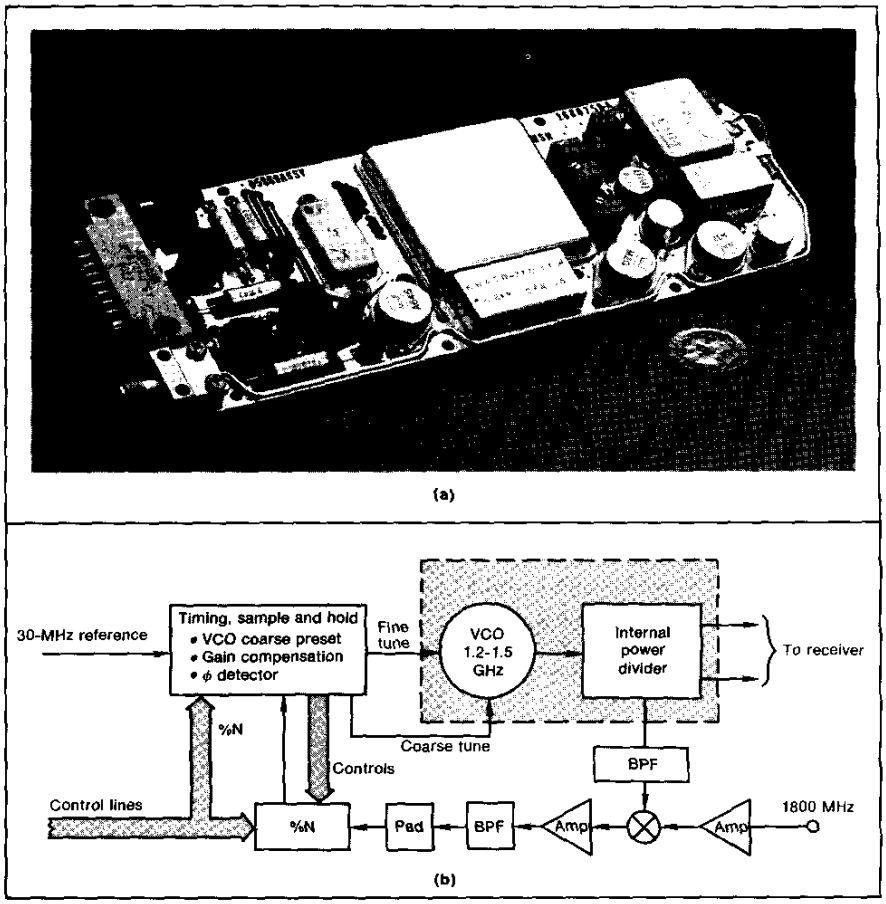
These two equations become very simple where K = 1. The term K, as defined in last month's article (Eq. 19), equals K_dK_vT/N.

Many other factors must be included in the actual design of a sampled phase-locked loop. Features that have not been addressed include time delay in the loop, the finite gain-bandwidth product of lead-lag filters, and inefficient sampling by the phase detector.

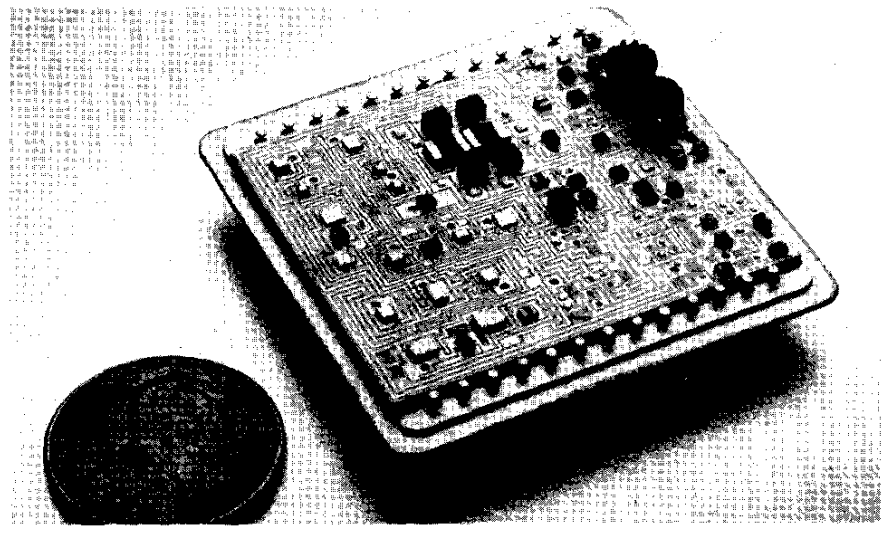
Because of the sampling features of the control system, any frequency component that is not a coherent multiple of the reference frequency will be folded into the baseband, causing spurious output responses. The reference signal in particular must be devoid of any nonharmonically related components. Gain distribution in the loop is also critical to ensure low sampling spurs. The largest phase-detector gain that still provides adequate capture range should be used. Computer-aided analysis has shown that near zero-beat responses are more easily obtained with Type I loop architectures than with Type II architectures. Phase-locking time for the Type II loop was generally twice that required for the Type I system. The Type I loop is ideal for many communications systems, but if VCO post-tuning drift is present, a Type II architecture may be required. The Type I architecture provides no guard against the effects of post-tuning drift.

The design concepts presented in these two articles have been implemented in a synthesizer (Fig. 5a) which will provide the LO function in the JTIDS program. A block diagram of the synthesizer is shown in Fig. 5b. The synthesizer uses a high-side mixing operation to bring the 1.2-to-1.5-GHz synthesizer output frequency range to within the range of available ECL dual modulus dividers. The VCO was designed for excellent linearity (typically within 1 percent) and level output power (typically within ±1 dB) over the required temperature range. The heart of the synthesizer is the large timing-sample-and-hold hybrid. This hybrid performs the VCO coarse-tuning, dynamic loop gain compensation, and critically clean phase detector/sampling function. The sampling operation is not followed by filtering to reduce spurs, because this would also decrease phase-locking speed.

The unsealed timing-sample-and-hold hybrid is shown in Fig. 6. Approximately 22 ICs, 35 transistors, 60 resistors, and 45 capacitors have been packaged into the 1.6-in. × 1.6-in. unit. The hybrid provides its own power-supply grooming in critical areas, and all signals to and from its interface are appropriately buffered to minimize interactions with external factors. ●●



5. This L-band synthesizer was developed for the Navy *and will serve as the synthesizer LO in the JTIDS program.*



6. The timing-sample-and-hold hybrid *contains 22 ICs, 35 transistors, 60 resistors, and 45 capacitors packaged in an area 1.6 in. (10.3 cm) square. It performs VCO coarse-tuning, dynamic loop gain compensation, and the phase detector sampling function.*