Charge-Pump Noise Model for PLLs

I've spent a few moments here contemplating the form of the phase noise model being used by National Semiconductor and others. Specifically, National models the phase detector noise contribution at a PLL's output as:

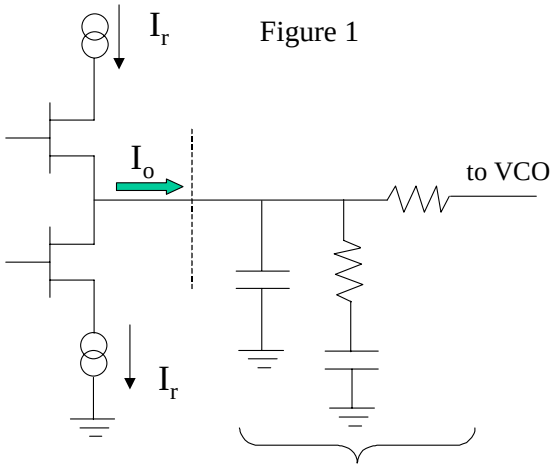
$$\mathcal{L}_o = -213\frac{dBc}{Hz} + 20\log_{10}\left(F_{out}\right) - 10\log_{10}\left(F_{compare}\right) \quad [1]$$

In the case of a 1 GHz output, 30 kHz comparison frequency, $\mathcal{L}_o = -77.8$ dBc/Hz . (Historically I have used –211 + margin for the Platinum series, but I just found a National applications article using the –213 value.)

The real question being asked is why the 10 $\log_{10}$( ) dependency with respect to the phase detector comparison frequency.

A very simplistic view of the charge-pump output is provided here in Figure 1 below.

Figure 1 Simple Model for Phase/Frequency Output Charge-Pump



In steady-state closed-loop operation, the plot of current flow versus time looks crudely something like that shown in Figure 2. The closer that the "+" and "-" current flow regions come to overlapping in Figure 2, the less glitch energy at the phase detector output there will be to aggravate the reference spurs / sideband issue. This can be easily argued by computing the Laplace transform of one reference period as

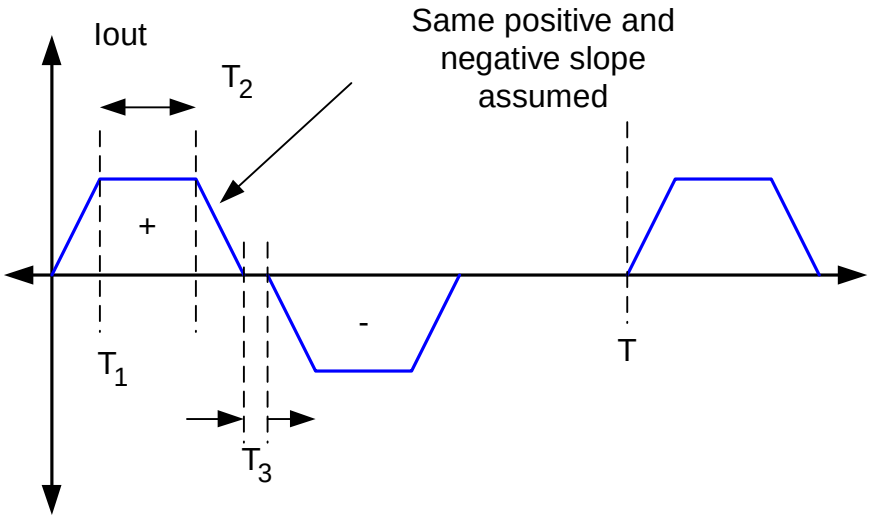
$$p(s) = g(s)\left[1 - e^{-s(2T_1+T_2+T_3)}\right] \quad [2]$$

where

$$g(s) = \alpha\frac{1 - e^{-sT_1} - e^{-s(T_1+T_2)} + e^{-s(2T_1+T_2)}}{s^2} \quad [3]$$

and α is the slope of the posive trapezoidal edge in A/sec units. We want to focus on the noise behavior however, so we will not take this portion of the discussion any further.

Figure 2 Simple Model for Output Current Pulses from Charge Pump



Whenever direct current flows (I_r), shot current will be present having an rms value of $\sqrt{2qI_r}$ where q is the charge of an electron. Resistances of course exhibit Nyquist noise that will have an rms value of $\sqrt{4kTR}$ in a 1 Hertz bandwidth where k is Boltzmann's constant. Accurate models for FET noise etc. are readily available in the literature[1] (in particular, the shot current in an FET is also dependent on g_m).

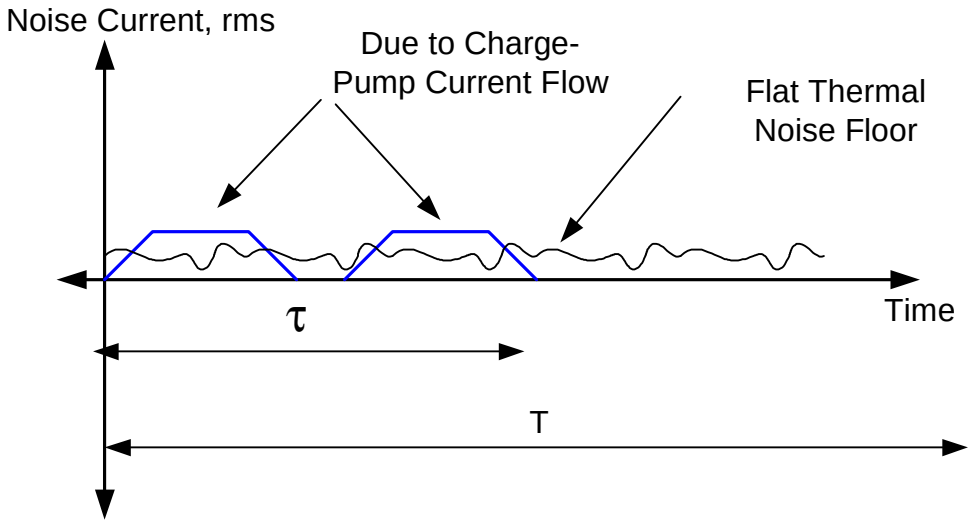
The key point here is that the noise scenario looks something like that shown in Figure 3. Clearly, the "flat" noise floor level is present all of the time. Even if it is interrupted during the charge-pump action during each reference period, the change in the observed (flat) noise power will be nonperceptable because $\tau << T$. The charge-pump noise current is another matter.

If the two FETs in Figure 1 are really well designed, and the drive circuitry to the gates does not leak to the I_o current output, it is reasonable that the flat noise floor can be made almost as low as theory will allow. In any case, this noise mechanism is virtually independent of the phase comparison frequency again because $\tau << T$.

For the shot-noise current portion that is due to the on-times of the current sources, the situation is different. We can estimate the magnitude of the noise current as $I_n = \sqrt{2qI_r}$. The observed output noise power (in a 1 ohm load) due to this noise current source is then

[1] G. Massobrio, P. Antognetti, Semiconductor Device Modeling with Spice, 2nd Ed., McGraw-Hill, 1993; P.R. Gray, R.G. Meyer, Analysis and Design of Analog ICs, John Wiley and Sons, 1977

Figure 3 Noise Sources at Charge-Pump Output



$$p \approx I_n^2 \frac{\tau}{T} = 2qI_r\left(\frac{\tau}{T}\right) \qquad [4]$$

where this contribution is clearly duty-cycle dependent, or dependent on $F_{compare}$ (assuming that τ is constant). This form shows a 3 dB change per comparison frequency octave (rather than 6 dB) because it is power rather than voltage. In terms of "phase noise", at the phase detector output, we have roughly

$$\sigma_\theta^2 \approx FlatNoise + \frac{8\pi^2 q\tau F_{compare}}{I_r} \quad \frac{rad^2}{Hz} \qquad [5]$$

Putting in some "real numbers"

$$\begin{aligned} q &= 1.602 * 10^{-19}\ coul. \\ \tau &= 20 \quad n\sec \\ F_{compare} &= 30 \quad kHz \\ I_r &= 4 \quad mA \end{aligned} \qquad [6]$$

we observe that $\sigma_\theta^2 = 1.9\ 10^{-18}$ which corresponds to an output phase noise floor (due to the shot noise current) of –179 dBc/Hz. Comparing this result to the noise model given for the National Semiconductor Platinum PLL device family [1], at a 1 GHz output, that equation evaluates to –168 dBc/Hz at the phase detector floor. Therefore, this very crude simple analysis comes within about 10 dB of what we actually see with the National devices, neglecting the flat noise floor which has not been included yet. More importantly, we have the phase detector referred noise floor due to this shot current given by

$$\mathcal{L}_o = 20\log\left(\frac{\sigma_\theta}{\sqrt{2}}\right) \quad \frac{dBc}{Hz}$$
$$= 20\log\left[\sqrt{\frac{8\pi^2 q\tau F_{compare}}{2I_r}}\right]$$
$$= 20\log\left[\sqrt{\frac{8\pi^2 q}{2I_r}}\right] + 10\log\left(\tau F_{compare}\right) \qquad [7]$$
$$= \alpha_o + 10\log\left(\tau F_{compare}\right) \quad \frac{dBc}{Hz}$$

In this result, α_o is like a noise figure of merit for the phase detector output which remains constant, but clearly, the 10log( ) dependency on the phase comparison frequency is now clearly visible.

Conclusion

Any noise source that is gated "on" during the "+" and "-" switching intervals in Figure 2, whether due to shot-current, power supply, or other sources, has its impact at the phase detector output scaled (in power) by the duty factor, d= τ/T. Therefore, the 3 dB per octave behavior observed for phase noise performance versus the phase-comparison frequency will always be observed whenever the noise during the "+" and "-" switching intervals is much greater than the flat noise floor that is present continuously.

This model suggests that the only way to improve the overall phase noise performance of the phase detector (when the 3 dB/octave phenomenon is occurring) is to reduce the noise contributions during the "+" and "-" time intervals.

If this 3 dB per octave behavior with phase comparison frequency is not seen in a candidate phase detector, more than likely the flat noise sketched in Figure 3 is higher than the duty-factor weighted "+" and "-" noise source, and additional corrective design steps are needed to reduce the flat noise sources.

