A GSM MODULATOR USING A ΔΣ FREQUENCY DISCRIMINATOR BASED SYNTHESIZER

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ABSTRACT

This paper describes a new transmitter architecture suitable for GSM modulation. The technique is based on direct modulation of a high resolution ΔΣ frequency discriminator based synthesizer to produce the modulated RF signal without any up-conversion. The advantage of this architecture is that it does not require mixers or D/A converters to generate the In-phase and Quadrature signals as in conventional GSM transmitters. This eliminates many of the analog problems associated with mixing and filtering and results in an architecture suitable for monolithic integration.

1. INTRODUCTION

Conventional GSM transmitters utilize quadrature amplitude modulation (QAM) with In-phase (I) and Quadrature (Q) signals that are mixed with a local oscillator operating at the carrier frequency. A typical system is shown in Fig. 1, where the baseband I and Q data is converted to analog and mixed with a local oscillator [1]. This method, although viable, requires

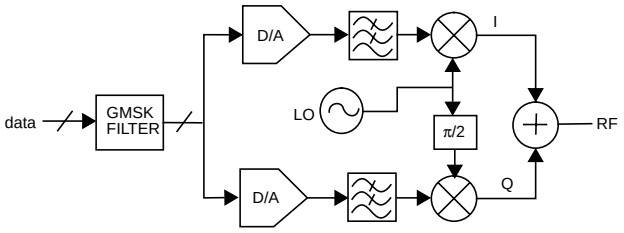

Fig. 1. GSM modulator using quadrature amplitude modulation (QAM).

mixers, filters and D/A converters to up-convert the baseband I and Q signals to the RF carrier frequency. It is difficult to realize the required analog filters in monolithic form so the system becomes complex and costly.

A more elegant solution shown in Fig. 2 is direct modulation of a high resolution ΔΣ synthesizer as described in [2]. In this architecture, the phase-locked loop (PLL) closed-loop bandwidth is narrow (compared to the reference frequency) to satisfy the PLL noise requirements. This restricts the modulating signal bandwidth since the PLL can only readily track

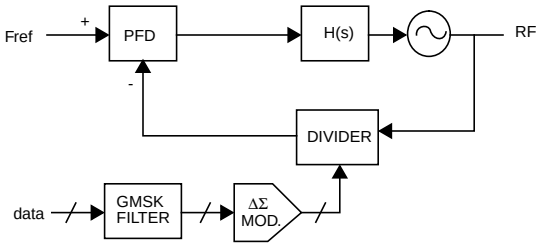

Fig. 2. Direct modulation of a ΔΣ synthesizer.

frequencies within its bandwidth so this architecture is only suitable for narrow-band modulation.

An alternative for wide-band modulation is to break the loop during transmission. Then the modulation is limited only by the VCO and power amplifier bandwidth. This technique has been used for DECT (Gaussian frequency shift keyed modulation) in [3] where the transmission data bursts are relatively short and accurate phase control is not required. The problem with opening the loop is that the VCO is free-running and will drift over time with no phase noise suppression. Another difficulty is avoiding switching transients while breaking the loop. A transient while opening the loop results in a frequency channel offset error during the transmit time.

Wide-band modulation of a closed loop is possible if some form of compensation is used to overcome the natural roll off of the PLL loop bandwidth. One method proposed in [4] uses an equalizer to compensate for the limited PLL loop bandwidth as shown in Fig. 3. In principle equalization is possible as long as the true PLL characteristics are known. This tends to be the pitfall since

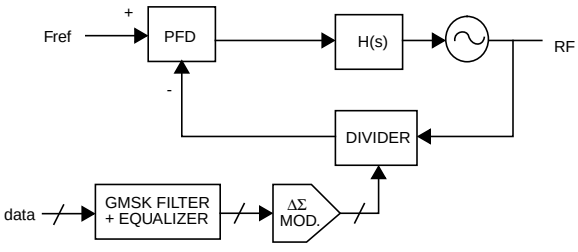

Fig. 3. Equalized direct modulation of a ΔΣ synthesizer.

this PLL contains analog filters which cannot be realized to close specifications and therefore the necessary equalization transfer function is not known. The synthesizer proposed in [5] is a better architecture to use with equalization since it incorporates mostly digital signal processing which has predictable transfer functions to use in designing the equalizer.

2. GSM MODULATOR ARCHITECTURE

The proposed modulator architecture is a variant of the ΔΣ frequency discriminator based synthesizer first reported in [5] and illustrated in Fig. 4.

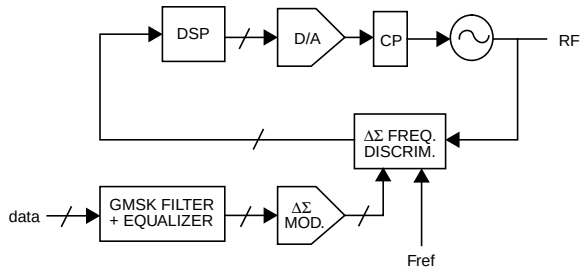

Fig. 4. Equalized direct modulation of a ΔΣFD based synthesizer.

The new synthesizer, as in [5], uses a ΔΣ frequency discriminator (ΔΣFD) [6],[7] in the feedback path to convert the VCO frequency into an oversampled bitstream. Thus the ΔΣFD serves as a frequency discriminator and A/D converter which replaces the divider and phase detector in conventional ΔΣ synthesizers. The operation is similar to [5] except that the ΔΣFD output contains only the error between the VCO and desired channel frequency as opposed to the dc channel offset plus error. This is accomplished by modulating the base modulus of the ΔΣFD, as shown in Fig. 5, where before it was set to a constant value.

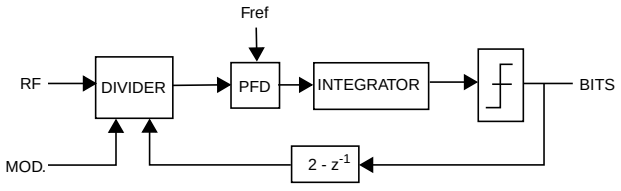

Fig. 5. ΔΣ frequency discriminator with external modulation control.

The advantage of controlling the ΔΣFD directly is that there is no need to decimate and filter the bitstream before comparing it to the desired channel as in [5]. This reduces the dynamic range requirements of the digital signal processing (DSP) in the loop since the input signal is only one bit wide. Another benefit is that ΔΣ modulators (including ΔΣFD's) may suffer from idle tones with dc (constant frequency for ΔΣFD's) inputs. Modulating the ΔΣFD keeps the discriminator busy which suppresses any idle tones. The problem with this approach is that the desired channel is a high resolution value while the ΔΣFD modulus input can only accept integer values. The mechanism to convert from a high resolution channel into a low resolution modulus is by remodulating with a digital ΔΣ modulator. If the synthesizer is used as a local oscillator (LO), the input to the ΔΣ modulator would be the constant channel value while its output would dither between integer values whose average value represents the channel. Similarly, modulation of the synthesizer is possible if the ΔΣ modulator input is time varying according to the data. The same narrow-band modulation limitations apply to this architecture as for the architecture of Fig. 2, [2], since it too has a relatively narrow loop bandwidth to satisfy phase noise requirements. However, as proposed in [4], it is possible to equalize the effects of the PLL bandwidth by compensation in this case as the PLL is mostly digital and an exact equalizer can be realized.

3. DESIGN PARAMETERS

Determining the PLL loop parameters requires that an adequate model be developed. In this case we have modulation requirements to consider in addition to the phase noise and transient characteristics of a basic synthesizer. It is useful to analyze this mixed mode (continuous-time and discrete-time) synthesizer in the S-domain and Z-domain although a pure Z-domain model could also be used. Fig. 6 shows a simplified model of the synthesizer without the modulation blocks.

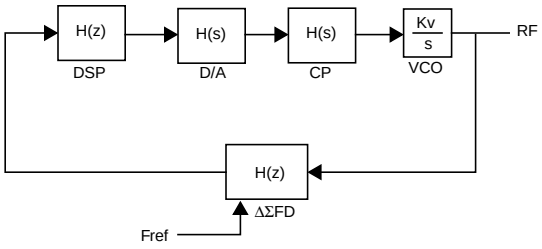

Fig. 6. Linearized equivalent model of ΔΣFD based synthesizer.

From this model, the stability and transient characteristics may be determined. The loop stability is best determined through the use of open-loop Bode plots which quickly reveal the gain and phase margins even though the system is mixed mode.

The performance of the synthesizer as an LO may be adjusted from these loop parameters. Once the synthesizer has met the phase noise and transient settling specifications, the design of the modulator can proceed. The general idea is to inject the modulation data and compensate for the tendency of the PLL to suppress any signal outside of its loop bandwidth. This implies that in

addition to the Gaussian minimum shift keying (GMSK) filter, an equalization filter is necessary with a response that is the inverse of the PLL closed-loop transfer function seen by the modulation data. The result is a modulation bandwidth that is larger than the PLL bandwidth as shown in Fig. 7.

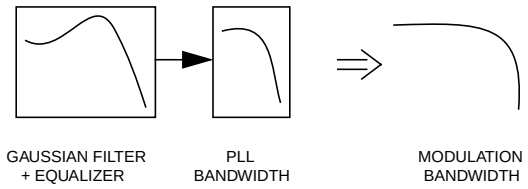

Fig. 7. Effect of equalizer on modulation bandwidth.

The equalization of the PLL closed loop response increases the dynamic range of the data but this is easily handled by extending the input range of the ΔΣ modulator.

4. PHASE NOISE

The synthesizer phase noise requirements determine the PLL loop bandwidth while switching speed is a secondary issue usually controlled by other means. Typically, due to VCO noise, a wide loop bandwidth is required while a narrow one is needed to adequately suppress the ΔΣ quantization noise from the ΔΣFD. For this design, the reference frequency (also the sampling frequency) is 13MHz and a suitable loop bandwidth is 30KHz. The phase noise is modeled as the sum of ΔΣFD quantization noise, charge pump noise and VCO phase noise, all output referred. This represents the major noise sources and gives a reasonable prediction of the actual synthesizer phase noise. Fig. 8 shows the simulated phase noise compared to the GSM phase noise spectral mask.

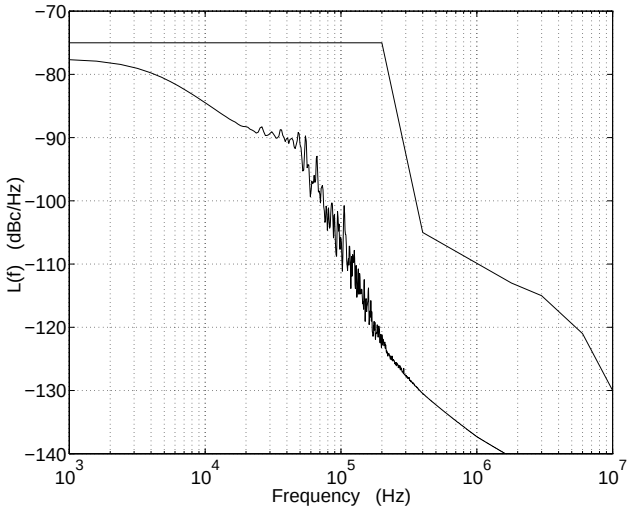

Fig. 8. Phase noise of ΔΣ frequency discriminator based synthesizer.

The PLL bandwidth is set to a value that adequately filters the ΔΣFD quantization noise to give acceptable phase noise performance. Reducing it any further would compromise the transient characteristics of the synthesizer (i.e. slower switching speed). If fast switching speed is necessary, the loop dynamics can be varied while switching channels to improve acquisition. This technique has been done in analog PLL synthesizers by dynamically changing the loop filter parameters, but care must be taken to ensure a smooth transition occurs to prevent erroneous RF output frequencies [8]. Since the synthesizer loop filter in this architecture is predominantly digital, the loop dynamics may be varied with complete control avoiding any output transients.

5. GSM OUTPUT SPECTRUM

The spectral requirements of a GSM modulated carrier are quite stringent due to the narrow channel spacing. Without careful spectral control, excessive RF power would spread into adjacent channels. Fig. 9 shows the GSM modulated RF carrier spectrum with random data input.

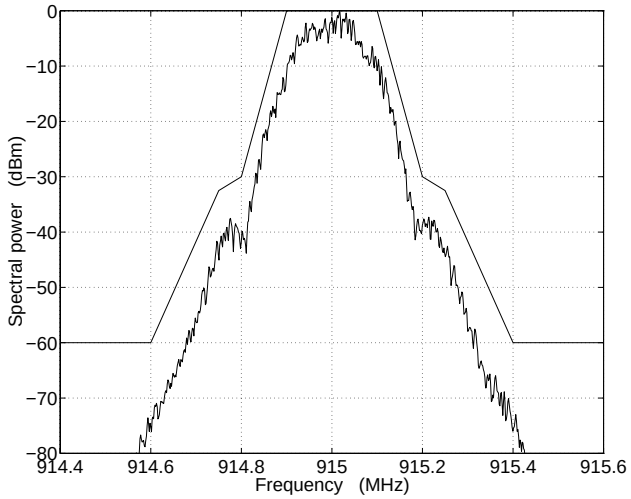

Fig. 9. Modulator RF spectrum with GSM modulation.

The RF spectrum exceeds the GSM spectral requirements and the spurious response is not difficult to meet since this architecture has no mixers and associated analog filters to introduce spurs. The only potential source of spurs are from limit cycles in the ΔΣ modulator with a DC input. These are inherently avoided since the modulation data keeps the ΔΣ modulator busy enough to randomize the quantization errors.

6. OPEN-LOOP GAIN CONTROL

The open-loop response and gain K of a conventional indirect synthesizer using analog loop filters and a VCO [2],[4] is generally unknown. The reason is that the filters cannot be realized to close specifications and the VCO sensitivity may vary due to process tolerances.

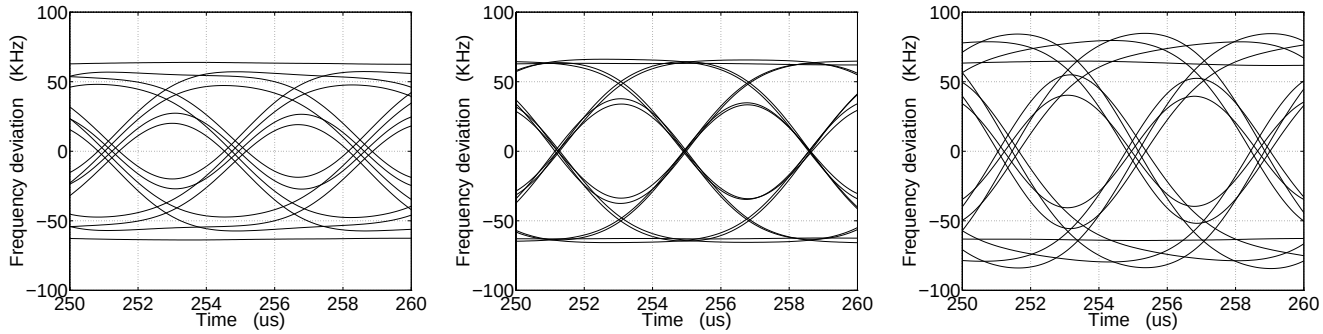

Fig. 10. Received GMSK baseband modulation with a) -20% gain error, b) no gain error, c) +20% gain error.

Traditionally, the solution to this problem is to provide some means of adjusting the filter response and open-loop gain K by using an active loop filter. In this architecture, the synthesizer loop gain is the only unknown parameter and is caused by deviation of the VCO sensitivity K_V due to process variations.

The effect of an open-loop gain error in the new modulator architecture of Fig. 4 is readily visible in the eye diagrams shown in Fig. 10. A -20% gain error (Fig. 10a)) results in significant closing of the eye and a reduced noise margin. Additionally, the zero crossing are spread over a larger time period and this makes the receiver more sensitive to timing errors. Conversely, a +20% gain error (Fig. 10c)) has a larger peak distortion with an adequate eye opening but the zero crossings remain spread leading to similar timing sensitivity. Therefore, some form of external adjustment is necessary to compensate for the gain error caused by the unknown VCO sensitivity. Practically, this needs to be done once since the VCO sensitivity wouldn't drift far from the initial process value although periodic corrections are possible.

A suitable compensation method is to measure the actual VCO sensitivity and compensate for it using the existing DSP. This can be done by tuning the synthesizer to the upper and lower GSM transmit frequencies and measuring the tuning voltage in each case. Conversion of the analog tuning voltage to a digital value can be accomplished using the same D/A converter that forms part of the loop filter so minimal extra hardware is required. Once the two tuning voltages have been obtained, a new K_V can be computed and the digital loop parameters adjusted accordingly.

7. CONCLUSIONS

A new GSM modulator architecture has been described that eliminates the complexity of conventional I and Q type modulators. The modulator is based on direct modulation of a $\Delta\Sigma$ frequency discriminator based synthesizer that produces the RF signal without up conversion. This technique retains the narrow loop bandwidth for adequate $\Delta\Sigma$ quantization noise suppression while extending the modulation bandwidth by an order of magnitude to accommodate the data rate. The architecture is predominantly digital which results in a system suitable for monolithic integration and offers significant cost reduction.

ACKNOWLEDGMENTS

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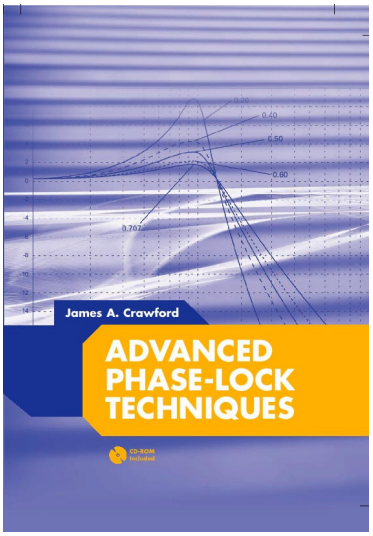

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3	*Fundamental Limits* A detailed discussion of the many fundamental limits that PLL designers may have to be attentive to or else never achieve their lofty performance objectives, e.g., Paley-Wiener Criterion, Poisson Sum, Time-Bandwidth Product.	38
4	*Noise in PLL-Based Systems* An extensive look at noise, its sources, and its modeling in PLL systems. Includes special attention to 1/*f* noise, and the creation of custom noise sources that exhibit specific power spectral densities.	66
5	*System Performance* A detailed look at phase noise and clock-jitter, and their effects on system performance. Attention given to transmitters, receivers, and specific signaling waveforms like OFDM, M-QAM, M-PSK. Relationships between EVM and image suppression are presented for the first time. The effect of phase noise on channel capacity and channel cutoff rate are also developed.	48
6	*Fundamental Concepts for Continuous-Time Systems* A thorough examination of the classical continuous-time PLL up through 4^{th}-order. The powerful Haggai constant phase-margin architecture is presented along with the type-3 PLL. Pseudo-continuous PLL systems (the most common PLL type in use today) are examined rigorously. Transient response calculation methods, 9 in total, are discussed in detail.	71
7	*Fundamental Concepts for Sampled-Data Control Systems* A thorough discussion of sampling effects in continuous-time systems is developed in terms of the *z*-transform, and closed-form results given through 4^{th}-order.	32
8	*Fractional-N Frequency Synthesizers* A historic look at the fractional-N frequency synthesis method based on the U.S. patent record is first presented, followed by a thorough treatment of the concept based on Δ-Σ methods.	54
9	*Oscillators* An exhaustive look at oscillator fundamentals, configurations, and their use in PLL systems.	62
10	*Clock and Data Recovery* Bit synchronization and clock recovery are developed in rigorous terms and compared to the theoretical performance attainable as dictated by the Cramer-Rao bound.	52